Low-Power RF Front-End Design for Wireless Body Area Networks

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(ABSTRACT)

Wireless body area networks (WBANs) have tremendous potential to benefit from wireless communication technology and are expected to make sweeping changes in the future human health care and medical fields. While the prospects for WBAN products are high, meeting required device performance with a meager amount of power consumption poses significant design challenges. In order to address these issues, IEEE has recently developed a draft of IEEE 802.15.6 standard dedicated to low bit-rate short-range wireless communications on, in, or around the human body. Commercially available SoC (System-on-Chip) devices targeted for WBAN applications typically embed proprietary wireless transceivers. However, those devices usually do not meet the quality of service (QoS), low power, and/or noninterference necessary for WBAN applications, nor meet the IEEE standard specifications. This dissertation presents a design of low-power RF front-end conforming to the IEEE standard in Medical Communication Service (MICS) band of 402-405 MHz.

First, we investigated IEEE 802.15.6 PHY specifications for narrow band WBAN applications. System performance analysis and simulation for an AWGN (additive white Gaussian noise) channel was conducted to obtain the BER (bit error rate) and the PER (packet error rate) as the figure of merit. Based on the system performance study, the link budget was derived as a groundwork for our RF front-end design. Next, we examined candidate RF front-end architectures suitable for MICS applications. Based on our study, we proposed to adopt a direct conversion transmitter and a low-IF receiver architecture for the RF front-end. An asynchronous wake-up receiver was also proposed, which is composed of a carrier sensing circuit and a serial code detector. Third, we proposed and implemented low-power building blocks of the proposed RF front-end. Two quadrature signal generation techniques were proposed and implemented for generation of
quadrature frequency sources. The two quadrature voltage controlled oscillators (QVCOs) were designed using our proposed current-reuse VCO with two damping resistors. A stacked LNA and a down-conversion mixer were proposed for low supply and low power operation for the receiver front-end. A driver amplifier and an up-conversion mixer for the transmitter front-end were implemented. The proposed driver amplifier uses cascaded PMOS transistors to minimize the Miller effect and enhance the input/output isolation. The up-conversion mixer is based on a Gilbert cell with resistive loads. Simulation results and performance comparisons for each designed building block are presented. Finally, we present a case study on a direct VCO modulation transmitter and a super-regenerative receiver, which can also be suitable for an MICS transceiver. Several crucial building blocks including a digitally-controlled oscillator (DCO) and quench signal generators are proposed and implemented with a small number of external components.
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Dedication

To my reverend parents and parents-in-law

To my beloved family,

Gyu Hee Park and Jae Ryeong Kim

Thank you for your endless support and incredible patience.
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Chapter 1:
Introduction

Advances in modern wireless technology, along with evolutionary integrated IC technology, has ushered a new era for implantable medical devices. The proliferation of implantable medical devices reduces the possibility of infections and inconveniences to patients [1]-[5]. Implantable medical devices become more effective through formation of a network, usually called wireless body area network (WBAN). In fact, a WBAN can go beyond implantable devices; WBAN applications include medical, consumer electronics, personal entertainments, and so on. Owing to the market demand, WBAN research thus far has concentrated on healthcare applications. Low power wireless devices for biomedical applications such as patient monitoring, swallowable endoscopies, and implantable biomedical solutions are expected to make sweeping changes in the health care and the medical fields [1]. They will usher a new generation of wireless control and monitoring applications that were inconceivable in the past.

The ITU-R recommended the Medical Implant Communication Service (MICS) band of 402-405 MHz over a decade ago, and various regions of the world including US, Europe, and Australia have arranged the regulatory standards to support use of MICS devices. The MICS band has the signal propagation characteristics conductive to the propagation of radio signals in the human body. The band is compatible with the incumbent users of the band (meteorological aids such as weather balloons). In addition, the band is globally available due to the international frequency allocations [6],[7]. IEEE approved the formation of a working group IEEE802.15.6 in December 2007, whose task was to develop WBAN standards in response to the needs for short range wireless communications on, in, or around human body [6].

While the prospect for WBAN products is high, meeting the required device performance with an extremely small amount of power consumption poses significant
design challenges. Those implantable devices should be able to operate for a long period with tiny batteries or energy scavenged from the ambient, while having small form factors to enable them implantable. Commercial SoC (System-on-Chip) devices targeted for WBAN applications typically embed proprietary wireless transceivers [4],[5], and consume more than 10 mW during operation. Further, they often fail to meet the required quality of service (QoS), which is important for WBAN applications.

Many solutions have been presented in the past years for the realization of ultra low-power MICS band transceivers. To maximize battery life and reduce the form factor, simple radio architectures and modulation schemes are usually adopted. As for the receiver, super-regenerative architecture using on-off keying (OOK) modulation is reported in [8]. The receiver consumes fairly large power (5.5 mW) and uses a complex quench control scheme. Frequency shift keying (FSK) is a popular approach due to its relatively simple hardware complexity. Examples of FSK implementations based on direct conversion or low-IF systems are found in [3],[9]. A dual-receiver system supporting both OOK and FSK is also demonstrated in [4]. MICS transmitters usually adopt FSK modulation scheme, since its constant envelope characteristic increases efficiency of power amplifiers, thereby enabling longer battery life. Direct modulation transmitter and direct conversion BFSK transmitter using all digital frequency locked loop (ADFLL) are presented in [10] and [11], respectively.

It is well known that the front-end of a wireless device dissipates most power of the system, and it is particularly true for small wireless devices such as for WBANs and wireless sensor networks. Hence, reduction of power dissipation for the RF front-end of a WBAN device is crucial to minimize the overall power dissipation. It should be noted that current Personal Area Networks (PANs) do not meet the medical (proximity to human tissue) and relevant communication regulations. Thus, this research investigates low power RF front-end design for implant devices operating in the MICS band (402-405 MHz). Specifically, it endeavors to answer the following questions:
1) What are the unique characteristics that could be exploited for low-power MICS RF transceiver design?

2) What are the specifications and requirements imposed by the recently developed IEEE standard for the RF transceiver design?

3) Which transceiver architecture is best suited for low-power MICS transceivers?

4) How can we effectively achieve low-voltage and low-power operation of building blocks targeting for fully monolithic implementation?

The proposed dissertation research attempts to answer the above questions, and the answers presented in each chapter are the major contributions of the dissertation research. The research results presented in this dissertation enable designers to design ultra-low power RF front-end tailored to MICS applications.

Chapter 2 tries to answer the first question. We identify the objectives of WBANs and present channel models with possible communication scenarios, which are being actively discussed at the IEEE standardization subcommittee. Exploiting the low emission limit requirements (-16 dBm EIRP) of the MICS band, unique features such as relaxed frequency stability criteria and excellent temperature regulation property of human body are explored.

Chapter 3 intends to answer the second question and investigates baseband signal processing techniques and the modulation scheme employed in the IEEE 802.15.6 PHY specifications for the narrow band WBAN applications. We start with introduction of the requirements for WBAN applications. Then, we address issues related with generation of packet service data units. System performance analysis and simulation with MATLAB for the AWGN (additive white Gaussian Noise) channel are presented as the BER (bit error rate) as the figure of merit. The simulation setup is shown in Figure 1.1. We also provide the simulation results with respect to the processing gain and the PER (packet error rate). Based on the system performance simulation, we derive the link budget necessary for RF front end design.
Chapter 4 presents answers to the third question and describes RF front-end architectures for an MICS transceiver. Various candidate architectures including direct-VCO (voltage controlled oscillator) modulation, direct conversion, and low-IF architectures are examined. Based on the study, we propose to adopt a direct conversion transmitter and a low-IF receiver architecture for the RF front-end as shown in Figure 1.2. We also propose an asynchronous wake-up receiver, which is composed of a carrier sensing circuit and a serial code detector [35].

Chapter 5 answers the last question and presents design of low-power building blocks of the proposed RF front-end. First, we present two quadrature signal generation techniques [45],[48]. Both quadrature voltage controlled oscillators (QVCOs) are designed using our current-reuse VCO with two damping resistors. Next, we present stacking of an LNA and a down-conversion mixer, which reduces the supply voltage and the power dissipation [64]. We also present a low power driver amplifier (DA) and an up-conversion mixer. The proposed DA uses cascaded PMOS (p-type metal oxide silicon) transistors to minimize the Miller effect and enhance the input/output isolation. The up-conversion mixer is based on the Gilbert cell with resistive loads. A direct antenna matching scheme is also explored and proposed. We present simulation results of each building block and compare its performance with other related works.

Chapter 6 provides another answer to the third and fourth questions. We present a case study that proposes to use a direct VCO modulation transmitter and a super-regenerative receiver for an MICS transceiver. We show that the asymmetric transceiver architecture is also well suited for the MICS application owing to its low circuit complexity to result in low power. Several key building blocks including digitally-controlled oscillator (DCO) and quench signal generators were investigated and implemented with a small number of external components. Simulation result of the building blocks is presented. Finally, Chapter 7 summarizes and concludes the dissertation research.
Figure 1.1: Simulation Block Diagram for the Proposed MICS Transceiver

Figure 1.2: Proposed Transceiver Architecture for MICS Applications
Chapter 2: Preliminaries

Wireless Body Area Network (WBAN) systems and their respective transceivers must be optimized to consume as little energy as possible while achieving acceptable levels of performance. There are several critical features that could be exploited in order to ensure WBAN transceivers to operate at the minimum level of energy required. In this chapter, we present our observation of the featuring characteristics of the target application, WBAN. We describe the objectives of WBAN and channel models considered by the IEEE standardization subcommittee. We also describe unique features of the Medical Implant Communication Service (MICS) band.

2.1 Objectives of Wireless Body Area Network

In response to the needs for standardizing Wireless Body Area Network, the IEEE approved formation of a working group for IEEE802.15.6 wireless standard, known as WBAN, in December 2007. The working group intends to endow a future generation of short-range wireless communications on, in or around human body [6]. The working group targets for low-power devices and applications including medical and consumer electronics / personal entertainments.

A variety of applications will be supported by the WBAN standard. Sensor based biomedical applications such as vital signal monitoring, wearable medical devices, electrocardiogram (ECG), body temperature sensors are enumerated candidate examples. This will include body-centric solutions for future wearable computers. Similarly, the same technology can provide effective solutions for personal entertainment as well. The
existence of a body area network standard will provide opportunities to expand these product features, better healthcare and well being for the users.

Current Personal Area Network (PAN) does not meet the medical (proximity to human tissue) and relevant communication regulations for some application environments. They also do not support the combination of reliability (QoS), low power, appropriate data rate and noninterference required to broadly address the breadth of body area network applications. Addressing these problems, body area networks will open up a new set of applications in wireless communications with huge potential for a new market and offer a tremendous opportunity for researchers and developers to exploit its market potential. Figure 2.1 shows the scope and requirement of WBAN compared with other wireless technologies in term of data rate and power consumption. As shown in the figure, WBAN intend to cover the low-rate applications with the data rate below 10 Mbps under the restriction of very low power consumption.

Figure 2.1: Scope and Requirement of WBAN Compared with Other Technologies
2.2 Channel Models for WBAN

An important step for the development of a wireless body area network device is characterization of the electromagnetic wave propagation from devices that are close to or inside the human body. Significant efforts carried out to make channel models as realistic, but the complexity of the human tissue structure and the body shape makes it difficult to derive a simple path loss model for WBAN. As antennas for WBAN applications are placed on or inside the body, the WBAN channel model should take into account the influence of the body on the radio propagation [7].

An IEEE 802.15.6 subcommittee provided guidelines for the development of WBAN channel models. The subcommittee defined three types of nodes as below:

1) Implant node: A node that is placed inside the human body. This could be immediately below the skin to further deeper inside the body tissue

2) Body Surface node: A node that is placed on the surface of the human skin or at most 2 centimeters away

3) External node: A node that is not in contact with human skin (between a few centimeters and up to 5 meters away from the body)

The channel model is needed to evaluate the performance of a physical layer. Possible communication links between the three nodes are graphically displayed in Figure 2.2. Seven possible communication links for operation of IEEE 802.15.6 devices are identified. The links, along with their appropriate frequency bands, are listed in Table 2.1 [7]. The links are determined based on the location of the communicating nodes, i.e., implant, body surface and external. The links are grouped into four classes that can be represented by the same channel models (CM) as shown in the table. The IEEE standard group is making their efforts to develop standards for physical and MAC layers based on the channel models. MICS (400 MHz) and several ISM (600, 900 MHz, 2.4 GHz) bands are recommended for the use of in and around the human body. UWB (3.1-10.6 GHz) band is being considered for the wide-band communication link between external node and body surface. We discuss our target MICS band in detail in the subsequent section.
Figure 2.2: Possible Communication Links for WBAN

Table 2.1: List of Communications Scenarios

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Description</th>
<th>Frequency Band</th>
<th>Channel Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>Implant to Implant</td>
<td>402-405 MHz</td>
<td>CM1</td>
</tr>
<tr>
<td>S2</td>
<td>Implant to Body Surface</td>
<td>402-405 MHz</td>
<td>CM2</td>
</tr>
<tr>
<td>S3</td>
<td>Implant to External</td>
<td>402-405 MHz</td>
<td>CM2</td>
</tr>
<tr>
<td>S4</td>
<td>Body Surface to Body Surface (LOS)</td>
<td>13.5, 50, 400, 600, 900 MHz, 2.4, 3.1-10.6 GHz</td>
<td>CM3</td>
</tr>
<tr>
<td>S5</td>
<td>Body Surface to Body Surface (NLOS)</td>
<td>13.5, 50, 400, 600, 900 MHz, 2.4, 3.1-10.6 GHz</td>
<td>CM3</td>
</tr>
<tr>
<td>S6</td>
<td>Body Surface to External (LOS)</td>
<td>900 MHz, 2.4, 3.1-10.6 GHz</td>
<td>CM4</td>
</tr>
<tr>
<td>S7</td>
<td>Body Surface to External (NLOS)</td>
<td>900 MHz, 2.4, 3.1-10.6 GHz</td>
<td>CM4</td>
</tr>
</tbody>
</table>
2.3 Medical Implant Communication Service

Following Recommendation SA1346 of ITU-R in 1998, the FCC established the Medical Implant Communication Service (MICS) band of 402-405 MHz in 1999, and similar ones were established in Europe, Japan, South Korea in following years [12]. The MICS band is a shared secondary band license-free. No other devices are allowed to operate within this band except meteorological balloons which are the primary and incumbent users of the band. This helps reduce the risk of interference and blocking that could occur in a license-free band. The other countries also support the use of MICS devices for the same services, but often different names.

The MICS band supports use of a long range (typically 2 meters) high-speed wireless links. The MICS band overcomes the range limitations of inductive systems and facilitates the development of next generation medical devices with improved patient health care. MICS would greatly improve the utility of medical implant devices by allowing physicians to establish high-speed, easy-to-use, reliable, short-range wireless links to such devices as monitoring and control equipments [12].

Requirements for MICS transceivers are available in the ITU-R Recommendation SA.1346. The main requirements for MICS devices include a maximum equivalent isotropically radiated power (EIRP) of -16 dBm (24 μW). A number of segmented minimum channel spacing of 25 kHz can be combined for the use of ten channels to provide for a bandwidth of up to 300 kHz. The channel emission limit is illustrated in Figure 2.2. Maximum EIRP limit is applied to any 300 kHz bandwidth and the out-of-band emission is limited up to -20 dB from the carrier. Interference mitigation techniques such as LBT (Listen-Before-Talk) for programmer/control transmitters and AFA (Adaptive Frequency Agile) mechanisms are also required to manage channels across MICS systems [12].

Compared to other available frequencies, the MICS frequency band is well suited for the technical requirements of the MICS. The signal propagation characteristic of the band is conductive to the transmission of radio signals in the human body. The band is compatible with the incumbent user of the band (Meteorological aids such as weather
baloons). In addition, the band is globally available due to the international frequency allocations.

![Welch Power Spectral Density Estimate](image)

**Figure 2.3: Emission Limit for an MICS Chanel**

### 2.4 Unique Characteristics of MICS Applications

Medical implant communication systems have unique operating environments. The human body, in which medical implant communication systems are embedded, rarely exhibits abrupt temperature changes and its moderate shifts occur very slowly. The temperature regulation of a human body can be exploited to reduce system design complexity, power consumption, and the device size. FCC regulation standard requires each transmitter in the MICS service maintain a frequency stability of only 100 ppm of the operating frequency over the range of 25°C to 45°C for medical implant transmitters; and 0°C to 55°C for medical implant programmer/control transmitters [7]. The provision does not impose stringent frequency stability criteria for an MICS transmitter compared to other modern radios. For example, cellular phones are required to maintain a frequency stability of less than 1 ppm in the temperature range of -40°C to 85°C. The relaxed
frequency stability requirement can be exploited in design of medical implants. For instance, an external crystal oscillator can be replaced with an on-chip oscillator, which ensures minimum use of external components.

Another important feature that could be exploited for MICS applications is that most biomedical information has low bandwidth, and resultantly MICS transmitters can be operated with a low duty cycle. Since the biomedical information changes little during the monitoring period, a low speed A/D converter can be used for digitization of the information. The sampled data can be accumulated in the memory residing in the implant node. During the data acquisition, transmitters can sleep most of the time. Once the digitized data is ready to send, the transmitter turns on briefly and sends the data packets in a short period. This feature of the operational trait can lead to a simpler topology in transmitter architectures that consume less power, but are less spectrally efficient [12],[13].

Note that spectrum efficiency inherently entails complex transmitter architectures that usually consume relatively large power compared to simpler ones. Further, an MICS transmitter can trade spectrum inefficiency for ultra-low power consumption. For instance, direct-modulation FSK transmitters consume less power than PSK and QAM transmitters, but spectrally less efficient.

2.5 Summary of Preliminaries

In this chapter, we identified the objectives of wireless body area network. We reviewed channel models and possible communication scenarios, which are being actively discussed in the IEEE standardization subcommittee. We noted the MICS band for the use of in-body communication link. The MICS band (402-405 MHz) supports the use of short range (typically 2 meters) wireless links. The main requirements for MICS devices lie in the maximum equivalent isotropically radiated power (EIRP) of -16 dBm (24 μW). Along with the low emission limit, relaxed frequency stability requirement is found as another critical feature that could be exploited.

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Chapter 3:
IEEE 802.15.6 Narrowband Standard

In this chapter, we investigate the newly developed draft IEEE 802.15.6 PHY specification for narrow band WBAN applications. Baseband signal processing schemes and modulation parameters are investigated in detail. System performance analysis with the ideal transceiver in AWGN channel is presented with the BER as the figure of merit. Based on the performance analysis, we derive the link budget for the ground work of RF Front-end design.

3.1 Overview of the Draft Standard

The draft IEEE 802.15.6 is a newly developed standard dedicated to low bit-rate WBAN used for low power applications [14]. The standard supports short range, wireless communication in the vicinity of, or inside, a human body. It uses existing ISM bands approved by national medical and/or regulatory authorities. Current Personal Area network (PAN) does not meet the relevant communication regulations for some application environments. Moreover, they do not support the combination of reliability, Quality of Service (QoS), low power, data rate and noninterference required to broadly address the breadth of WBAN applications. In that perspective, there is a need for a standard optimized for ultra-low power devices operating on, in or around the human body to serve a variety of applications including medical and personal entertainment. The requirements for WBAN applications are list as follows [14]:

- Very low-power consumption
- Low-complexity
- Robust wireless link to support bounded latency and minimize data loss
- PHY information data rate should be greater than the sensor information data rate to allow devices to save power via duty cycling and hibernation
- Support for multiple co-located WBAN networks
- Coexistence with other networks
- Robustness to other wireless technologies
- Support for multiple frequency band to enable operation within or on the body

The physical layer (PHY) protocol for WBAN covers packet structure, modulation, preamble, etc and is responsible for the following tasks:

- Activation and deactivation of the radio transceiver
- Clear channel assessment (CCA) within the current channel
- Data transmission and reception

Figure 3.1 is the block diagram of an example of baseband signal processor for the generation of packets or packet service data unit (PSDU). The physical layer of this standard adopts simple and low-complexity channel coding schemes such as BCH, spreading, interleaving, and scrambling. As shown in the Figure 3.1, the modulator first encodes the information bits provided by the MAC using BCH encoding process. If the spreading factor is 2 or 4, the resulting un-coded or coded bits are spread using a repetition code and then interleaved using a bit interleaver. The resulting bit stream is then scrambled to mitigate burst errors. Finally, the resulting scrambled bit stream is then mapped onto the appropriate constellation using rotated differential phase shift keying ($\pi/n$-DMPSK) with square root raised cosine (SRRC) pulse shaping, which is determined by the data rate and frequency band of operation.
3.2 Physical Layer Specification

3.2.1 Baseband Data Processing

3.2.1.1 Packet Structure

Figure 3.2 shows the format for the physical layer protocol data unit (PPDU), which is composed of three main components: the PLCP preamble, the PLCP header and the PSDU [14]. The components are listed in the order of transmission. The PLCP preamble is the first component of the PPDU. The purpose of the preamble is to aid the receiver in the timing synchronization and carrier-offset recovery.

The PLCP header is the second main component of the PPDU. The purpose of this component is to convey the necessary information about the physical layer (PHY) and media access control (MAC) parameters to aid in the decoding of the PSDU at the receiver. The PLCP header can be further decomposed into a RATE field, a LENGTH field, a SCRAMBLER SEED, a BURST MODE field, reserved bits, a header check sequence (HCS), and BCH parity bits. The BCH parity bits are added in order to improve the robustness of the PLCP header. The PLCP header is transmitted using the given header data rate in the operating frequency band.
The PSDU is the last component of the PPDU. This component is formed by concatenating the MAC header with the MAC frame body and frame check sequence (FCS). The PSDU is then scrambled and optionally encoded by a BCH code. The PSDU is transmitted using any of the available data rates in the operating frequency band.

![IEEE 802.15.6 PPDU Structure](image)

Figure 3.2: IEEE 802.15.6 PPDU Structure

### 3.2.1.2 BCH Encoding

The information bits are encoded using BCH encoding process with a code rate of 51/63 for PSDU generation. Meanwhile a systematic BCH $(31, 19, \ t=2)$ code which is a shortened code derived from a BCH $(63, 51, \ t=2)$ is used for PLCP header generation. Figure 3.3 illustrates the BCH encoding process for a single codeword. Before encoding, shortening bits are added and equally distributed over all codewords. After encoding, the shortened bits are removed prior to transmission. The shortened bits are never transmitted on-air. The generator polynomial for a systematic BCH $(63,51,t=2)$ code is given as:

\[
g(x) = 1 + x^3 + x^4 + x^5 + x^8 + x^{10} + x^{12}
\]  

(3.1)

![BCH Encoding Process for a Single Codeword](image)

Figure 3.3: BCH Encoding Process for a Single Codeword
3.2.1.3 Spreading

The standard uses very simple spreading scheme which is basically repetition of the information bits. For example, for a spreading factor of 2, each input bit is repeated two times. For a spreading factor of 4, each input bit is repeated four times as illustrated in Figure 3.4.

![Spreading Scheme](image)

3.2.1.4 Bit Interleaving

In order to provide robustness against error propagation, the output of the spreader is interleaved prior to modulation. The repeated bits are interleaved using simple, low-complexity two-bit interleaver. The bit interleaving operation is performed by first grouping the spread bits into blocks of $2S$ bits, where $S$ is the spreading factor, and then using a block interleaver of size $2S$ to permute the bits. Let the sequences $a(i)$ and $b(i)$, where $i=0,1,...,2S-1$, represent the input and output bits of the $2S$ bit interleaver, respectively. The output of the $2S$ bit interleaver is given by the following relationship:

$$b(i) = a\left(S \times \text{rem}(i, 2) + \left\lfloor \frac{i}{2} \right\rfloor \right) \quad i = 0,1,...,2S - 1$$

(3.2)

By combing interleaving together with spreading and low complexity binary block codes, we can get robustness for multipath and interference. The interleaving procedure for the example ($S = 2$) is graphically illustrated in Figure 3.5.
3.2.1.5 Data Scrambling

For the scrambler, a polynomial \( G(x) = 1 + x^2 + x^{12} + x^{13} + x^{14} \) is used to whiten the data. Figure 3.6 shows a typical implementation of the side-stream scrambler. The output of the scrambler is generated as:

\[
x[n] = x[n-2] \oplus x[n-12] \oplus x[n-13] \oplus x[n-14]
\]  
(3.3)

where “\( \oplus \)” denotes modulo-2 addition. Table 3.1 defines the initialization vector, \( x_{init} \), for the side-stream scrambler as a function of the scrambler seed (SS) value which is found in the PLCP header. The initialization vector is determined from the scrambler seed value in the PHY header of the received frame.
### Table 3.1: Scrambler Seed Selection

<table>
<thead>
<tr>
<th>Scrambler Seed (SS)</th>
<th>Initialization Vector $x_{\text{init}} = x[-1]x[-2]...x[-14]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>00101111001101</td>
</tr>
<tr>
<td>1</td>
<td>00000001001111</td>
</tr>
</tbody>
</table>

#### 3.2.2 Data Rate Dependent Modulation

##### 3.2.2.1 Modulation Parameters

In order to enable operation within or on the body surface, the standard supports for multiple frequency bands. The data rate dependent parameters for each of the possible frequency band of operation are summarized in Table 3.2. For all the frequency bands except the 420 – 450 MHz band, the standard for PHY specifications employs differentially encoded PSK, also known as DPSK. The DPSK transceiver architecture makes it possible to implement a lower-cost non-coherent receiver rather than a coherent receiver that requires a carrier synchronization loop [15]. Offset modulation scheme is adopted to enhance signal bandwidth efficiency. Square root raised cosine (SRRC) is used to mitigate inter-symbol interference (ISI). The data rates are variable depending on both BCH code rates and spreading factors. Modulation parameters for PLCP header and PSDU for the MICS band are elaborated in Table 3.3.

Meanwhile, it is notable that the crowded three ISM frequency bands graded in Table 3.2 coincide with the bands for the IEEE 802.15.4 or Zigbee applications. In comparison to the IEEE 802.15.4 or ZigBee PHY standard, the PHY specifications for the WBAN are much more relaxed as shown in the Table 3.4 [16][17]. For example, transmitter power can be reduced to -10 dBm which is 10 dB lower than that of ZigBee standard. With only 3-5 m operational range, the low transmit power enables a simpler output power amplifier with reduced chip size and low power consumption.
Table 3.2: Modulation Parameters for Each Frequency Band

<table>
<thead>
<tr>
<th>Frequency bands</th>
<th>Modulation*</th>
<th>Symbol rate</th>
<th>Data rate**</th>
<th>Pulse shape</th>
</tr>
</thead>
<tbody>
<tr>
<td>402 – 405 MHz</td>
<td>π/2-DBPSK</td>
<td>187.5 kps</td>
<td>57.5 ~ 455.4 kbps</td>
<td>SRRC***</td>
</tr>
<tr>
<td></td>
<td>π/4-DQPSK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>π/8-D8PSK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>420 – 450 MHz</td>
<td>GMSK</td>
<td>187.5 kps</td>
<td>57.5 ~ 187.5 kbps</td>
<td>BT = 0.5</td>
</tr>
<tr>
<td>863 – 870 MHz</td>
<td>π/2-DBPSK</td>
<td>250 kps</td>
<td>76.7 ~ 607.1 kbps</td>
<td>SRRC</td>
</tr>
<tr>
<td></td>
<td>π/4-DQPSK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>π/8-D8PSK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>902 – 928 MHz</td>
<td>π/2-DBPSK</td>
<td>300 kps</td>
<td>91.9 ~ 728.6 kbps</td>
<td>SRRC</td>
</tr>
<tr>
<td></td>
<td>π/4-DQPSK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>π/8-D8PSK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>950 – 956 MHz</td>
<td>π/2-DBPSK</td>
<td>250 kps</td>
<td>76.7 ~ 607.1 kbps</td>
<td>SRRC</td>
</tr>
<tr>
<td></td>
<td>π/4-DQPSK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>π/8-D8PSK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2360 – 2400 MHz</td>
<td>π/2-DBPSK</td>
<td>600 kps</td>
<td>91.9 ~ 971.4 kbps</td>
<td>SRRC</td>
</tr>
<tr>
<td></td>
<td>π/4-DQPSK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2400 – 2483.5 MHz</td>
<td>π/2-DBPSK</td>
<td>600 kps</td>
<td>91.9 ~ 971.4 kbps</td>
<td>SRRC</td>
</tr>
<tr>
<td></td>
<td>π/4-DQPSK</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(*) π/2-DBPSK and π/4-DQPSK are mandatory but π/8-D8PSK is optional except for 420-450 MHz. (**) Data rate is dependent on the code rate and spreading factor. (***) Square Root Raised Cosine

Table 3.3: Modulation Parameters for MICS Band (402-405 MHz)

<table>
<thead>
<tr>
<th>Packet</th>
<th>Modulation</th>
<th>Symbol Rate (kps)</th>
<th>Code Rate (k/n)</th>
<th>Spreading Factor</th>
<th>Data Rate (kbps)</th>
<th>Pulse shape</th>
<th>Pulse shape</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>π/2-DBPSK</td>
<td>187.5</td>
<td>19/31</td>
<td>2</td>
<td>57.5</td>
<td>SRRC</td>
<td>Mandatory</td>
</tr>
<tr>
<td>PSDU</td>
<td>π/2-DBPSK</td>
<td>187.5</td>
<td>51/63</td>
<td>2</td>
<td>75.9</td>
<td>SRRC</td>
<td>Mandatory</td>
</tr>
<tr>
<td>PSDU</td>
<td>π/2-DBPSK</td>
<td>187.5</td>
<td>51/63</td>
<td>1</td>
<td>151.8</td>
<td>SRRC</td>
<td>Mandatory</td>
</tr>
<tr>
<td>PSDU</td>
<td>π/4-DQPSK</td>
<td>187.5</td>
<td>51/63</td>
<td>1</td>
<td>303.6</td>
<td>SRRC</td>
<td>Mandatory</td>
</tr>
<tr>
<td>PSDU</td>
<td>π/8-D8PSK</td>
<td>187.5</td>
<td>51/63</td>
<td>1</td>
<td>455.4</td>
<td>SRRC</td>
<td>Optional</td>
</tr>
</tbody>
</table>

(*) π/4-DQPSK is also mandatory and π/8-D8PSK is optional except for 420-450 MHz. (**) Data rate is dependent on the code rate and spreading factor. (***) Square Root Raised Cosine
### Table 3.4: IEEE 802.15.6 PHY Specifications and RF Requirements

<table>
<thead>
<tr>
<th>PHY</th>
<th>868/915 MHz PHY</th>
<th>2.4 GHz PHY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency band</td>
<td>868-868.6 MHz</td>
<td>902-928 MHz</td>
</tr>
<tr>
<td>Channel spacing</td>
<td>0.4 MHz</td>
<td>0.5 MHz</td>
</tr>
<tr>
<td>Transmit power (Min.)</td>
<td>-10 dBm</td>
<td>-10 dBm</td>
</tr>
<tr>
<td>Sensitivity (Min.)</td>
<td>-97 dBm</td>
<td>-97 dBm</td>
</tr>
<tr>
<td>Sensitivity (Max.)</td>
<td>-26 dBm</td>
<td>-26 dBm</td>
</tr>
<tr>
<td>Noise figure</td>
<td>&lt; 17 dB</td>
<td>&lt; 17 dB</td>
</tr>
</tbody>
</table>

#### 3.2.2.2 Rotated Differential MPSK

One notable thing for the narrow band (NB) WBAN is that it adopts rotated differential phase shift keying (PSK) scheme for the modulation. The bit stream is mapped onto one of three rotated and differentially-encoded constellations: π/2-DBPSK, π/4-DQPSK, or π/8-D8PSK. The binary bit stream with size of \( N, a(n), n = 0,1,\ldots,N-1 \), is mapped onto a corresponding complex-values sequence \( S(k), k = 0,1,\ldots,(N/\log_2(M))-1 \) for an \( M \)-ary system as follows:

\[
S(k) = S(k-1)\exp(j\theta_k) \quad k = 1,2,\ldots,(N/\log_2(M))-1
\]  

(3.4)

where \( S(0) = \exp(j\pi/M) \) and the relationship between the bit stream \( a(n) \) and the phase change \( \theta_k \) is given in Table 3.5, Table 3.6, Table 3.7 for π/2-DBPSK, π/4-DQPSK, and π/8-D8PSK, respectively. The π/2-DBPSK signal is generated from a set of constellations that are rotated by π/2 with respect to each other [18]. As such, π/M-DMPSK signal has constellations that are rotated by π/M at each symbol. Figure 3.7 illustrates constellations for π/2-DBPSK (a) and π/4-DQPSK (b).

Figure 3.8 is the simulation result for the π/4-DQPSK signals and its constellation diagrams. In this figure, left ones are for the unfiltered signal and right ones are filtered with square root raised cosine (SRRC) filter, which will be elaborated in the subsequent section. Given a point on one of the signal constellations that corresponds to two bits of input data, two new bits are read to determine the next point that is selected from the
other constellation. That is, the two new input bits cause a phase shift of ±45° or ±135°, depending on their value [18]. Hence, the phase transition of the signal can be mitigated by adopting rotated phase shifting scheme, which prevents the spectral regrowth and widening [19]. The less envelope fluctuation or spectral regrowth requires more relaxed linear power amplifier implementation [20],[21]. Another attractive feature of the π/\(M\)DMPSK modulation scheme is that it can be non-coherently detected so that a lower-cost non-coherent receiver can be implemented rather than a coherent receiver that requires a carrier synchronization loop [15].

Table 3.5: \(\pi/2\)-DBPSK Mapping

<table>
<thead>
<tr>
<th>(a(n))</th>
<th>(\theta_k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>(\pi/2)</td>
</tr>
<tr>
<td>1</td>
<td>(3\pi/2)</td>
</tr>
</tbody>
</table>

Table 3.6: \(\pi/4\)-DQPSK Mapping

<table>
<thead>
<tr>
<th>(a(2n))</th>
<th>(a(2n+1))</th>
<th>(\theta_k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>(\pi/4)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>(3\pi/4)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>(7\pi/4)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>(5\pi/4)</td>
</tr>
</tbody>
</table>

Table 3.7: \(\pi/8\)-D8PSK Mapping

<table>
<thead>
<tr>
<th>(a(3n))</th>
<th>(a(3n+1))</th>
<th>(a(3n+2))</th>
<th>(\theta_k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(\pi/8)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>(3\pi/8)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>(7\pi/8)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>(5\pi/8)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(15\pi/8)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>(13\pi/8)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>(9\pi/8)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>(11\pi/8)</td>
</tr>
</tbody>
</table>
Figure 3.7: Signal Constellations for $\pi/2$-DBPSK (a) and $\pi/4$-DQPSK (b)

Figure 3.8: I-Q Signals and Constellations for $\pi/4$-DQPSK
3.2.2.3 Square Root Raised Cosine Pulse Shaping

The pulse shape used for data transmission is the square root raised cosine (SRRC) pulse which is one of zero inter-symbol interference (ISI) pulse shapes. SRRC pulse is derived from the raised cosine pulse whose frequency response $H_{RC}(f)$ is square of that of the raised cosine pulse, $H_{SQRC}(f)$ so that:

$$H_{SQRC}(f) = \sqrt{|H_{RC}(f)|}$$  (3.5)

The inverse Fourier transform gives the time-domain SRRC pulse shape as [23]:

$$h_{SQRC}(t) = 4\beta \frac{\cos \left(1+\beta \frac{\pi}{T}\right) + \sin \left(1-\beta \frac{\pi}{T}\right) (4\beta T/T')^{-1}}{\pi \sqrt{T} \left[1 - \left(4\beta t/T\right)^2\right]}$$  (3.6)

where $\beta$ is the roll-off factor and $T$ is the symbol duration. The top pane in Figure 3.9 illustrates the impulse response of SRRC filter whose roll off factor = 0.32 and $T = 1$. Note that the zero crossings do not exactly occur at integer multiples of $T$. However, the convolution of SRRC filter with itself has the zero crossing falling at integer multiples of $T$ since the cascade combination of two SRRC is a zero-ISI as shown in the bottom pane of Figure 3.9 [24].

Figure 3.10 is the Power Spectral Density of MICS signals modulated in $\pi/4$-DQPSK. The left one is for the case of rectangular symbol pulses and the first sidelobe is attenuated by only 13.4 dB. The right one is for the case of SRRC filtering is used. As shown in the figure, the modulated signal meets the regulatory spectrum mask if the SRRC filtering is used. The output power requirement is -16 dBm EIRP for the MICS applications. The out-of-band emission is limited to -20 dB lower than that of the carrier frequency. With the SRRC pulse shaping filter, the output of the transmitter well meet the spectral requirement as shown in the right in Figure 3.10.
Figure 3.9: Impulse Response of SRRC filter (top) Convolution of Cascade of two SRRC Filters (bottom)

Figure 3.10: Power Spectral Density of π/4-DQPSK MICS Signals
3.2.2.4 Band Plan and Channelization

Table 3.8 shows seven candidate frequency bands and the relationship between center frequency, $f_c$, and channel number, $n_c$, for the narrow band (NB) WBAN applications. As shown in the table, the candidate frequency bands are 402 – 405 MHz, 420 – 450 MHz, 863 – 870 MHz, 902 – 928 MHz, 950 – 956 MHz, 2360 – 2400 MHz and 2400 – 2483.5 MHz. The mapping functions $g_1(n_c)$ and $g_2(n_c)$ used in the 420 – 450 MHz and 863 – 870 MHz frequency bands, respectively are defined as follows:

$$
g_1(n_c) = \begin{cases} 
\begin{align*}
n_c & \quad 0 \leq n_c \leq 1 \\
n_c + 6.875 & \quad 2 \leq n_c \leq 4 \\
n_c + 13.4 & \quad n_c = 5 \\
n_c + 35.025 & \quad 6 \leq n_c \leq 7 \\
n_c + 40.925 & \quad 8 \leq n_c \leq 9 \\
n_c + 47.25 & \quad 10 \leq n_c \leq 11
\end{align*}
\end{cases}
, \quad \text{and} \quad g_2(n_c) = \begin{cases} 
\begin{align*}
n_c & \quad 0 \leq n_c \leq 7 \\
n_c + 0.5 & \quad n_c = 8 \\
n_c + 1 & \quad 9 \leq n_c \leq 12 \\
n_c + 1.5 & \quad n_c = 13
\end{align*}
\end{cases}

(3.7)$$

The targeted MICS frequency band (402-405 MHz) has 10 channels with channel spacing of 300 kHz. Note that 79 channels are assigned in the crowded 2.4 GHz ISM band with 1 MHz channel spacing. Meanwhile, the IEEE 802.15.4 standard assigns 16 channels in the 2.4 GHz with ample channel spacing of 5 MHz.

Table 3.8: Relationship between Center Frequency and Channel Number

<table>
<thead>
<tr>
<th>Frequency Band (MHz)</th>
<th>Relationship between $f_c$ and $n_c$</th>
</tr>
</thead>
<tbody>
<tr>
<td>402-405</td>
<td>$f_c = 402.15 + 0.30 \times n_c$ (MHz), $n_c = 0, \ldots, 9$</td>
</tr>
<tr>
<td>420-450</td>
<td>$f_c = 420.30 + 0.50 \times g_1(n_c)$ (MHz), $n_c = 0, \ldots, 11$</td>
</tr>
<tr>
<td>863-870</td>
<td>$f_c = 863.20 + 0.40 \times g_2(n_c)$ (MHz), $n_c = 0, \ldots, 13$</td>
</tr>
<tr>
<td>902-928</td>
<td>$f_c = 903.50 + 0.50 \times n_c$ (MHz), $n_c = 0, \ldots, 47$</td>
</tr>
<tr>
<td>950-956</td>
<td>$f_c = 951.10 + 0.40 \times n_c$ (MHz), $n_c = 0, \ldots, 11$</td>
</tr>
<tr>
<td>2360-2400</td>
<td>$f_c = 2362.00 + 1.00 \times n_c$ (MHz), $n_c = 0, \ldots, 37$</td>
</tr>
<tr>
<td>2400-2483.5</td>
<td>$f_c = 2402.00 + 1.00 \times n_c$ (MHz), $n_c = 0, \ldots, 78$</td>
</tr>
</tbody>
</table>
3.3 Performance Evaluation

3.3.1 System Simulation Setup

Figure 3.11 shows block diagram of the simulation setup for our target MICS band transceiver. For the MICS band the symbol rate has the fixed value of 187.5 kbps. However, the information data rate varies from 75.9 to 455.4 kbps depending on their various coding schemes. The details are discussed in section 3.2.2 and summarized in Table 3.3. Three modulation schemes are chosen depending on their data rates: $\pi/2$-DBPSK, $\pi/4$-DQPSK, and $\pi/8$-D8PSK. BCH(63,51) coding is applied for PSDU generation. For PLCP Header generation, BCH(31,19) is used which is shortened code derived from a BCH(63,51). The coded bit stream is spreaded and interleaved optionally with the spreading factor (S) of two for the case of data rate 75.9 kbps when the modulation scheme is $\pi/2$-DBPSK. PLCP Header is also spreaded and interleaved with $\pi/2$-DBPSK modulation scheme. Simple scrambler is used for the robustness to the burst error. Square Root Raised Cosine (SRRC) filters are used in the transmitter and receiver, both having a roll off factor of 0.35. For simplicity, the signal is assumed to propagate through an additive white Gaussian noise (AWGN) channel with no fading, frequency selectivity, interference nonlinearity or dispersion.

![Simulation Block Diagram for MICS Transceiver](image)

Figure 3.11: Simulation Block Diagram for MICS Transceiver
3.3.2 Simulation Results

3.3.2.1 BER and PER for Rotated Differential PSK System

System performance has been investigated through MATLAB simulation using the bit error rate (BER) and packet error rate (PER) as the figure of merit. Figure 3.12 and Figure 3.13 show simulated BER and PER curves in an AWGN channel, where no coding scheme is applied. For the comparison, the BER and PER curves for QPSK are also plotted. As expected, coherently detected π/4-QPSK has the same BER as QPSK system, whose BER is given by [18]:

\[ P_e = Q\left(\sqrt{2SNR}\right) \]  

(3.8)

However, π/4-DQPSK has the higher BER compared to QPSK. For the same BER, differentially detected π/4-DQPSK requires about 3 dB more SNR than that for QPSK [18].

![Figure 3.12: BER Performance with No Coding](image-url)
The overall performance of the draft IEEE 802.15.6 PHY standard can be characterized with packet error rate (PER) that defines the average fraction of transmitted packets that are not detected correctly. The required PER should be less than 10% measured over random PHY service data unit (PSDU) of 255 octets. For small BER, the PER can be roughly approximated by multiplying the BER by the number of bits per packet given by:

\[ P_p = 1 - (1 - p_e)^N \approx Np_e \]  \hspace{1cm} (3.9)

where \( p_e \) is BER and \( N \) is number of bits per packet. The simulated PER as shown in Figure 3.13 exhibits that the ideal receiver requires minimum SNR of about 9.5 dB for \( \pi/2 \)-DBPSK, 11.2 dB for \( \pi/4 \)-DQPSK, and 15 dB for \( \pi/8 \)-D8PSK, respectively [22].

Figure 3.13: PER Performance with No Coding
3.3.2.2 BER Processing Gain

Employing various coding schemes as shown in Figure 3.11, the transceiver is expected to have processing gain. With the BCH\((n=63,k=51,t=2)\), the coding gain is approximately calculated as \(kt/n = 1.6\) dB [23]. The simulated BER curves for the transceiver in Figure 3.11 over AWGN channel are plotted in Figure 3.14 and Figure 3.15. The simulated result shows that the BER curves well behave as expected with a certain amount of processing gain. For the \(\pi/2\)-DBPSK case, simple spreading is also used, which is repetition of the information bits \(S\) times. Simulation result shows that the spreading scheme has additional 0.5 dB processing gain.

![Figure 3.14: BER Performance for \(\pi/2\)-DBPSK with Coding](image)

Figure 3.14: BER Performance for \(\pi/2\)-DBPSK with Coding
3.3.2.3 PER Processing Gain

The simulated PER curves are plotted in Figure 3.16, Figure 3.17, and Figure 3.18. Employing coding schemes, the receiver has processing gains of 2.2 dB for \( \pi/2 \)-DBPSK, 2.9 dB for \( \pi/4 \)-DQPSK, and 3.3 dB for \( \pi/8 \)-D8PSK, respectively, for PER = 0.1 as required by the standard. Again, repetition spreading is also applied and simulated for the \( \pi/2 \)-DBPSK system. As shown in Figure 3.16, additional processing gain of 0.2 dB is achieved with the spreading scheme. Table 3.9 summarizes simulation results of the required minimum SNR (PER = 1) for each modulation schemes.

Table 3.9: Required Minimum SNR and Processing Gains

<table>
<thead>
<tr>
<th></th>
<th>( \pi/2 )-DBPSK*</th>
<th>( \pi/2 )-DBPSK</th>
<th>( \pi/4 )-DQPSK</th>
<th>( \pi/8 )-D8PSK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. Req. SNR (No Code)</td>
<td>9.5 dB</td>
<td>9.5 dB</td>
<td>11.2 dB</td>
<td>15.0 dB</td>
</tr>
<tr>
<td>Min. Req. SNR (Code)</td>
<td>7.1 dB</td>
<td>7.3 dB</td>
<td>8.3 dB</td>
<td>11.7 dB</td>
</tr>
<tr>
<td>Processing Gain</td>
<td>2.4 dB</td>
<td>2.2 dB</td>
<td>2.9 dB</td>
<td>3.3 dB</td>
</tr>
</tbody>
</table>

* \( \pi/2 \)-DBPSK applied with spreading as well as coding
Figure 3.16: PER Performance for $\pi/2$-DBPSK with Coding

Figure 3.17: PER Performance for $\pi/4$-DQPSK with Coding
3.3.3 Link Budget Analysis

Table 3.10 is the link budget analysis for each data rate option in the MICS band. Here we assumed the antenna gain is 0 dB and implementation loss is 6 dB. The path loss is classified into two: inside body and outside body. Those data are based on the actual measurements reported in [25]. The SNRs for each data rate option used here are calculated from the simulation results. Resultant maximum allowed system noise figure (NF) ranges from 22.95 dB to 17.35 dB. Considering the Zigbee standard requires minimum 19 dB for the overall system noise figure [17], the MICS band WBAN application requires more relaxed specification. However, for the higher data rate such as 455.4 kbps, the allowable system NF is not so relaxed compared to the Zigbee counterpart. The analysis guides some groundwork for the choice of transceiver architecture and building blocks. The relaxed requirements can be exploited to choose and design ultra-low power circuit topologies sacrificing the other performance parameters.
Table 3.10: Link Budget Analysis for MICS band

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Unit</th>
<th>Mand. 1</th>
<th>Mand. 2</th>
<th>Mand. 3</th>
<th>Optional</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate ($R_b$)</td>
<td>kbps</td>
<td>75.9</td>
<td>151.8</td>
<td>303.6</td>
<td>455.4</td>
</tr>
<tr>
<td>Center Frequency ($f_c$)</td>
<td>MHz</td>
<td>405</td>
<td>405</td>
<td>405</td>
<td>405</td>
</tr>
<tr>
<td>Bandwidth ($BW$)</td>
<td>MHz</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>Average Tx Power ($P_T$)</td>
<td>dBm</td>
<td>-16</td>
<td>-16</td>
<td>-16</td>
<td>-16</td>
</tr>
<tr>
<td>Tx Antenna Gain ($G_T$)</td>
<td>dBi</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Path Loss Inside Body ($L_b$)</td>
<td>dB</td>
<td>34</td>
<td>34</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>Distance Outside Body ($d_1$)</td>
<td>m</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Path Loss @ $d_1$: $L_1 = 20\log_{10}(4\pi df_c/c)$</td>
<td>dB</td>
<td>34.15</td>
<td>34.15</td>
<td>34.15</td>
<td>34.15</td>
</tr>
<tr>
<td>Rx Antenna Gain ($G_R$)</td>
<td>dBi</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Rx Power: $P_R = P_T + G_T + G_R - L_1 - L_b$</td>
<td>dBm</td>
<td>-84.15</td>
<td>-84.15</td>
<td>-84.15</td>
<td>-84.15</td>
</tr>
<tr>
<td>Noise Floor: $N = -174 + 10\log_{10}(BW)$</td>
<td>dBm</td>
<td>-119.2</td>
<td>-119.2</td>
<td>-119.2</td>
<td>-119.2</td>
</tr>
<tr>
<td>RF Noise Figure ($N_F$)</td>
<td>dB</td>
<td>10.0</td>
<td>10.0</td>
<td>10.0</td>
<td>10.0</td>
</tr>
<tr>
<td>Average Noise Power: $P_N = N + N_F$</td>
<td>dBm</td>
<td>-109.2</td>
<td>-109.2</td>
<td>-109.2</td>
<td>-109.2</td>
</tr>
<tr>
<td>Minimum SNR ($S$) (PER = 10%)</td>
<td>dB</td>
<td>7.1</td>
<td>7.3</td>
<td>8.3</td>
<td>11.7</td>
</tr>
<tr>
<td>Implementation Loss ($I$)</td>
<td>dB</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Link Margin: $M = P_R - P_N - S - I$</td>
<td>dB</td>
<td>11.95</td>
<td>11.75</td>
<td>10.75</td>
<td>7.35</td>
</tr>
<tr>
<td>Minimum Sensitivity ($P_s$)</td>
<td>dBm</td>
<td>-98</td>
<td>-95</td>
<td>-92</td>
<td>-86</td>
</tr>
<tr>
<td>Maximum Allowed System $NF = M + N_F$</td>
<td>dB</td>
<td>21.95</td>
<td>21.75</td>
<td>20.75</td>
<td>17.35</td>
</tr>
</tbody>
</table>

*For the worst case (applying maximum distance and path loss inside body)

*Maximum allowed system NF for 900 MHz Zigbee application is 19 dB
3.4 Chapter Summary

In this chapter, we investigated the newly developed draft IEEE 802.15.6 PHY specification for narrow band WBAN applications. We focused on the PHY protocol which covers packet structure, modulation scheme, etc. Baseband signal processing schemes and modulation parameters were investigated in detail. System performance analysis with the ideal transceiver in AWGN channel was presented with the BER as the figure of merit. The derived link budget based on the performance analysis provides us with the groundwork of RF Front-end design.

In Section 3.1, we identified and listed up the requirements for WBAN applications. We focused on the physical layer (PHY) protocol for WBAN. The PHY protocol for WBAN covers packet structure, modulation, preamble, etc. We also provided overview of the signal flow and processing for the generation of packet service data unit (PSDU).

In Section 3.2, we provided detailed description for the WBAN signal generation in the baseband signal processor. The physical layer of this standard adopts simple and low-complexity channel coding schemes such as BCH, spreading, interleaving, scrambling. Each scheme for the coding and signal processing was detailed. One of the unique features for the WBAN standard is that the modulation parameters are variable depending on the data rate chosen. Rotated phase shift keying modulation scheme was investigated in depth. The effect of pulse shaping with SRRC was also investigated.

Section 3.3 provided performance analysis results through MATLAB simulation using BER as the figure of merit. We demonstrated that coherently detected rotated phase shift keying has the same BER as MPSK system. Ideal MICS band was implemented with MATLAB and simulated under AWGN channel. The overall performance was investigated and the resultant processing gain was provided as the PER requirement. Based on the performance analysis, we derived wireless link budget, which gives the groundwork of RF front-end architecture and low-power building block design.
Chapter 4:
Radio Transceiver Architectures

In this chapter, we investigate candidate RF front-end architectures for the development of MICS transceiver. Comparative study on the direct conversion architecture and low-IF architecture is performed. Based on our study, we propose to adopt direct conversion transmitter and low-IF receiver architecture for the MICS RF front-end. We also propose an asynchronous wake-up receiver architecture which is composed of carrier sensing circuit and serial code detector.

4.1 Challenges in Transceiver Design

The major design challenge associated with MICS transceivers is to extend their operation life time under limited energy sources while maintaining reliable operation under the interference of other signals. The data communication for implants is typically asymmetrical. The implants only need to receive simple commands to control their operation. This trait leads us to investigate the use of low-power transceiver in the MICS band. It is generally known that a significant portion of energy is dissipated in the transceiver of a wireless device. In order to achieve low-energy operation while meeting the interference-resilient performances in MICS transceiver, designers should consider the entire design flow from architecture down to circuit level.

Since the IEEE 802.15.6 standard employs differentially encoded PSK (DPSK) scheme for the physical layer, quadrature modulation is required for both the receive path and the transmit path in the RF transceiver. Direct conversion and super-heterodyne architectures have been commercially successful in modern wireless transceivers [26]-[28]. However, they inherently rely on the use of mixers, bandpass filters which require considerable power dissipation. In this perspective, direct voltage-controlled oscillator
(VCO) modulation technique could be considered as a candidate for MICS transmitter. However, direct VCO modulation transmitters typically incur frequency drift issue. Moreover, it does not meet the standard requirement because it basically operates on the frequency modulation scheme.

Reducing power consumption of the RF front-end in the idle duration is important. Duty cycling is one popular wake-up scheme [29]. The WBAN nodes sleep in an idle state most of the time while waking up at the predefined time to communicate with the host. This approach can reduce considerable amount of energy by exploiting the inherent low duty cycling characteristic of biomedical information. However, the low duty cycle results in increased latency in communication. Moreover, WBAN devices still wake up even if there is no data to transmit or receive, which results in redundant energy dissipation. In that sense, noble power management scheme in protocol or architecture level is required.

4.2 RF Front-End Architectures

4.2.1 Direct-VCO Modulation Architecture

Direct modulation means that the output frequency of the modulator is at the desired RF carrier frequency and no frequency conversion is required. Direct modulation architecture is generally applied for the constant envelope modulation scheme. In this context, the simplest approach for implementing a GFSK/GMSK modulator is to simply pass the data sequence through a Gaussian pulse shape filter and apply the filtered signal to the input of a VCO [30]. This approach is illustrated in Figure 4.1.

Despite the simplicity of this approach, it is not widely used in practice due to a major performance limitation, the center frequency instability [31]. Furthermore, the newly developed IEEE 802.15.6 draft standard incorporates phase modulation scheme. Hence, it is not optimal for the WBAN RF transceiver. However, direct modulation scheme can be applied to some restricted applications such as wake-up functionality. The
simple structure and low-power traits can be exploited to implement wake-up circuitry in the MICS band RF transceiver module as shown in Figure 4.2.

4.2.2 Direct-Conversion Architecture

Direct conversion (also called as “quadrature,” “homodyne,” or “zero-IF”) modulator is one of the most general architectures for wireless transceivers. This approach has enjoyed commercial success, and several semiconductor manufacturers offer integrate the RF front-end with the direct-conversion modulation and a baseband signal processors including DAC and filtering on a single IC [30]-[32]. As shown
In Figure 4.3, major components of the direct conversion front-end consist of a bandpass filter, an LNA (low noise amplifier), up/down mixers, a VCO (including a PLL), a power amplifier, and an RX/TX switch. The local oscillator is generated by a phase locked loop based frequency synthesizer for practical RF systems. The use of the PLL synthesizer is required to achieve the necessary center frequency accuracy, while maintaining the ability to change the output frequency.

While very general in nature, the direct conversion modulator approach has several notable drawbacks. The two RF mixers have stringent requirements on linearity to control adjacent channel interference. The gain and phase of the in phase (I) and quadrature (Q) signal paths must be tightly matched. Mismatch between I and Q paths as well as phase errors in the 90 degree phase splitter cause the envelope of the RF signal to experience fluctuations. When passed through a nonlinear amplifier, these envelope fluctuations cause spectral spreading. In addition to the spectral spreading, the phase function becomes distorted. Furthermore, to meet the required level of performance in the noted areas, the RF mixers and quadrature network consume moderate amounts of power [33].

Super heterodyne receivers will not be considered for MICS applications. They are not desirable from a low power perspective, because the power consumption of the frequency converter is larger compared to that of the modulator.

![Figure 4.3: A front-end of a Direct-Conversion Transmitter](image)
4.2.3 Low-IF Architecture

The Low-IF Receiver features a similar integrability as the zero-IF one but is less susceptible to the low-frequency interference. The desired channel is down-converted to a very low-frequency band around DC, typically ranging from a half to a few channel spacing. Unlike the zero-IF RX, the image is not the desired channel itself. The required image rejection is normally higher as the power of the image can be significantly larger than that of the desired channel [33]. As shown in the Figure 4.4, the Low-IF receiver performs the IF-to-BB (baseband) down-conversion digitally, eliminating the secondary image problem while permitting a pole-frequency-relaxed dc-offset cancellation adopted in the analog BB. The disadvantages are a higher bandwidth requirement compared with the zero-IF from the LPFs and PGAs, and a higher conversion rate required from the A/Ds. Furthermore, the Low-IF receiver is less sensitive to flicker noise and DC-offset at the expense of a higher image-rejection requirement [33].

Figure 4.4: Low-IF Receiver Block Diagram

4.3 Proposed Radio Architecture

4.3.1 Proposed Main Transceiver Front-End

The use of traditional superheterodyne architectures has started to fade out due to its high power and high cost. Those constraints are considered even worse especially for the ultra low power operations such as ZigBee and WBAN devices. The state-of-the-art
works typically adopt either low-IF or direct-conversion architecture for the low-power transceiver RF front-end. Recent literature has shown that most ZigBee devices adopt the low-IF receiver and direct-conversion transmitter architectures for their RF front-ends [33]. In that sense, we propose to adopt direct-conversion transmitter and low-IF receiver for the MICS applications.

Figure 4.5 is the proposed transceiver including baseband processor. Figure 4.6 is the block diagram of the transceiver RF front-end. Regardless of which architecture is used, quadrature mixing is generally required for most amplitude and phase/frequency modulated signals that have a quadrature component. In this receiver, the IF-to-Baseband down-conversion is performed digitally, eliminating the secondary image problem while permitting DC-offset cancellation adopted in the analog baseband. The transmitter uses direct-conversion architecture. As mentioned previously, the well-known LO pulling is one of major challenge for this architecture.

![Figure 4.5: Proposed Transceiver Architecture for MICS Applications](image-url)
4.3.2 Proposed Wake-up Receiver

4.3.2.1 Energy-Efficient Wake-Up Scheme

The use of an additional wake-up receiver renders an energy-efficient solution for the WBANs. However, an efficient combination of wake-up hardware and MAC protocol should be considered to maximize the advantages of the power management system. As shown in Figure 4.7, the DC interrupt signal is directly fed into the processor for post-
processing so that the processor has to handle addressing and identification, which results in additional power consumption. To address this issue, researchers proposed a unique protocol, which adopts a duty cycle scheduling and radio wake-up identification scheme [29],[34]. By applying duty cycle scheduling to the wake-up receiver, it is possible to shut-off the leakage current during the idling time. For the radio identification scheme, multiple wake-up stages or frequency selective resonant circuits could be used for the sake of adequate identification [29]. However, the approach increases hardware complexity and still involves a processor to control the wake-up procedure.

![Figure 4.7: Block Diagram of a Typical Wake-Up Receiver](image)

### 4.3.2.2 Proposed Wake-up Receiver

The proposed wake up receiver consists of a carrier detection circuit and a serial code detector, which decodes a message from the carrier pulses shown in Figure 4.8 [35]. An RF matching circuit and LC tank connected to the antenna can be capacitively tuned for channel selection or a single channel can be used by all of the nodes on a network for wake-up signals to simplify the design. To convert the AC signal to a detectable DC voltage, a Cockcroft-Walton Multiplier like the one in Figure 4.9 can be used [36]. This circuit uses diodes and capacitors to rectify and build a large DC charge on the output. The level of the output signal increases with a greater number of diode and capacitor stages. However, since this voltage can become high in the presence of powerful RF signals, an over-voltage protection circuit is needed to bleed off current when the voltage reaches a certain threshold. This also allows for the charge to dissipate when the carrier is no longer being received, allowing for pulses to be detected instead of maintaining a constant charge.
4.4 Chapter Summary

In this chapter, we investigated candidate RF front-end architectures for the MICS transceiver design. Based on our study, we propose to adopt direct conversion transmitter and low-IF receiver architecture for the main transceiver. We also propose a noble asynchronous wake-up receiver.

In Section 4.1, we discussed the design challenge and requirements associated with MICS transceiver design.

In Section 4.2, we investigated various RF front-end architectures including direct-VCO modulation, direct conversion, and low-IF architectures. Advantages and disadvantages for the candidate architectures were discussed.

In Section 4.3, we propose to adopt direct conversion transmitter and low-IF receiver architecture for the MICS RF front-end. We also propose an asynchronous wake-up receiver which is composed of carrier sensing circuit and serial code detector.
Chapter 5:
Low-Power RF Front-End Design

In this chapter, we investigate and present the design of low power RF Front-end building blocks including frequency source generation, receiver RF front-end, and transmitter RF front-end circuits as a ground work for a fully monolithic RF front-end. Two different quadrature voltage controlled oscillators (QVCOs) are investigated and their performance analyses are presented in detail. An RF receiver design is proposed and its circuit level details are described. An RF transmitter is also designed and its circuit level details are described. The performance of the designed RF Front-end is evaluated through simulations in TSMC 0.18µm RF CMOS process.

5.1 Frequency Source Generation

5.1.1 Our Approach

Power consumption is a major factor for implantable RF transceivers, since the lifetime of a battery-powered device is determined by its power consumption. The phase-locked loop (PLL) of a transceiver, specifically the voltage-controlled oscillator (VCO) and the quadrature signal generator, attributes large portion of the total power consumption. In order to minimize power consumption of a VCO, while maintaining good phase noise performance, some researchers incorporated off-chip inductors at the cost of a large form factor [37]. Therefore, it is necessary to find power efficient solutions at both circuit and architecture levels.

As a ground work for a fully monolithic RF front-end, we investigate ultra-low power quadrature VCOs targeting for implantable devices in WBAN applications. In this section, we survey quadrature signal generation methods focusing on frequency-division
and quadrature-coupling methods. We present implementations of the two quadrature signal generation techniques. They are based on the frequency division and the quadrature coupling methods. We provide simulation results and compare the performances of the designed QVCOs (quadrature VCOs).

5.1.2 Quadrature VCO Architectures

One of the most popular approaches to generate quadrature periodic signals is to use an oscillator operating at double the desired frequency followed by a divide-by-two frequency divider. This approach generally requires increased power consumption due to its higher operating frequencies. Moreover, this approach shows poor quadrature accuracy as it requires an accurate 50% duty cycle for the VCO core [38]. Quadrature-coupling is another popular approach. A quadrature-coupled QVCO usually comprises two anti-phase-coupled identical differential LC oscillators [39]. Hence, this approach still poses design challenge to reduce power consumption while exhibiting well known limitations such as phase noise and phase error.

5.1.2.1 RC-CR Network

The simplest quadrature approach is to shift the signal by ±45°, using an RC-CR network as shown in Figure 5.1 [38]. The drawback of an RC-CR network is that the amplitude of the quadrature output is equal only at one frequency \( \omega_0 = 1/(RC) \) and attenuates at different rates as the input frequency moves away from \( \omega_0 \). Moreover, the RC-CR network can only produce single-ended quadrature outputs. Narrowband operation can be addressed by adding buffer stages to the output, or by using a more complex passive network consisting of several RC-CR stages known as polyphase filter. Although these filters can provide bandwidth extension of 10% per added stage, the amount of thermal noise generated, as well as not being robust to process and temperature variation limit the performance. Moreover, they suffer from excessive power consumption required for buffering and cancellation of amplitude mismatches. Hence, we do not consider this RC-CR network configuration for the WBAN applications.
5.1.2.2 Frequency-Division

Another simple approach is to use an oscillator operating at double the target frequency and perform a frequency division using flip-flops. Figure 5.2 shows a block diagram of a divide-by-two frequency divider, which divides LO+ (and LO-) by two. Figure 5.3 is graphical illustration how the quadrature signals are generated by simple divide-by-two circuits. The configuration requires 50 percent duty cycle for the VCO core to generate an accurate quadrature signal. The conventional high-speed current-mode-logic (CML) is widely used for the implementation of the D flip-flops [38], and parallel current switching topology is also employed for some low supply voltage applications [40].

In general, the power consumption of a core VCO and a divide-by-two circuit is large at a high operating frequency, but relatively small for the MICS band of 400 MHz. In addition, the VCO operating at the double the frequency increases the quality factor Q of on-chip inductors and avoids pushing/pulling effects on the VCO owing to a much lower Power Amplifier (PA) frequency.

5.1.2.3 Quadrature-Coupling

A quadrature-coupled QVCO usually comprises of two identical anti-phase-coupled differential VCOs as shown in Figure 5.4. The combination of direct and cross (inverting) connections forces the two VCOs to oscillate in quadrature. Several coupling
schemes are possible for anti-phase injection between the two VCOs. A series coupling scheme is known to be robust to the phase noise and the I/Q phase error. However, the scheme reduces the headroom due to its cascode connection, which is a major hindrance for a low voltage operation and low power. A parallel coupling scheme addresses the problem, but does not allow bias current sharing of the two VCOs to increase the power dissipation [41]. Transformers can be used for the coupling [42], but it is less attractive for MICS applications due to large die size of on-chip transformers.

![Figure 5.2: Frequency Divider as Part of a Quadrature Generator](image)

![Figure 5.3: Quadrature Signal Generation Using Divide-by-Two Circuit](image)

![Figure 5.4: Directly Coupled Two VCOs](image)
5.1.2.4 Ring Oscillator

In principle, a ring oscillator and a quadrature-coupled QVCO can perform the same function and generate quadrature signals directly. However, ring oscillators are unsuitable for most modern transceivers due to high phase noise. Further, they consume large power, and hence, we rule out ring oscillators for MICS applications.

5.1.3 Low-Power Core VCO

In this section, we investigate current-reuse differential LC-VCO as the core VCO in preparation of fully monolithic QVCO design. We adopt a current-reuse differential LC-VCO as the core VCO due to its low-power consumption [43]. The current-reuse LC-VCO configuration uses a cross-coupled NMOS and PMOS pair as a negative conductance generator as shown in Figure 5.5(a). The VCO reduces power dissipation almost half compared with a conventional topology.

![Diagram of Current-Reuse VCO](image)

**Figure 5.5:** (a) Current-Reuse VCO (b) Proposed Current-Reuse VCO with Source Damping Resistors
5.1.3.1 Current-Reuse VCO with Damping Resistors

One of the drawbacks of the current-reuse VCO configuration is that the amplitude imbalance of the differential outputs is relatively larger than that of a conventional LC-VCO due to the asymmetric circuit structure, which inevitably aggravates I-Q mismatch problem in quadrature transceivers. To address the problem, Yun et al. added a passive damping resistor $R_s$ at the source of the NMOS transistor to balance the transconductance difference between PMOS and NMOS transistors [43].

The damping resistor controls the dc bias current, but does not degrade the Q of LC tank. Since the damping resistor is a source degeneration resistor, the overall transconductance of the transistor, $G_m$ is obtained as

$$G_m \approx \frac{g_m}{1 + g_m R_s} \quad (5.1)$$

where $g_m$ is the small signal transconductance of the NMOS transistor. Equation (5.1) implies that as $R_s$ increases, $G_m$ becomes a weaker function of $g_m$ and hence the drain current. Therefore, $R_s$ desensitizes the variation of the gain during the oscillation at the cost of lower effective $G_m$.

The damping resistor at the source node of NMOS reportedly improves the symmetry of the differential output waveforms [43]. However, the simulation result in Figure 5.6(a) shows that it does not always enable designers to achieve optimum design solutions due to the limited design parameters. In this example, the NMOS and PMOS are fairly well matched and are set at minimum device size for the low power operation. As shown in Figure 5.6(a), the damping resistor, $R_s$, no longer helps improve the imbalance problem of differential outputs because the VCO already operates in the current-limited regime.

In order to further enhance balanced differential outputs, we exploit two source damping resistors on both PMOS and NMOS transistors of a current-reuse VCO as shown in Figure 5.5(b). The two damping resistors control the DC current, which determines differential output waveforms. By carefully rationing the two damping resistors, symmetric differential output can be achieved. Figure 5.6(b) shows the
simulated phase difference and amplitude imbalance versus $R_{s2}$ ($R_{s1}$ is fixed at 10 Ω). Optimum values for $R_{s2}$ range from 5 Ω to 15 Ω while maintaining amplitude imbalance less than 2 % and phase difference less than 0.3°. The simulation results confirm that by using the damping resistors on both source nodes, the possibility of achieving matched transconductances is greatly enhanced.

Figure 5.6: Amplitude imbalance and phase difference for (a) current-reuse VCO (Versus $R_s$) (b) current-reuse VCO with source damping resistors (versus $R_{s2}$, $R_{s1} = 10$ Ω)
5.1.3.2 Low Phase Noise of Current-Reuse VCO

The current-reuse VCO topology inherently renders excellent phase noise performance. Hajimiri and Lee demonstrated that the phase noise of an oscillator is most susceptible when the waveform is in transition or zero-crossing and least susceptible when it is at the peak [44]. Figure 3 shows simulated dynamic drain voltage and current of a current-reuse VCO in Figure 1(a). Note that the current or energy injected into the tank of a current-reuse VCO is delivered all at once at the minimum noise sensitivity point. This is the desirable feature, since the maximum noise generation instant is aligned with the VCO’s minimum sensitivity point.

The use of damping resistors further enhances the phase noise performance of the current-reuse VCO. The $1/f^3$ corner of the phase noise is given by

$$\omega_{1/f^3} \approx \frac{K}{C_{ox}WL} \cdot \frac{g_m^2}{\gamma \cdot g_{d0}} \cdot \frac{1}{4kT} \cdot \left(\frac{c_0}{c_1}\right)^2$$ (5.2)

where $c_0$ and $c_1$ are the first and the second Fourier series coefficients of the impulse sensitivity function (ISF) respectively [44]. From the equation (5.2), it is clear that the $1/f^3$ corner is proportional to the square of the transconductance of the active device. From equations (5.1) and (5.2), it is expected that the $1/f^3$ corner will be reduced by desensitizing the overall transconductance $G_m$ using the damping resistors. Hence the current-reuse VCO with source damping resistors is inherently immune to the phase noise degradation.

![Figure 5.7: Dynamic Drain Voltage and Current of Current-Reuse VCO (@800 MHz)](image-url)
### 5.1.4 Parallel QVCO (P-QVCO) Design

#### 5.1.4.1 Proposed Parallel QVCO (P-QVCO) Architecture

We propose to implement a parallel coupled QVCO employing a current-reuse VCO as its core VCO [45]. Our P-QVCO shown in Figure 5.8 adopts a parallel coupling technique to combine two current-reuse VCOs. This approach delivers quadrature signals directly by realizing the anti-phase injection using the coupling transistors, MC1-MC4, in parallel with switching transistors, M1-M4. This coupling mechanism requires no additional voltage headroom, which enables operation at low supply voltages. The primary trade-off with this coupling scheme is that the coupling transistors form additional current paths, inevitably increasing the bias current of the QVCO. In order to reduce overall bias current consumption of the topology, current-reuse VCO with damping resistors is adopted as the core VCO for the QVCO.

![Schematic of Proposed Current-Reuse Parallel QVCO (P-QVCO)](image)

**Figure 5.8: Schematic of Proposed Current-Reuse Parallel QVCO (P-QVCO)**

The coupling strength $\alpha$ between the two VCOs of the conventional parallel-coupled QVCO can be defined as [46]:

$$\alpha = \frac{g_{\text{cpl}}}{g_{\text{sw}}} = \frac{W_{\text{cpl}}}{W_{\text{sw}}}$$  \hspace{1cm} (5.3)
where \( g_{cpl} \) and \( W_{cpl} \) are the transconductance and width of the coupling transistor, and \( g_{sw} \) and \( W_{sw} \) the transconductance and width of the switching transistor, respectively. It is known that the increase in \( \alpha \) degrades the phase noise while the phase error is reduced, or vice versa [46].

Figure 5.9 shows simulated phase noise and phase error versus coupling device size. The phase noise is degraded as the coupling device size increases. Meanwhile, the phase error is reduced up to a certain point, after which the phase error starts to increase as the coupling device size increases. The increased phase error for the large coupling devices is mainly due to the worsened amplitude imbalance in that regime. The imbalanced quadrature signals inevitably degrade both phase noise and phase error. In that sense, careful consideration should be given to the choice of such design parameters. The simulation results show that the minimum I/Q phase error is 1.2° when the NMOS coupling device has width of 6 µm with minimum length of 180 nm. The phase noise is as small as -125.7 dBc/Hz@100kHz with the device.

![Graph showing phase noise and phase error vs. coupling device width](image)

**Figure 5.9: Phase Noise (@100 kHz) and Phase Error for the Current-Reuse P-QVCO**

### 5.1.4.2 Implementation of the P-QVCO

The proposed current-reuse P-QVCO has been implemented using TSMC 180 nm RF CMOS technology. To reduce the current drawn by the oscillator, an inductor with
high inductance and high Q, should be used. Built-in inductors with L=16.8 nH and Q=6.7 (rather than a customized one) have been adopted to minimize the tank loss at the MICS frequency and MOS varactors are used for a fine tuning of the oscillation frequency. The damping resistors for the current-reuse VCO have the value of 10 Ω respectively. Since the low power consumption is our primary goal, minimum size coupling transistors are used at the expense of phase error in order to minimize additional bias current flowing through the coupling transistors.

5.1.4.3 Performance Evaluation of the Designed P-QVCO

The designed P-QVCO exhibits fairly balanced output waveforms with the amplitude error of 1.4 %. The current consumption of the QVCO is 2.6 mA. Low Q of the on-chip inductors requires large transistor size for the P-QVCO to consume large amount of power. Figure 5.10 shows the generated quadrature signal waveforms of the P-QVCO. Figure 5.11 shows the output phase noise performance for the presented P-QVCO. The simulated values are -126 dBc/Hz and -130 dBc/Hz at 100 kHz and 1MHz offset respectively. The overall phase noise exhibits excellent performance. The Figure-of-Merit (FoM), which is widely used to compare VCO performance, is expressed as below [43]:

$$FOM = L(f_o) + 10\log\left(\frac{P_{DC}}{f_o}\right)^2$$

(5.4)

where \(L(f_o)\) denotes the phase noise at the offset frequency \(f_o\) and \(P_{DC}\) power dissipation. \(f_o\) the oscillating frequency. The FoM of the design was evaluated as -187, which is quite excellent compared with other works. Table 5.1 lists summary of the performances of the presented P-QVCO along with the comparison with those of previously published ones.
Figure 5.10: Output Waveforms of the P-QVCO

Figure 5.11: Phase Noise Performance of the Current-Reuse P-QVCO

Table 5.1: Performance Summary of the Designed P-QVCO

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<td>1.0</td>
</tr>
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<td>-162</td>
<td>-179</td>
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5.1.5 Divide-by-Two QVCO (D-QVCO) Design

5.1.5.1 D-QVCO Architecture and Implementation

A current-reuse VCO running at twice the target frequency and a divide-by-two circuit are implemented as a two-stage structure as shown in Figure 5.12 [48]. The first stage is a VCO operating at 800MHz, and the second stage is a frequency divider which divides the frequency from the VCO by half and thereby generates quadrature signals.

A VCO with two damping resistors of $10 \, \Omega$ each oscillates at 800 MHz. A built-in inductor with $L=16.8 \, \text{nH}$ and $Q=6.7$ (rather than a customized one) has been used to minimize the tank loss at the frequency and MOS varactors are used for a fine tuning of the oscillation frequency.

![Figure 5.12: D-QVCO Architecture](image)

5.1.5.2 Parallel Constant Current Switching Divider

For the divide-by-two, a master-slave configuration of two source-coupled-logic (SCL) latches is commonly used. However, in order to aggressively scale down the supply voltage, we need to use a low-voltage, low-power and high-speed frequency divider. For our work, we adopted parallel constant current switching topology which is suitable for a low supply voltage [40]. By integrating parallel current switching topology with constant tail current, it can be operated at the low supply voltage compared to the conventional current-mode logic (CML). Figure 5.13 shows a simplified schematic diagram, in which the folding topology increases the headroom and the current sources
M4 and M5 boost the gain to enable small bias currents. All the transistors of the divider circuits are minimized to reduce the power consumption. The folding topology combined with the tail current allows the divider to operate at the lower supply voltage compared to conventional dividers based on current-mode logic.

![Parallel Constant Current Mirror Switching Divider (only Latch1 shown)](image)

Figure 5.13: Parallel Constant Current Mirror Switching Divider (only Latch1 shown)

### 5.1.5.3 Performance Evaluation of the Designed D-QVCO

We simulated the D-QVCO implemented using TSMC 180 nm RF CMOS technology. Figure 5.14 shows the generated quadrature signal waveforms of the D-QVCO. D-QVCO has more balanced output waveforms than those of P-QVCO due to the saturated operation of the divider circuit. The total bias current of the D-QVCO is 230 µA (47 µA for the divider). The D-QVCO consumes about four times less power than the P-QVCO. On-chip inductors exhibit low Q at the MICS band, which requires larger transistor size for the P-QVCO to consume more power.

Figure 5.15 shows the output phase noise performance for the presented D-QVCO. The simulated values for the D-QVCO are -129 dBc/Hz at 1MHz offset. At the higher offset frequency, the D-QVCO has poor phase noise performance, since the frequency
dividers degrade the phase noise in the region. However, as expected, the overall phase noise performance is excellent for the D-QVCO. The Figure-of-Merit (FoM) was calculated as -185.

![Output Waveforms of the D-QVCO](image)

**Figure 5.14: Output Waveforms of the D-QVCO**

![Phase Noise Performance](image)

**Figure 5.15: Phase Noise Performance of the Current-Reuse D-QVCO**
5.2 Receiver Front-End

5.2.1 Our Approach

Low-noise amplifiers (LNAs) and down-conversion mixers are the first (and/or second) circuits in the receiver path. The well known Friis equation (5.8) indicates that overall system noise figure tends to be dominated by the noise performance of the first couple of stages in a receiver [49],[50]. Traditionally, lots of efforts have been given to minimize the noise figure (NF) contribution of the first few stages, especially of the LNAs [51]-[56].

\[
NF_{tot} = 1 + (NF_1^2 - 1) + \frac{NF_2^2 - 1}{A_{p1}} + \cdots + \frac{NF_m^2 - 1}{A_{p1}\cdots A_{p(m-1)}}
\]  

(5.5)

where \( NF_m \) and \( A_m \) are noise factor and power gain of \( m^{th} \) stage respectively.

For the RF receiver front-end configuration, cascaded LNA and mixer is conventionally adopted due to its good noise figure (NF) performance. However, its high power consumption is a significant obstacle to satisfying specifications of low power applications such as MICS applications. Considering that the key design challenge for MICS devices is to minimize the power consumption of the RF circuitry, we need to come up with a noble RF front-end topology.

Many researchers thus far have investigated low power circuit techniques for the LNA and mixer design [57]-[60]. Merged LNA and mixer structures have been exploited to reduce power consumption in wireless transceivers by stacking LNA and mixer blocks, thus reusing the bias currents [57],[58]. Folded structure is another possible way for the realization of merged LNA and mixer [59],[60]. In addition, gm-boosting and sub-threshold operation techniques are also used [59],[61].

In order to realize low-power receiver RF front-end, we investigate stacking of an LNA and a down-mixer for MICS applications. The main idea for the low-power RF front-end design is to operate the LNA in the saturation region, while the mixer in sub-threshold region. In addition, gm-boosting technique is exploited using capacitors cross-
coupling at the LNA input stage. Combining these low-power techniques, we can achieve low noise figure (NF) and high linearity, which is critical for the overall performance of the RF receiver front-end.

5.2.2 Sub-Threshold RF Circuits

Sub-threshold biasing technique has been widely adopted in digital, analog, and even RF circuits [61],[63]. The main advantage for the sub-threshold operation lies in the significant power saving. The drain current in the weak inversion region of MOSFET is given as:

\[ i_D = \frac{W}{L} I_{DO} \exp \left( \frac{V_{GS}}{n \left( \frac{kT}{q} \right)} \right) \]  

(5.6)

where \( I_{DO} \) is a process-dependent factor, \( n \) is the sub-threshold slope factor, \( k \) is Boltzman constant, \( T \) is temperature (K), and \( q \) is the charge of an electron. Since the gate-source voltage \( V_{GS} \) in (5.6) is smaller than the threshold voltage of MOSFET, sub-threshold circuits generally require low voltage headroom so that they are favorable for stacked circuits such as merged LNA and mixer under a low supply voltage.

Meanwhile, the sub-threshold circuits pose critical design challenges. First, the transconductance \( g_m \) is notably small in the sub-threshold region compared to that of the strong inversion region. The small \( g_m \) can cause degraded noise performance for the LNA. Moreover, the gate-induced noise of the MOSFET is dominant under the sub-threshold operation. For those reasons, sub-threshold operation may not be beneficial for the input stage of the LNA. Secondly, the transition frequency \( f_t \) in the weak inversion region is much lower than that of the strong inversion region [61]. However, that does not matter for our target applications since the MICS band is allocated in the relatively low frequency (400 MHz).
5.2.3 Proposed Merged LNA and Mixer

The merged LNA and mixer configuration has been recently proposed for the sub-mW receivers. It can reduce power consumption effectively by sharing the DC current path flowing into both the LNA and the mixer [59],[60]. In order to meet our design specifications for the front-end circuits, we investigate a merged LNA and mixer scheme as a candidate.

The circuit schematic of the proposed merged LNA and Mixer is shown in Figure 5.16, where the transistor M1 and M2 consist of cross-coupled gm-boosting common gate input stage achieving better noise performance with lower power consumption [64]. The transistors M3 to M10 act as the switching pairs for the double-balanced mixer to convert the output current of the RF stage to IF band. The front-end circuit is designed to support a Low-IF (intermediate frequency) receiver. The Low-IF down-conversion avoids the flicker noise and DC offset associated with a direct-conversion. It contributes reliability, and incorporates a simple filter design followed by the LNA and mixer. The proposed merged LNA and mixer are explained in more detail in the subsequent sections.

Figure 5.16: Schematic of the Proposed Merged LNA and Mixer
5.2.3.1 Low Noise Amplifier (LNA) Design

As the LNA is the first circuitry of the receiver, the main considerations for the LNA design are enumerated as the low noise figure, input matching, and high gain. The common-gate amplifier offers superior input matching. In Figure 5.17, transistors M1 and M2 realize a common-gate (CG) LNA. The main advantage of a CG amplifier is a simple input matching to 50 $\Omega$ with $1/g_m$ method [62]. However a strong disadvantage is the higher noise figure. The common-gate stage has a minimum noise factor given by [62]:

$$F = 1 + \frac{\gamma g_{d0}}{g_m^2 R_s}$$  \hspace{1cm} (5.7)

Where the noise performance can be optimized by increasing the $g_m$, however it degrades the input matching. Since the trade-off relation between the input matching and noise figure characteristics incurs contradiction, some remedy to the CG configuration is required.

![Figure 5.17: (a) gm-boosted CG LNA topology, and (b) gm-boosted CG LNA implemented with capacitors cross-coupled](image)

In this work, the capacitor cross-coupled method with $C_{C1,2}$ is adopted as a gm-boosting scheme to solve the contradiction [59],[62], as shown in Figure 5.17. The capacitor between gate and source provides an inverting gain $A$, and decouples the link
between the input matching and the noise performance. As consequence, the $R_{\text{in}}$ and noise factor, $F$, of the CG amplifier can be calculated as:

$$R_{\text{in}} = \frac{1}{g_m(1+A)} \quad (5.8)$$

and

$$F = 1 + \frac{\gamma g_{d0}}{(1+A)^2 g_m^2 R_s} \quad (5.9)$$

where $g_{d0}$ and $\gamma$ are empirical process- and bias-dependent parameters [62]. As can be seen in the equations (5.8) and (5.9), choosing a proper value of $C_{C1,2}$, which determines gain $A$, enhances the noise performance while maintaining input matching.

### 5.2.3.2 Down-Conversion Mixer Design

To support quadrature modulation, two double-balanced mixers are implemented and stacked on top of the LNA as shown in Figure 5.16. Transistors M3 to M10 act as switching pairs in combination with LO signals, and produce in-phase (I) and quadrature-phase (Q) signals of IF signals. The RC tank loads at the mixer output constitute lowpass filters so that the high order harmonics will be filtered out.

The merged LNA and mixer does not require an intermediate matching network, thus saves chip area and cost. Furthermore, the reused bias currents from LNA to Mixer save DC power consumption. In this design, fully differential structure is adopted since it contributes the noise performance by suppressing the common-mode noise. The mixer operates in the sub-threshold region while the LNA stage operates in the strong inversion region. The noise performance of the LNA is not degraded, and the output swing of the mixer has enough margins even though with a low supply voltage of 1.2 V. As addressed previously, transistors in the weak inversion region have lower $f_t$ comparing to that in strong inversion region.
5.2.4 Performance Evaluation

The merged LNA and Mixer is designed and simulated using TSMC 180nm RF CMOS technology. The overall circuit consumes 1.84 mW under a supply voltage of 1.2 V. Thanks to the gm-boosting strategy, the noise figure is measured as low as 3.6 dB over the IF frequencies up to 50 MHz except DC point as shown in Figure 5.18.

The conversion gain is shown in Figure 5.19. The maximum gain of 21.6 dB is obtained at 404 MHz with a fixed IF frequency of 1 MHz. S11 is less than -25 dB through the entire MICS band shown in Figure 5.20, which means the sub-threshold operation of switching transistors does not degrade the input matching.

To analyze linearity performance, the two-tone test is held. P1dB is obtained at the input power of -19.214 dBm while an input RF power is given between -85 dBm to -50 dBm. IIP3 is measured at the input power of -6.8 dBm shown in Figure 5.21.

The performance of this proposed circuit is summarized and compared with other works in Table 5.2. All of the works have merged LNA and mixer topologies. The NF of [58] is comparable with that of ours. However, the power consumption of the work is unacceptably high for the MICS applications. As can be seen in the table, our work represents excellent NF performance, input matching, and super low power consumption while using only two inductors.

![Figure 5.18: Noise Figure vs. IF Frequencies](image-url)
Figure 5.19: Conversion Gain vs. Operating Frequencies

Figure 5.20: S11 vs. Operating Frequencies
Table 5.2: Performance Summary of the Designed Merged LNA and Mixer

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5.3 Transmitter Front-End

5.3.1 Our Approach

The RF front-end of the transmitter mainly consists of a power amplifier (PA) and an up-conversion mixer. Figure 5.22 shows block diagram of the designed RF front-end. The goal is to develop an I/Q architecture that is capable of functioning using PSK modulation and capable of sending data at 187.5 kbps. The desired supply voltage is as low as 1.2 V, and this system should be able to deliver a power output of -16dBm (25 μW). The power amplifier must be designed to drive a 50 Ω antenna load. Since the output power is relatively small compared to the conventional ones, herein we call it as a drive amplifier (DA). Most importantly, the power consumption of the device should be as low as possible. Our main goal for this design is that the combined power consumption of the DA and the mixer should be less than 1mW. For the mixer and DA design, minimum number of inductors should be used to save the die cost.

Figure 5.22: Block Diagram for the Transmitter RF Front-end
5.3.2 Proposed DA and Mixer Design

5.3.2.1 Driver Amplifier (DA) Design

Figure 5.23 is the proposed differential Driver Amplifier (DA) which has cascode transistors to minimize Miller effect and enhance the input/output isolations. The proposed differential DA uses PMOS devices in order to share the inductors with the LNA in the receiver path. The inductor sharing scheme will be elaborated in the following section. In the receiver mode, the switch is connected to Vdd so that the output impedance is at high for the LNA input matching. An advantage of this topology is that the two inductors seen in Figure 5.23 are actually shared between both the LNA and the DA. This allows for high Q inductors to be used while requiring only two inductors for the entire RF front-end. In addition, it does not require the use of a discrete RF switch for the connection to the antenna, as this functionality is built into the individual components.

Figure 5.23: Proposed Driver Amplifier (DA) Topology
### 5.3.2.2 Up-Conversion Mixer Design

The proposed up-conversion mixer is shown in Figure 5.24. First and foremost, it has very low power consumption compared to the other topologies. In addition, it was designed with a resistive load. This is important to us since we can reduce the number of inductors. Further, it is unique in that it does not require a specific current source as is required by many other designs. This enables the topology to have only two series transistors between $V_{DD}$ and GND, allowing for excellent performance under a low supply voltage. This design uses two mixers in parallel, while both share the same resistive load. This is possible because the output of a Gilbert cell is a current, and these currents are able to add directly. The $R_D$ resistor then converts the added currents to a voltage that can be applied to the DA. This proposed circuit requires three bias voltages to establish the bias conditions. All the input signals are capacitively coupled to the gates of the transistors.

![Proposed Up-Conversion Mixer](image)

**Figure 5.24: Proposed Up-Conversion Mixer**
5.3.3 Direct Antenna Matching

As shown in Figure 5.25, the L-C tank is used for 50 Ω impedance matching at the input of the LNA and reused for the load impedance to drive antenna at the output of the DA. The capacitor array is implemented for the tuning purpose to control its resonant frequency.

![Figure 5.25: Direct Antenna Matching of LNA and DA](image)

5.3.4 Performance Evaluation

The proposed driver amplifier and up-conversion mixer was implemented in TSMC 0.18µm RF CMOS process and simulated with Cadence design tools. The overall circuit consumes 725 µW for DA under a supply voltage of 1.2 V.

Up-conversion mixer conversion gain was simulated with a purely resistive load of 20 kΩ. However, the actual value will be lower as the capacitive load of the DA heavily loads down the output of the mixer. Figure 5.26 shows conversion gain as a function of LO input (V_{LO}). The mixer is currently operating with a V_{LO} of 200mV peak-
to-peak, corresponding to 100mV on the graph. Note that in the region around 100mV, the curve is quite linear. An increase in $V_{LO}$ would increase the conversion gain. However a large increase would negatively affect the linearity of the system.

Figure 5.26: Mixer Conversion Gain vs. LO

Figure 5.27: DA Output Power vs. Input Power
Figure 5.27 shows output power as a function of available input power. At an output power of -16dBm, the output power is linearly dependent on the input power, implying that an increase of input voltage would cause a proportional increase in the output voltage. The graph also shows that regardless of input power, the output power saturates at roughly -4dBm.

The output reflection coefficient, S22, was plotted to better understand the operation of the circuit and the effect of the antenna as shown in Figure 5.28. In the range of 400 MHz frequency, the DA had an S22 of under -5dB. As a result of the L-match, and the frequency selection associated with an L-match, note that there is a large dip in the magnitude of S22 at our operating frequency, which means matching is achieved.

The IIP3 of the mixer is characterized in Figure 5.29. The first order frequency used was 403.251MHz, and the third order frequency used was 403.249MHZ. The IIP3 was found to be around 4.5dBm. The result shows good linearity for our mixer, as the available input power to our mixer as the simulation was defined is -10dBm, meaning that we are operating 14.5dBm below the IIP3 point. Figure 5.30 shows the IIP3 of the overall system. The 1st order and 3rd order frequency are the same as the IIP3 of the mixer (403.251MHz and 403.249MHz respectively). The overall system has an IIP3 found to be -1.59dBm. This gives a margin of 8.41 dBm.
In addition to the shown measurements, the DA was also measured in a standalone test. The OIP3, which is a more logical measurement for a power amplifier, was found to be 6.46 dBm. Because this device operates at -16 dBm, there is over 20 dBm of headroom at the operating point of the DA. This indicates very good linearity.

Figure 5.29: Illustration of IIP3 of the Mixer

Figure 5.30: Illustration of IIP3 of the Transmitter RF Front-end
5.4 Chapter Summary

In this chapter, we presented our work on developing low-power and low-cost building blocks for an RF transceiver front-end such as frequency source generation, receiver front-end, and transmitter front-end in Sections 5.1, 5.2, and 5.4, respectively. All the building blocks were implemented in TSMC 0.18 µm RF CMOS process. Performance of the designed RF front-end was evaluated by simulation in circuit level.

In Section 5.1, we investigated and presented ultra-low power quadrature VCOs targeting for implantable devices in WBAN applications. We presented implementations of the two quadrature signal generation techniques. They are based on the frequency division and the quadrature coupling methods. Both the QVCOs are designed based on the newly proposed current-reuse VCO with two damping resistors. We provided simulation results and compared the performances of the two designed QVCOs.

In Section 5.2, we presented the implementation of the proposed low-power receiver RF front-end. By stacking LNA and down-conversion mixer, we can come up with low supply and low power RF front-end. Various low power circuit techniques such as gm-boosting and sub-threshold operation were also exploited. Performance analysis was given and it turns out that the designed receiver RF front-end achieves low noise figure and high linearity while meeting the overall performance requirements.

Section 5.3 provided illustration of circuit topologies and performance analysis of the proposed driver amplifier (DA) and up-conversion mixer. The proposed DA uses cascaded PMOS transistors to minimize Miller effect and enhance the input/output isolations. The up-conversion mixer is based on the Gilbert cell implemented with resistive loads. Meanwhile, a direct antenna matching scheme was proposed to share the inductor loads with the receiver path.
Chapter 6:
Case Study: Super-Regenerative Transceiver

In this chapter, we present a transceiver architecture targeted for MICS applications. The proposed transmitter realizes direct VCO modulation incorporating a dual spiral antenna as an inductor element. We propose to adopt super-regenerative receiver architecture based on the frequency modulation scheme. For the realization of fully on-chip transceiver implementation, we present several low-power building blocks such as digitally-controlled oscillator and quench signal generator.

6.1 Consideration of Modulation Schemes

The RF front-end is the major source of power dissipation for many wireless devices. When a modulated signal with significant amplitude variations such as QPSK or QAM is applied to a transmitter, specifically to a power amplifier exhibiting nonlinearities, two signal degradations occur. The first effect is the signal distortion, which causes degraded reception by the intended receiver. The second one is an increase in spurious transmit energy in adjacent channels. This effect, known as spectral re-growth, plays a prime role in determining the required amplifier’s linearity [49],[50].

A modulation type with less amplitude variations increases the efficiency of a power amplifier causing longer battery life. One popular approach to minimize nonlinear effects is to adopt constant envelope modulation schemes. Gaussian frequency shift keying (GFSK) and Gaussian minimum shift keying (GMSK) are widely adopted for such a system as European cordless telephone (DECT) standard and the European Global
System for Mobile Communications (GSM) system [33]. They are appraised to be immune to nonlinear distortion effects.

### 6.1.1 Classes of Modulation

Modulation types can be classified generally as either linear modulation or nonlinear modulation [23]. For example, pulse amplitude modulation (PAM) is linear due to the linear relationship between the data symbols and the transmitted signals. When analyzing narrowband signals, it is often convenient to represent the signal as:

\[ s(t) = \text{Re}\{s_{ce}(t)e^{j\omega_c t}\} \]  

(6.1)

The signal \( s_{ce}(t) \) is known as the complex envelope of the signal and \( \omega_c \) is the center frequency of the carrier. For PAM, the complex envelope is given as:

\[ s_{ce}(t) = \sum_k a_k p(t - kT) \]  

(6.2)

The sequence of data symbols is given by \( a_k \) and \( p(t) \) is the impulse response of a linear time-invariant pulse shaping filter. When the impulse response \( p(t) \) is a smooth function, the envelope of the RF output signal, \( |s_{ce}(t)| \), varies with time. Examples of linear modulations are QPSK and QAM [23].

Phase and frequency modulations are nonlinear because the output signal does not depend on the modulating signal in a linear fashion. One advantage of this type of modulations is that the envelope can be made inherently constant. The complex envelope for a constant envelope signal is given as:

\[ s_{ce}(t) = e^{j\psi(t)} \]  

(6.3)

The phase function, \( \psi(t) \), is commonly generated by filtering the data sequence, \( a_k \), with a linear time-invariant filter with impulse response, \( p(t) \).

\[ \psi(t) = \sum_k a_k p(t - kT) \]  

(6.4)
6.1.2 GFSK and GMSK

The class of modulations given by (6.13) and (6.14) include two popular and closely related modulation types which are Gaussian Frequency Shift Keying (GFSK) and Gaussian Minimum Shift keying (GMSK). GFSK and GMSK are modified versions of FSK and MSK using the pulse shaping filter which is given by:

\[ p_{GMSK}(t) = rect_T(t) \ast g(t) \] (6.5)

where \( rect_T(t) \) is a rectangular pulse of duration \( T \), and \( g(t) \) is a Gaussian pulse. The difference between MSK and FSK is that MSK requires a modulation index of precisely 0.5, while FSK can work with different modulation indices. FSK is a constant envelope form of digital modulation and can be implemented easily by directly modulating the instantaneous frequency of an oscillator:

\[ f_i(t) = f_c + \Delta F \times m(t) \] (6.6)

where \( f_c \) is the carrier frequency, \( \Delta F \) is the frequency deviation constant, and \( m(t) \) \([-1, 1]\) is the digital modulating signal. For a bit rate \( R \), setting \( \Delta F = 0.25R \) results in Minimum Shift Keying (MSK). MSK is the most spectrally efficient form of FSK that still produces orthogonal signaling and can be demodulated coherently [23]. This relaxes SNR requirements in the base station receiver, reducing output power requirements on the implanted transmitter. Theoretically, MSK can be used at a bit rate of 200 kb/s without any pre-filtering and meet the MICS spectral mask since its first nulls occur at \( f_c \pm 0.75R = f_c \pm 150R \) and subsequent peaks are at least 25 dB below the main lobe [65].

6.2 Transceiver Architecture

In the previous Chapter, we investigated several possible architectures for an MICS transceiver. We should consider two unique features mentioned in Chapter 2 to choose an optimal architecture as well as technical requirements of an MICS transceiver. The first feature is that the human body is an excellent temperature regulator. The second one is that the standards and regulations relax frequency stability and output power for
MICS applications [65]. Together with those features, the demand for longer battery life and small form factor should be also taken into account, since implant devices are supposed to last for years without battery recharges or replacements. Furthermore, while it is critical for the implant to consume minimal power, the corresponding control node is free to consume much more power. WBAN is likely to operate in the simple star topology network, so that the center control nodes can absorb hardware complexity from the implant nodes.

With these observations in mind, we propose to adopt a direct modulation transceiver for the implant device. The direct-modulation architecture is preferable as a constant-envelope system, because it consumes much smaller power and die area than the homodyne architecture with complicated up-conversion mixers. For that reason, researchers thus far have investigated and implemented low power MICS RF transceiver which adopted constant envelope modulation scheme [66]-[68]. Both direct VCO modulation and PLL-based loop control could be candidate techniques to implement direct modulators. Among the two candidates, direct VCO modulation technique has much simpler architecture than the PLL-based counterpart, which inevitably results in complicated implementation and possibly requires external components for reference frequency generation. The relaxed technical requirements for an MICS transceiver are sufficient to offset inferior frequency stability of a direct VCO modulator.

The direct VCO modulation scheme ushers us to a simple, low-power topology as shown in Figure 6.1. The proposed block diagram for an implant transceiver has a digitally-controlled oscillator (DCO), which is directly modulated with FSK. Digital signals from the baseband processor are used to tune the DCO. Relaxed output power requirement (-16 dBm EIRP) leads us to incorporate a dual spiral antenna as an inductive tank load, which eliminates a power amplifier. An antenna directly connected to the DCO without any buffer causes some problems such as oscillator pulling and mismatch and it will be discussed later. Further, it cannot adopt the homodyne or super-heterodyne topologies, since they are not able to detect the super-regenerated signal from the DCO. Hence, our transceiver adopts a super-regenerative architecture, which is widely used for ultra-low power applications. One shortcoming of a super-regenerative receiver is sensitive to the noise injection and poor selectivity performance [8],[11],[69].
6.2.1 Transmitter Architecture

A simple FSK transmitter comprising a DCO and dual spiral antenna as an inductive load is shown in Figure 6.2. The DCO is modulated directly with the data sent from the baseband processor. An equivalent circuit for the antenna can be simplified as a parallel R-L tank, and the resonant tank frequency is given as:

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

(6.7)
Frequency tuning and modulation are performed by controlling the capacitance, which consists of an array of a capacitor bank. A design challenge is that it requires a large number of bits to tune a wide frequency range while achieving small frequency steps. Furthermore, a conventional implementation of capacitor arrays requires a large number of small capacitors, which may be impractical. For example, it requires 9 bits to tune the entire range (which is 402~405 MHz) of the MICS band with the frequency tuning step of 10 kHz as summarized in Table 6.1. In the case, the minimum step size of the capacitor should be less than 0.187 fF. Since it is impractical to realize such a small capacitor with conventional CMOS technologies, a certain level of scheme should be devised to achieve the small step sizes with practical capacitor values.

Table 6.1: Tuning Capacitor Bank Specifications Example for MICS Application

<table>
<thead>
<tr>
<th>Operating freq.</th>
<th>Inductance</th>
<th>Capacitance tune range</th>
</tr>
</thead>
<tbody>
<tr>
<td>402 ~ 405 MHz</td>
<td>23 nH, Q = 7.1</td>
<td>$C = \frac{1}{(2\pi f_o)^2 L} \approx 6.435 \text{ pF} \sim 6.531 \text{ pF}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Resolution</th>
<th>Required frequency step</th>
<th>Minimum capacitor step size</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 kHz</td>
<td>$M = \frac{3\text{MHz}}{10\text{kHz}} = 300 \text{ (9 bits)}$</td>
<td>0.187 fF</td>
</tr>
</tbody>
</table>

**6.2.2 Receiver Architecture**

As noted earlier, our transceiver adopts a super-regenerative receiver (SRR). The extraordinary high gain and simplicity of the super-regeneration leads to low-power consumption and small circuit area. Further, a SRR allows a direct connection between the antenna and the oscillator.
6.2.2.1 Theory of Super-Regeneration

Super-regenerative receiver has been explored in long history for low-power applications. However, the theory has not been understood well so that it is worth revisiting the operational principle and mechanism of super-generation. The basic idea behind super-regeneration is graphically illustrated in Figure 6.3. Super-regeneration is based on the startup of an oscillator. Two identical oscillators in the Figure 6.3 are powered up and down under the control of the same quench signal. The top example in the Figure 6.3 (a) shows the start-up of a standalone oscillator. The oscillation envelope (i.e., the peak-to-peak amplitude) grows and decays with the quench signal. The middle example in the Figure 6.3 (b) shows a case with the injection of an external signal (such as a signal received by an antenna) into the oscillator causing the oscillation to start up much earlier [70]. Since the difference in startup time depends on the strength of the injected signal, the oscillator can be used as a detector. However, once the oscillation saturates, we have to disable the oscillation to cause the startup again.

![Figure 6.3: Envelope of Oscillation without (a) and with (b) an Injected Signal](image-url)
Super-regeneration can be understood using a parallel resonant tank, which forms the core of a resonant oscillator, as shown in Figure 6.4. The resonant tank consists of an inductor $L$, a capacitor $C$, and a shunt conductance $G_+ - G_-$. Here, $G_+$ represents the parasitic loss of the resonant circuit while $G_-$ represents the negative conductance provided by active devices [70]. The active devices compensate the loss of the tank, and the overall conductance, $G = G_+ - G_-$, can be either positive or negative depending on the energy supplied by the active devices. An injected input signal is modeled by a sinusoidal current source $A \sin(\omega t)$.

![Figure 6.4: Parallel Resonant Circuit Representing an Oscillator](image)

Summing the currents in Figure 6.4, we have

$$C \frac{dV}{dt} + GV + \frac{1}{L} \int V dt = A \sin(\omega t) \quad (6.8)$$

Solving for $V$, the complete solution of the voltage across the tank can be written as:

$$V = e^{-\alpha t} \left( k_1 e^{j \omega_d t} + k_2 e^{-j \omega_d t} \right) + \frac{A \sin(\omega t + \phi)}{\sqrt{G^2 + (\omega C - 1/\omega L)^2}} \quad (6.9)$$

where the damping factor, $\alpha = G/2C$, is directly proportional to the conductance $G$ and the damping frequency as below.

$$\omega_d = \sqrt{\left(1/\omega L C\right) - \left(G/2C\right)^2} = \sqrt{\omega_0^2 - \alpha^2} \quad (6.10)$$
The first term in (6.11) is a transient oscillation at frequency $\omega_d$ with the damping factor $\alpha$, representing the free response, and it does not depend on the injected signal [70]. If $G$ is positive, the active devices do not provide enough energy to compensate all the loss in the tank, so that the free oscillation dies out and only the second term, which represents the forced response to the injected signal, remains. On the other hand, if $G$ is negative, the active devices provide more energy than is dissipated in the resonant circuit, building up a free oscillation from an initial voltage. This case is termed super-regeneration.

In order to detect the injected signal, we first make the conductance $G$ positive, letting the free oscillation die out, and then change the conductance from positive to negative. Thus, the initial voltage, at the moment that the total conductance turns negative, is solely determined by the forced response (i.e., the second term of (6.11)). Once a free oscillation starts, the oscillation amplitude tends to grow regardless of the injected signal, and therefore to amplify and detect any subsequent input samples, it is necessary to reset any oscillation by periodically alternating the total conductance from negative to positive [70]. Since an LC tank always has a certain positive conductance due to loss (i.e., $G+$), we only have to control the negative conductance $G-$ to vary the sign and value of the overall conductance. The value of the negative conductance is controlled by the quench signal. The rate at which we alternate the total conductance is called the quench frequency.

### 6.2.2.2 Proposed Super-Regenerative Receiver

Figure 6.5 shows the block diagram of the proposed super-regenerative receiver (SRR). The proposed SRR incorporates an optional low-noise amplifier (LNA), a digitally controlled oscillator (DCO) which is shared by the transmitter, an envelope detector, a limiter, and a quench oscillator. The input RF signal is injected to the periodically quenched DCO to produce input-dependent oscillation envelopes. When we use the loop antenna as the inductive load in the DCO, the low noise amplifier in the block diagram could be bypassed. Incorporating a low-noise amplifier generally provides input matching and improved isolation for the oscillator. The LNA also serves as a buffer.
between the antenna and the oscillator. Ideally, we want the injection signal source to have infinite output impedance, as is the case with an ideal source. The quench oscillator supplies the bias current of the DCO, controlling the negative conductance generated by the active devices. The bias current is periodically varied so that the circuit selects and amplifies the sampled RF signals. The envelope detector senses the oscillation envelope and its outputs are fed to a limiter (or comparator). The limiter determines if and when the oscillation occurs and reflects the strength of the detected signal. To save the power consumption in the RF front-end, decision for generating corresponding digital data is made in the baseband processor. Quench control logic can be implemented in the baseband area.

Figure 6.5: Proposed Super-regenerative Receiver Architecture

6.2.2.3 Frequency Calibration

Considering that the oscillator’s on-chip RLC tank is sensitive to process, power supply voltage, and temperature (PVT), a certain level of frequency tuning scheme is indispensable. In addition, regulatory MICS multi-channel operation further necessitates frequency tuning scheme. Modern transceivers typically use frequency synthesizers to phase-lock a voltage-controlled oscillator (VCO) to a very stable reference such as a crystal oscillator. However, PLL based frequency tuning schemes require so much energy that it is not suitable for such device as implants whose operation will be limited by the
battery lifetime or the amount of energy scavenged. Furthermore, there are plenty of reasons for the ultra-low power medical implants to circumvent the use of a frequency synthesizer: first, the frequency stability requirement for MICS (±100 ppm) is far more relaxed than typical systems and second, the human body provides excellent temperature regulation reducing both the amount of overall frequency drift and its rate of change. Instead of relying on a phase-lock loop, Bohorquez et al proposed to exploit distributed feedback loop between the external controller and the implantable device. This scheme adopts a frequency correction loop which pushes complexity from the implant to the base-station [65]. In this scheme, the base-station monitors the DCO’s oscillation frequency and sends information to the implant to correct frequency errors.

6.3 Low Power Building Block Design

6.3.1 Low Power VCO Design

In this section, we present our design for low power voltage controlled oscillator (VCO) for our MICS transceiver. Our differential NMOS VCO exploits the coupling effect of inductor load, and the capacitor bank achieves piece-wise linear approximation for the frequency-versus-code characteristic for a given digital tuning input range.

6.3.1.1 Low Power Oscillator Topology

We investigate several kinds of VCO topologies to identify a VCO topology suitable for MICS applications and describe low-power VCO topologies in this section. Implementation of fully integrated low power, low phase noise voltage controlled oscillators is one of the challenges for the design of radio frequency front-end modules. Oscillators can be grouped into several categories depending on their topological characteristics [71]-[74]. Single-ended topologies has single output terminal referenced to the ground whereas differential topologies has differential output port. Even though differential output oscillators have some disadvantage such as relatively large power consumption compared to the single ended counterparts, differential output oscillators are
generally preferred since they have large voltage swing, common mode noise rejection effects and good phase noise performance characteristics.

Differential oscillators are further grouped into two popular categories. One group is cross-coupled LC oscillators, and the other one is differential Colpitts oscillators [71]. A cross-coupled oscillator is one of the widely used oscillators, since it is easy to implement and has a relaxed start-up condition. A Colpitts oscillator has superior cyclo-stationary noise properties and hence can achieve potentially lower phase noise. However, Colpitts oscillators still pose some challenges such as stringent start-up condition and capacitance tuning issues. Table 6.2 summarizes characteristics of each oscillator topology.

Table 6.2: Comparison of Oscillator Topologies

<table>
<thead>
<tr>
<th>Single-ended</th>
<th>Differential</th>
</tr>
</thead>
<tbody>
<tr>
<td>Limited voltage swing</td>
<td>Large voltage swing</td>
</tr>
<tr>
<td>Small power consumption</td>
<td>Relatively Large power consumption</td>
</tr>
<tr>
<td>Sensitive to parameter variation</td>
<td>Common mode noise rejection</td>
</tr>
<tr>
<td></td>
<td>Better phase noise performance</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cross-Coupled (Complementary)</th>
<th>Differential Colpitts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Easy implementation</td>
<td>Implementation Issues (C1/C2)</td>
</tr>
<tr>
<td>Relaxed oscillation condition ($g_mR_p \geq 1$)</td>
<td>Strict oscillation condition ($g_mR_p \geq 4$)</td>
</tr>
<tr>
<td>Degraded phase noise performance</td>
<td>Better phase noise performance</td>
</tr>
</tbody>
</table>
6.3.1.2 Transformer Load Cross-coupled Oscillator

We adopt the cross-coupled oscillator topology due to a relaxed oscillation condition and the relaxed phase noise requirement of a VCO for WBAN applications. Figure 6.6 shows a cross-coupled oscillator, which is the basis for our oscillator design. The oscillator in Figure 6.6 provides a higher output swing for very low supply voltages owing to only a single stack of transistor [72]. Also, it achieves better phase noise performance than other versions, since it does not need any active devices such as a current source. The DC output of the VCO is biased at $V_{DD}$ so that the output swing of the VCO can be as high as $2V_{DD}$.

![Figure 6.6: Cross-coupled VCO without a Current Source](image)

The cross-coupled oscillator shown in Figure 6.6 has two inductors, which occupy fairly large die area. One of the schemes to mitigate the shortcoming is to exploit the coupling effects of the two inductors. As depicted in Figure 6.8, the voltage outputs of the two inductors have $180^\circ$ phase difference. Use of cross-coupled inductors in the opposite direction rather than two separate inductors can save the die area and possibly enhancing the performance, especially through the increased Q-factors. Coupling the two inductors can be realized by a fully monolithic transformer. Hence, we propose to utilize the
transformer load by effectively coupling the two inductor loads of cross-coupled oscillator named TF-VCO.

A monolithic transformer has a higher Q-factor than that of a single LC tank. Figure 6.8 shows the simplified electrical models of an inductor and a transformer. Since each transformer winding has an L/2 inductance and an equivalent resistance of R/2, the Q-factor of the transformer is expresses as:

\[
Q_{load} \approx \frac{\omega_{osc} (1 + k)L}{2} \geq \frac{\omega_{osc} (1 + k)L}{R} \approx (1 + k)Q_{ind}
\]  

(6.11)

where \(\omega_{osc}\) is the oscillator’s resonant frequency, \(Q_{load}\) and \(Q_{ind}\) are the Q-factors of the loaded transformer and the inductor, respectively, Parameter \(k\) is the coupling coefficient. Although it is derived from a simple inductor model, the expression reveals that a transformer-based LC tank can achieve a higher quality factor than that of a single LC tank.

Figure 6.7: Transformer Load VCO
6.3.1.3 Antenna Loading

Recently, researchers suggested using dual spiral antennas for implant devices and capsule endoscope system applications [75]. A spiral antenna is modeled as different sized loop antennas, and a small loop antenna is regarded as a magnetic dipole with an omni-directional radiation pattern. Since a very small sized antenna has an isotropic radiation pattern, a dual spiral antenna also has an isotropic radiation pattern. An isotropic radiation pattern is desirable for implant applications because the radiation pattern is detected at any position.

A major advantage of the proposed transformer load VCO (TF-VCO) is the ability to incorporate a dual spiral antenna as an inductive tank load for the direct VOC modulation scheme. Figure 6.9 illustrates TF-VCO loading dual spiral antenna as an inductive element.
6.3.2 Capacitor Bank Design

MICS devices operate over the 402 MHz to 405 MHz band with the maximum channel spacing of 300 kHz. Employment of sub-threshold transistor biasing and a fairly large inductor with a high Q-factor poses a challenge for the DCO design in the MICS band, because it requires an extremely small unit capacitor cell to meet the spacing of 300 kHz. The oscillation frequency of the DCO is given as:

\[ f_0 = \frac{1}{2\pi \sqrt{L(C_0 + C_{var})}} \]  

(6.12)

where \( L \) is the tank inductance, \( C_0 \) is the constant capacitance due to the device and wiring parasitic, \( C_{var} \) represents the variable capacitance used to tune the frequency. For example, given the 100 ppm frequency stability criteria and the 5% tuning range (393~413 MHz), the approximate required number of frequency steps \( M \) is calculated as:
\[ M \geq \frac{\text{Tuning range}}{\text{resolution}} = \frac{20\text{MHz}}{20\text{kHz}} = 1000 \] (6.13)

The capacitance must have the ability to tune minimum 20 kHz step size, which corresponds to at least ten control bits of tuning. Assuming an inductance load of 20 nH, the capacitance be able to tune from 7.425 pF to 8.201 pF with a minimum capacitor step size of 0.36 fF which is impractically small to implement with conventional CMOS technologies. Implementation of a 0.36 fF for the least significant bit (LSB) capacitance poses a challenge, since parasitic capacitances in the modern technologies are on the same order of magnitude.

One possibility is to use small diode varactors switched between high and low capacitance states depending on the digital modulating signals. Another way to realize extremely small capacitance is using the gate capacitance of a MOS transistor. A diode varactor exploits the trait that a reverse-biased p-n junction can serve as a variable capacitor. The capacitance of a diode varactor is determined by the device size and the reverse bias voltage applied to the junction. However, the nonlinear capacitance of a diode varactor incurs phase noise due to the coupling of the control voltage to the tank. Furthermore, diode varactors are vulnerable to the PVT (Process, Voltage, and Temperature) variations.

NMOS or PMOS gate capacitance has also been widely used to realize a small unit capacitance. Recently, Han et al. proposed to use complementary MOS capacitance for fine tuning [76]. A complementary MOS capacitor shows extremely small capacitance that is an order of magnitude smaller than a PMOS or NMOS capacitance. Table 6.3 gives unit capacitances available in various processes [76]. In summary, MOSFETs offer small unit capacitance. One drawback is phase noise due to the coupling of the control voltage to the tank.
Table 6.3: Capacitance of MOSFET in Various Processes

<table>
<thead>
<tr>
<th>Process</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Complementary</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C&lt;sub&gt;on&lt;/sub&gt;</td>
<td>C&lt;sub&gt;off&lt;/sub&gt;</td>
<td>ΔC</td>
</tr>
<tr>
<td>65 nm</td>
<td>200a</td>
<td>104a</td>
<td>96a</td>
</tr>
<tr>
<td>90 nm</td>
<td>253a</td>
<td>143a</td>
<td>110a</td>
</tr>
<tr>
<td>130 nm</td>
<td>3.7f</td>
<td>2.0f</td>
<td>1.7f</td>
</tr>
<tr>
<td>180 nm</td>
<td>4.2f</td>
<td>2.2f</td>
<td>2.0f</td>
</tr>
</tbody>
</table>

6.3.2.1 Switched Capacitor Cell

A switched capacitor implemented with linear capacitors avoids the problems of varactor diodes and MOS capacitances. Switched capacitors using a standard metal-insulator-metal (MIM) capacitor has much a lower temperature coefficient than varactors and allows a digital signal to control capacitor banks, enabling fully digital implementation. A switched capacitor bank can be used to a small capacitance step, and Figure 6.10 shows a simplified schematic of a switched capacitor cell structure [74]. When the switch \( V_{ctrl} \) changes from on to off, the change in capacitance at the output node \( V_o \) is obtained as:

\[
\Delta C = \frac{C_u}{N+1} \tag{6.14}
\]

The minimum value of metal-insulator-metal (MIM) capacitor \( C_u \) available from 0.18 CMOS process standard library is about 20 fF. According to the above expression, the required ration \( N \) is 55 to meet the minimum unit capacitance 0.36 fF. The switched capacitor architecture exploits the rationing scheme with larger unit capacitors \( C_u \) and offers several advantages. First, any routing parasitics at the input node has no effect upon \( \Delta C \). Furthermore, any routing or switch parasitics at the node \( V_m \) may be lumped into the array of N capacitors and so some explicit capacitors may then be removed to
maintain the desired $\Delta C$ [74]. Second, it allows standard digital outputs to control the capacitor bank.

![Figure 6.10: Switched Capacitor Cell Structure](image)

### 6.3.2.2 Capacitor Bank Topology

A model of a capacitor bank composed of $2^N - 1$ identical varactors is shown in Figure 6.11, where it can be seen that the varactor consists of a unit switched capacitor cell. Each unit switched capacitor cell is controlled by a digital control word $(d_{n-1}, \ldots, d_2, d_1, d_0)$ and the total capacitance, $C_{\text{total}}$, can be represented as:

$$C_{\text{total}} = (2^N - 1)C_0 + d_0 \times \Delta C + d_1 \times 2\Delta C + \cdots + d_{N-1} \times 2^{N-1} \Delta C$$  \hspace{1cm} (6.15)$$

where $C_0$ and $\Delta C$ represent the offset and unit capacitance of the switched capacitor cell, respectively. We can easily find that the total capacitance of the sub-bank is linearly dependent on the incremental capacitance $\Delta C$ and the sub-bank is binary coded. The simulation result also shows the linear relationships between the total capacitance, $C_{\text{total}}$ and the increment, $\Delta C$. 


The minimum MIM cap $C_u$ for a unit switched capacitor cell available from IBM 130 standard library is about 60 fF, for example. Simple calculation lead us to have the desired ration $N$ of 600 to meet the minimum unit capacitance 0.1 fF. Hence simple approach is not desirable for the bank structure. In order to further reduce the incremental capacitor changes, noble capacitor bank structure is proposed as shown in Figure 6.13. The tuning capacitor bank consists of coarse, medium and fine tuning sub-banks. In this proposed structure, the effective change in the total capacitor bank is much smaller than
changes made to the sub-bank because of the small capacitors connected in series with capacitor sub-bank. As shown in Figure 6.14, the simulation result shows that this topology allows switched capacitors on the order of 60 fF to be used while achieving incremental capacitance changes across the inductor on the order of 0.1 fF.

Since VCO output frequency is proportional to $1/\sqrt{C}$, the total capacitance of the capacitor bank must take an exponential form of $n^{-2}$, rather than a linear form to obtain perfectly linear coarse tuning characteristics. One way to obtain linearity in frequency tuning is that each capacitor bank is thermometer coded and predistorted. Capacitor predistortion can be used to mitigate nonlinearity. To achieve a perfectly linear digital-to-frequency relationship, each desired frequency is used to find the respective values of unit capacitor cell. Implementing each unique incremental values of capacitance, however, would be impractical. Instead, a very good piece-wise linear approximation is usually implemented using a thermometer-coded capacitor bank.

![Figure 6.13: Proposed Capacitor Bank Topology](Image)

Figure 6.13: Proposed Capacitor Bank Topology
6.3.2.3 Capacitor Bank Implementation

We have designed a digitally controlled transformer load oscillator (DCO) with TSMC 180 nm RF CMOS process. The tuning frequency of a digitally controlled oscillator (DCO) is controlled by the capacitor value of the oscillator. The inductor value for our DCO is chosen as high as 20.7 nH which is relatively large compared to the typical monolithic ones. A fairly large inductance with a high Q-factor poses a challenge for the DCO design in MICS band, because it requires extremely small unit capacitor cells for the fine tuning capability. For example, given the 100 ppm frequency stability criteria and 5% tuning range (391–413 MHz) which is enough considering MICS occupies only 3MHz bandwidth, the capacitance must have the ability to tune minimum 20 kHz step size which corresponds to at least ten control bits of tuning. Assuming an inductance load of 20 nH, the capacitance must tune from 7.425 pF to 8.201 pF with a minimum capacitor step size of 0.36 fF which is impractically small to implement with the conventional CMOS technologies.

In order to achieve a sub-femto unit capacitance step, we adopt a switched capacitor cell array using a metal-insulator-metal capacitor (MIM cap). The minimum
value of the MIM cap available from the TSMC 180 nm RF CMOS process is about 20 fF, requiring N = 55 for a step of 0.36 fF. Use of identical size capacitors requires a large number of capacitors.

### 6.3.3 Performance Evaluation

The proposed DCO was designed with TSMC 180 nm RF CMOS process. A symmetrical octagonal center-tapped inductor available from the standard library was used to implement the transformer load. A center-tapped inductor with 9 turns of 30 µm thick topmost metal layer achieves a large inductance of 20.7 nH with Q-factor of 7.1, and all these parameters were chosen carefully to maximize the Q-factor at around the MICS frequency band. The implemented capacitor bank exhibits a unit capacitance step as small as 302 aF, which corresponds to the frequency resolution of 8.6 kHz. The DCO with a 12-bit digital tuning signal covers from 386 MHz to 419 MHz, which includes the entire MICS band.

The performance of our DCO is summarized and compared with other published ones in Table 6.4. The figure-of-merit (FOM) from [77] is used for the table expressed as:

\[
FOM = 10 \log \left( \frac{f_0}{\Delta f} \right)^2 \frac{1}{L(\Delta f) \times V_{dd} \times I_{dd}}
\]  

(6.16)

The FOM for our work is 188dB, which is favorable compared to other works in the table. The supply voltage for our DCO could be scaled as low as 600 mV, while exhibiting acceptable performance and the power consumption is 314 µW for the supply voltage.

Figure 6.15 shows the transient response of the DCO under the supply voltage, in which the start up is less than 100 ns for both frequencies, 386 MHz and 419 MHz. The low supply voltage reduces the output voltage swing, which is 360 mV peak-to-peak (p-p) for 386 MHz and 540 mV p-p for 419 MHz. Figure 6.16 show the phase noise of our
DCO under the supply voltage of 600 mV. The phase noise at 1 MHz offset is -128.9 dBc/Hz under the bias current of 523 µA, which is relatively small compared to the conventional LC oscillators.

Figure 6.15: Transient Responses Under the Supply Voltage of 600 mV
Figure 6.16: Phase Noise Performance @ 401 MHz

Table 6.4: Performance Comparison for the Designed DCO

<table>
<thead>
<tr>
<th>Reference</th>
<th>$V_{dd}$ (V)</th>
<th>$I_{dd}$</th>
<th>Freq.</th>
<th>Phase Noise (dBc/Hz)</th>
<th>Tuning Range</th>
<th>Freq. Resolution</th>
<th>FOM</th>
<th>Inductor</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work</td>
<td>0.6</td>
<td>523 µA</td>
<td>400 MHz</td>
<td>-129@1MHz</td>
<td>8.2%</td>
<td>8.6 kHz</td>
<td>188</td>
<td>On-chip</td>
</tr>
<tr>
<td>[38]</td>
<td>1.5</td>
<td>2.2 mA</td>
<td>400/800 MHz</td>
<td>-97.7@116kHz</td>
<td>n/a</td>
<td>n/a</td>
<td>166</td>
<td>On-chip</td>
</tr>
<tr>
<td>[65]</td>
<td>0.7</td>
<td>450 µA</td>
<td>400 MHz</td>
<td>n/a</td>
<td>6%</td>
<td>2 kHz</td>
<td>n/a</td>
<td>External coils</td>
</tr>
<tr>
<td>[66]</td>
<td>0.7</td>
<td>300 µA</td>
<td>400 MHz</td>
<td>n/a</td>
<td>2.5%</td>
<td>10 kHz</td>
<td>n/a</td>
<td>External coils</td>
</tr>
<tr>
<td>[74]</td>
<td>0.5</td>
<td>100 µA</td>
<td>1.9 GHz</td>
<td>-114@1MHz</td>
<td>n/a</td>
<td>190</td>
<td>Bond-wires</td>
<td></td>
</tr>
</tbody>
</table>
6.3.4 Programmable Quench Oscillator

The DCO of a super-regenerative receiver (SRR) is turned on and off at the quench rate to sample input RF signal. The quenching signal determines characteristics of the SRR’s response to an input signal. The selectivity of an SRR is also affected by the quench frequency. Since the quench frequency is equal to the receiver’s data rate, decreasing the quench frequency results in improved selectivity at the cost of a low data rate. The quench signal controls the negative conductance from the active devices of the negative $G_m$ LC oscillator. Since the negative conductance is proportional to the bias current of an oscillator, the periodic quench signal that controls the bias current of the DCO should be carefully designed to optimize the SRR’s performance. Various quench signals such as sinusoidal, sawtooth, triangular and rectangular waveforms are used. We propose to use either sawtooth or exponential quench waveform, because they exhibit better performance than the others [78]-[80]. We developed both types, sawtooth and exponential, quench signal generators, i.e., oscillators, to investigate their performance. A sawtooth signal generator is relatively simple compared to its exponential counterpart, but relatively poorer in performance.

6.3.4.1 Sawtooth Quench Oscillator

Figure 6.17 shows a simplified schematic diagram of a sawtooth oscillator used to generate a quench signal for an SRR [65]. The sawtooth voltage waveform $V_S$ is the voltage across the capacitor $C_S$, which integrates the current $I_S$ over time. Once voltage $V_S$ exceeds $V_{REF}$, a comparator turns on an nMOS switch, that discharges the capacitor and forces $V_S$ back to zero. This causes the comparator to turn off the nMOS switch and restart the cycle. The comparator includes some delay stages that cause $V_S$ to stay low and $V_{SW}$ to stay high for a short period of time as shown in Figure 6.18. The frequency of the quench oscillation is tuned using the programmable current $I_S$ and is approximately expressed as:

$$f_Q \approx \frac{I_S}{C_S V_{REF}}$$  \hspace{1cm} (6.17)
The voltage waveform $V_S$ is converted to a current $I_{bias}$ using a degenerated common-source pMOS transconductor. Through the current-mirror, $I_{bias}$ will provide the bias current $I_{DCO}$, controlling the negative conductance in the DCO. In order to save the power consumption in the quench signal generator, all the transistors are biased to operate in the weak inversion region.

![Figure 6.17: Sawtooth Quench Signal Generator](image)

Figure 6.17: Sawtooth Quench Signal Generator

![Figure 6.18: Timing Diagram of a Sawtooth Qench Signal Generator](image)

Figure 6.18: Timing Diagram of a Sawtooth Quench Signal Generator
6.3.4.2 Exponential Quench Oscillator

Traditionally, exponential circuits are implemented using the exponential-law characteristics of transistors, such as MOS transistors in the weak inversion [81]. We propose to use a low-voltage low-power current mode exponential circuit as shown in Figure 6.19 [82]. All the transistors are biased in the weak inversion region to operate in low-power. Transistors M1, M2, M3, and M4 of the circuit form two multipliers. The current source IB and the voltage follower M5 are added to keep M2 and M3 in the weak inversion region, and prevent the bulk-to-source junctions from forward bias. Here, $I_3$ can be expressed as

$$I_3 = \frac{I_2 I_4}{I_1} = \frac{(I_B + I_{in})^2}{I_B} = I_B + 2I_{in} + \frac{I_{in}^2}{I_B}$$

Therefore, applying taylor’s series expansion the output current $I_{out}$ can be obtained as

$$I_{out} = I_B + I_3 = 2I_B\left(1 + \frac{I_{in}}{I_B} + \frac{I_{in}^2}{2I_B^2}\right) \approx 2I_Be^{I_{in}/I_B}$$

The output current $I_{out}$ follows exponential dependency on the input current $I_{in}$.

![Exponential Circuit Diagram](image-url)

Figure 6.19: Exponential Circuit Diagram
A sawtooth signal generator followed by an exponential circuit constructs an exponential quench signal generator as shown in Figure 6.20.

![Figure 6.20: Block Diagram of an Exponential Quench Generator](image)

### 6.4 Chapter Summary

We proposed to use direct VCO modulation transmitter and super-regenerative receiver for MICS transceiver. Incorporating dual spiral antenna as a VCO inductor load circumvents the use of Power Amplifier, resultantly reducing overall power consumption. We also suggested adopting distributed frequency calibration loop by exploiting the characteristics such as relaxed frequency calibration stability criteria and excellent temperature regulation property of the human body in MICS applications. This approach eliminates the use of power hungry frequency synthesizer such as phase-locked loop. Several crucial building blocks including digitally-controlled oscillator (DCO) and quench signal generators were proposed and designed using the minimum number of external components. Simulation results envision fully on-chip implementation of the MICS transceiver.
Chapter 7:
Conclusion

Wireless Body Area network (WBAN) has tremendous potential to transform how people interact with and benefit from information technology. WBAN applications include medical, consumer electronics / personal entertainment and others. They will usher a new generation of wireless control and monitoring applications that were inconceivable in the past. While the prospect for WBAN products is high, meeting the required device performance with an extremely small amount of power consumption poses significant design challenges. The front-end of a wireless device is responsible for a major power dissipation of the system, and it is particularly true for small wireless devices such as for WBANs. Hence, reduction of power dissipation for the RF front-end of a WBAN device is crucial for overall efficiency. This dissertation investigates the specification and requirement of the recently developed draft IEEE standard for WBAN, proposes low-power RF front-end architecture for MICS transceiver, and presents the implementations of crucial building blocks such as frequency source generation, receiver front-end, and transmitter front-end.

First, Chapter 3 investigated the newly developed draft IEEE 802.15.6 PHY specification for narrow band WBAN applications focusing on the PHY protocol which covers packet structure, modulation scheme, etc. The physical layer of the standard adopts simple and low-complexity channel coding schemes such as BCH, spreading, interleaving, and scrambling. The scrambled bit stream is mapped onto the appropriate constellation using rotated differential phase shift keying ($\pi/n$-DMPSK) with square root raised cosine (SRRC) pulse shaping, which is determined by the data rate and frequency band of operation. For the system performance analysis, ideal transceiver was implemented and simulated through an AWGN channel using the bit error rate (BER) and packet error rate (PER) as the figure of merit. Performance analysis results exhibits that the receiver has processing gains of 2.2 dB for $\pi/2$-DBPSK, 2.9 dB for $\pi/4$-DQPSK,
and 3.3 dB for $\pi/8$-D8PSK, respectively, for PER = 0.1 as required by the standard. Based on the performance analysis, link budget analysis was performed. It shows that resultant maximum allowed system noise figure (NF) ranges from 22.95 dB to 17.35 dB, which are more relaxed compared to the ZigBee counterpart.

Next, Chapter 4 investigated candidate RF front-end architectures for the development of MICS transceiver. As the MICS application features low data rate, higher bandwidth requirement is mitigated for the low-IF architecture. Furthermore, Low-IF receiver is less sensitive to flicker noise and DC-offset at the expense of a higher image-rejection requirement. Based on this comparative study, we proposed to adopt direct conversion transmitter and low-IF receiver architecture for the MICS RF front-end. An asynchronous wake-up receiver architecture is also proposed, which is composed of carrier sensing circuit and serial code detector.

In Chapter 5, implementation of low-power and low-cost building blocks for an RF transceiver front-end was presented including frequency source generation, receiver front-end, and transmitter front-end blocks. All the building blocks were implemented in TSMC 0.18 µm RF CMOS process. Performance of the designed RF front-end was evaluated by simulation in circuit level. Two quadrature signal generation techniques were implemented. The presented QVCOs are based on the frequency division and the quadrature coupling methods. Total power consumption of the D-QVCO is four times smaller than that of the P-QVCO so that D-QVCO is considered better suited for MICS applications. A noble low-power receiver front-end was also implemented. By stacking LNA and down-conversion mixer, we came up with low supply and low power RF front-end. Various low power circuit techniques such as gm-boosting and sub-threshold operation were exploited. Performance evaluation exhibits that the merged LNA and Mixer consumes 1.84 mW under a supply voltage of 1.2 V. and has the overall noise figure of 3.6 dB. For the transmitter front-end, driver amplifier (DA) and up-conversion mixer were presented. The proposed DA uses cascaded PMOS transistors to minimize Miller effect and enhance the input/output isolations. The up-conversion mixer is based on the Gilbert cell implemented with resistive loads. Meanwhile, a direct antenna matching scheme was proposed to share the inductor loads with the receiver path.
Finally, direct VCO modulation transmitter and super-regenerative receiver were proposed and presented as a case study in Chapter 6. Constant envelope modulation scheme is power efficient approach to minimize overall power consumption. The proposed RF transceiver architecture operates on the constant modulation scheme. Incorporating dual spiral antenna as a VCO inductor load circumvents the use of Power Amplifier, resultantly reducing overall power consumption. Several crucial building blocks including digitally-controlled oscillator (DCO) and quench signal generators were proposed and designed using the minimum number of external components. Simulation results envisioned fully on-chip implementation of the MICS transceiver.
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