
Hyung-Jin Lee

A dissertation submitted to the committee on Graduate Studies of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

Committee:
Dr. Dong S. Ha, Chairman
Dr. James R. Armstrong
Dr. R. Michael Buehrer
Dr. Joseph G. Tront
Dr. Tom Martin

February 13, 2006
Blacksburg, VA

Keywords: Ultra Wideband, CMOS, Radio Frequency Integrated Circuit, Digital Receiver, Low power

Hyung-Jin Lee

(ABSTRACT)

CMOS technology is particularly attractive for commercialization of ultra wideband (UWB) radios due to its low power and low cost. In addition to CMOS implementation, UWB radios would also significantly benefit from a radio architecture that enables digital communications. In addition to the normal challenges of CMOS RFIC design, there are two major technical challenges for the implementation of CMOS digital UWB radios. The first is building RF and analog circuitry covering wide bandwidth over several GHz. The second is sampling and digitizing high frequency signals in the UWB frequency range of 3 GHz to 10 GHz, which is not feasible for existing CMOS analog-to-digital converters.

In this dissertation, we investigate the two technical challenges at the circuit level and the system level. We propose a systematic approach at the circuit level for optimal transistor sizing and biasing conditions that result in optimal noise and power matching over a wide bandwidth. We also propose a general scheme for wideband matching. To verify our methods, we design two single-stage low noise amplifiers (LNAs) in TSMC 0.18μm CMOS technology. Measurement results from fabricated chips indicate that the proposed LNAs could achieve as high as 16 dB power gain and as low as 2.2 dB noise figure with only 6.4 mA current dissipation under a supply voltage of 1.2 V.

At the system level, we propose a unique frequency domain receiver architecture. The receiver samples frequency components of a received signal rather than the traditional approach of sampling a received signal at discrete instances in time. The frequency domain sampling leads to a simple RF front-end architecture that directly samples an RF signal without the need to downconvert it into a baseband signal. Further,
our approach significantly reduces the sampling rate to the pulse repetition rate. We investigate a simple, low-power implementation of the frequency domain sampler with 1-bit ADCs. Simulation results show that the proposed frequency-domain UWB receiver significantly outperforms a conventional analog correlator.

A digital UWB receiver can be implemented efficiently in CMOS with the proposed LNA as an RF front-end, followed by the frequency domain sampler.
Acknowledgements

I would like to thank my advisor, Dr. Dong Ha, for all of his guidance, advice, and motivation throughout my graduate studies. Being his graduate student and a member of Virginia Tech VLSI for Telecommunications Lab was a great opportunity. The support from my advisory committee members, Dr. James Armstrong, Dr. Joseph Tront, Dr. Thomas Martin, and Dr. Michael Buehrer was also greatly appreciated.

In addition, I am grateful to the people at Electronics and Telecommunications Research Institute in Korea including Dr. Hyung Soo Lee, Dr. Sang Sung Choi, Dr. Jae Young Kim, Bong Hyuk Park, and Seung Sik Lee for sponsoring this work. They provided excellent technical advice, and tremendous help on fabrication, measurements, and publication.

I am thankful for the support and assistance of my fellow members and graduates of VTVT Lab, including Woo Cheol Chung, Sajay Jose, Rajesh Thirugnanam, Shen Wang, Kevin Marsden and Dr. Tales Pimenta. I would like to especially thank Nathaniel August for his productive conversations, intensive help and making my life in Blacksburg pleasurable. All of them made my stay at Virginia Tech enjoyable in and out of research. I wish them all great success in their research and future career.

Finally, I would like to thank my parents, Sang Do Lee and Gui Sook Kim. Their constant and limitless love, support, encouragement, and advice were the most essential part of my work and had my dreams completed.
Dedication

To

my parents,

Sang Do Lee and Gui Sook Kim,

who made all of this possible,

for their endless encouragement and patience.

Also to

Jina Kim,

Thank you, my love,

for coming into my life.

You are my dream come true.
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Chapter 1: 
Introduction

On February 14, 2002, the Federal Communications Commission allocated spectrum for a new radio communication technique called ultra wideband (UWB) [1]. Compared to traditional narrowband systems, UWB offers many advantages including accurate ranging and extremely high-speed data communication.

Historically, UWB utilized an impulse signal [2], [3], [4], [5], which provides the most accurate ranging and simplest hardware implementation. However, due to the FCC’s relaxed definition of UWB, which allows a bandwidth as small as 500MHz, some companies proposed alternative signaling methods to impulse-based UWB (I-UWB). The most recent and famous alternative signaling methods are multiband orthogonal frequency division multiplexing (MB-OFDM) [6], [7] and direct-sequence UWB (DS-UWB) [8], [9], [10], [11]. Both alternatives are carrier-based schemes modified from narrowband technology to fill an ultra wide bandwidth. Carrier-based UWB (C-UWB) tends to consume more power than I-UWB because of the high-speed switching activity in the RF front-end at the carrier frequency. Additionally, C-UWB is more susceptible to multipath induced fading effects. Hence, for low-power and low-cost application, I-UWB is superior to C-UWB in terms of performance and implementation cost.

For commercialization in consumer electronics devices, a low-cost, low-power implementation of UWB is essential. Due to the challenges of designing high-speed, wide-bandwidth components, initial implementations of UWB systems were based on high-speed technology such as SiGe and GaAs [12], [13], which incur relatively high power dissipation and cost. However, for low-power implementation, CMOS is the technology of choice because of its inherent low-power characteristics. Further, the popularity of CMOS allows low-cost implementation due to the wide range of commercial tools, the large body of expertise in CMOS design, and the widespread
adoption of CMOS manufacturing. In addition, CMOS offers the possibility of a complete UWB System-on-Chip (SOC) because CMOS dominates digital circuit designs. Although a complete UWB system can be realized with a relatively simple hardware structure in CMOS, some major challenges to commercialization stem from the implementation technology.

First, CMOS is not particularly suitable RFIC design due to its inherent physical limitations. Because of its relatively large capacitance, CMOS possesses a lower unity-gain frequency than other technologies. The unity-gain frequency is in the range of 20 GHz to 30 GHz for 0.18\textmu m CMOS technology; as a general design rule, the circuit should operate at about one-fifth of the unity-gain frequency. Thus, UWB, which can contain frequency components up to 10 GHz, pushes the limits of CMOS technology. A related challenge arises in that there are few accurate RF models for CMOS operating at such frequencies.

A key RF component for a UWB radio is low noise amplifier (LNA). Since the maximum allowable radiation power for UWB is only -41.3 dBm/MHz [1], a UWB LNA should provide a very low noise figure, and the typical required noise figure is lower than 3 dB. Several CMOS UWB LNA architectures were reported in [27], [28], and [44]. Each method intends to accommodate a wide bandwidth through input and/or output impedance matching. The CMOS UWB LNA introduced in [27] employs a Chebyshev filter structure for input matching and a source follower for output matching. Although this LNA is suitable for low power, it achieves a relatively low power gain of 10 dB, and incurs a high noise figure of 9 dB in the upper UWB frequency ranges due to the large number of passive components used for the Chebyshev bandpass filter. Another approach, named a distributed amplifier reported in [28], employs multiple narrowband LNAs to realize wideband matching. The distributed amplifier guarantees good matching performance and a high power gain over extremely wide bandwidth of 0.6 GHz to 22 GHz. However, it occupies impractically large silicon area, consumes large power, and results in a high noise figure up to 6 dB due to multiple amplifiers. So there is still room for substantial improvement in noise figure for existing CMOS LNAs, which motivated us to conduct research in this area. We investigated to develop a systematic design methodology for implementation of CMOS UWB LNAs. We exploited Miller effect,
which is relatively large and often considered as undesirable side-effect, to build an input impedance matching network. The method reduces the number of passive components to result in lower power dissipation and smaller silicon area. We also suggested a systematic transistor sizing and biasing method to optimize the noise performance. We designed an LNA based on our design methodology and measured its performance on test chips fabricated in TSMC 0.18 μm CMOS triple-well technology. Our LNA achieves the noise figure as low as 2.2 dB and high power gain of 16 dB over the target frequency band of 3 GHz to 5 GHz with good input and output impedance matching over the entire frequency band. The good noise performance of our LNA is due to reduction of the number of passive components used for input impedance matching and a systematic transistor sizing and biasing method to optimize the noise performance. Our LNA dissipates 7.68 mW and occupies 740 μm x 850 μm, which is the remarkably small for both in power dissipation and area compared to other reported CMOS UWB LNAs such as [27], [28], and [44]. It should be noted that we also explored several layout techniques such as shielding and guard ring to improve noise isolation performance furthermore.

Secondly, sampling extremely narrow UWB signals may not be feasible for existing analog-to-digital converters (ADCs) or it requires excessively complex hardware dissipating a prohibitively large amount of power or result in serious signal loss [14]. Thus, most existing I-UWB receivers are based on analog correlation, which correlates the received signal with a locally stored template pulse. However, an analog UWB receiver does not exploit the benefits of digital signal processing. For example, it is difficult for an analog UWB receiver to accurately control the timing of the signal reception, which degrades the performance.

Several methods to sample UWB signals were reported in [34], [35], and [36]. The method reported in [34] relies on a time-interleaving technique for multiple ADCs, in which each ADC samples the signal by equally time-spaced clock triggering. This method is highly sensitive to the timing jitter, so the time resolution capability of multiple clock signal generation dominates the sampling speed. Also, since each ADC has to sample a wideband signal, design of the front-end circuitry remains difficult. The alternative methods reported in [35], [36] utilizes a channelization technique. The channelization technique divides the entire signal band into multiple sub-bands, so each
ADC assigned to each sub-bands samples the signal in a fractional sampling rate to the original sampling rate. One problem with the channelization method lies in the use of non-ideal bandpass filters, which lead to overlapping of transition bands to cause the aliasing problem. Therefore, high performance bandpass filters are necessary for the channelization technique.

To address the shortcomings of existing methods described above, we investigated a different approach called frequency domain sampling in this dissertation. Our method samples frequency components of received signals, more specifically, it samples Fourier series coefficients within a certain time window using narrowband bandpass filters. Since the frequency domain approach samples the UWB signal in the RF passband rather than in the baseband, our UWB receiver does not require a downconverting mixer and baseband analog circuitry, such as a variable gain amplifier (VGA) and a lowpass filter (LPF). Therefore, the RF front-end of our UWB receiver consists of only the CMOS UWB LNA and the frequency domain sampler. Another advantage of the frequency domain approach is the ability to process multipath signals without using a conventional rake receiver.

This dissertation is organized as follows. Chapter 2 briefly reviews some fundamental characteristics of UWB, including signaling, modulation schemes, and applications. Chapter 3 explains and verifies a design methodology to build a UWB LNA with CMOS technology. In Chapter 4, we introduce a unique sampling method to relax the speed requirement of ADCs by sampling the spectrum of the received signal rather than time domain signal shape. We describe a receiver architecture based on this sampling technique that is suitable for CMOS implementation. In addition, a method to simplify the receiver for ultra low-power applications is also proposed. Finally, Chapter 5 concludes the dissertation.
Chapter 2: Preliminaries

2.1 History of Ultra Wideband

In 1901, an ultra wideband (UWB) communication was the first trans-Atlantic wireless transmission [15]. The sender, Gugliermo Marconi, created an impulse-like UWB signal by using the random conductance of a spark-plug.

The term UWB was first used in 1989 by the US Department of Defense. In addition to impulse-based wireless signaling, the term UWB has also been used in wireless communication to mean carrier-free, baseband, large-relative-band, radio/radar, nonsinusoidal, orthogonal function, or time-domain. Any communication system in which the instantaneous bandwidth is many times greater than the minimum necessary to transmit information can be classified as a UWB communications system.

The modern era UWB started in 1969 with the work of Harmuth at Catholic University of America; Ross and Robbins at Sperry Rand Corporation; and Paul van Etten at the USAF Rome Air Development Center [16], [17], [18]. Harmuth presented the basic design of transmitters and receivers. Ross and Robbins introduced coding schemes and many applications, including communications and radar. Van Etten developed fundamental system designs and antenna concepts. Some additional research on pulse transmitters, receivers, and antennas was also performed by researchers at Los Alamos National Laboratory, Lawrence Livermore National Laboratory, and in Russia.

The development of sample-and-hold circuits by both Hewlett-Packard and Tektronix in the late 1960s greatly advanced the field of UWB, since the circuits provided a way to display and integrate UWB signals. Later, in 1972, the invention of a sensitive baseband pulse receiver replaced the sampling circuits and allowed the
implementation of the first UWB system design. Most subsequent research after the 1970s focused on improving this basic design.

The first UWB ground penetrating radar was commercialized in 1974. In 1994, the first Micropower Impulse Radar (MIR) was developed, and it was a very compact, inexpensive, and ultra low power UWB radar.

The data encoding methods for UWB were developed far before the first modern system implementations. By 1943, the US Army already knew of pulse-position modulation. In 1961, Hoeppner patented a representation of pulsed communications systems.

In 1993, Scholtz introduced a multiple access technique called time-hopping for UWB communications systems. The time-hopping technique allocates to each user a unique spreading code that determines specific instances in time when it is allowed to transmit. Time-hopping enables not only radar and point-to-point communications, but also wireless networks.

Since the late 1990s, there has been intense research in UWB. In February 2002, the Federal Communications Commission (FCC) opened the spectrum from 3.1 GHz to 10.6 GHz for unlicensed use of UWB technology [1].

The FCC ruling has generated considerable interest in developing UWB communication systems, and it has created several new opportunities for innovation and development.

The great potential of UWB lies in the facts that it can co-exist with the users of already licensed spectrum and that it opens a wide range of applications. Such applications include high-speed wireless personal area networks (WPANs) and wireless USB.

Existing UWB technology can provide data rates up to 480Mbit/s in real multipath environments with very little power dissipation or silicon area. Besides providing a low cost solution for the increasingly higher demands for data rates, UWB will also open new consumer market segments such as inventory tracking system by replacing the current bar code system.
2.2 Characteristics of Ultra Wideband

It was not until February 14, 2002 that UWB technology gained great momentum. On that date, the FCC allocated a 7.5 GHz band for indoor wireless communications. The FCC defines a UWB device as having a –10 dB bandwidth between 3.1 and 10.6 GHz, while meeting the spectrum masks shown in Figure 2.2, Figure 2.3, and Figure 2.4.

The FCC defines a UWB transmitter as "an intentional radiator that, at any point in time, has a fractional bandwidth equal to or greater than 0.20 or has a UWB bandwidth equal to or greater than 500 MHz, regardless of the fractional bandwidth." as shown in Figure 2.1 [19], [20].

Fractional bandwidth is the bandwidth expressed as a fraction of the center frequency. If \( f_H \) is the highest frequency limit with a signal 10dB below the peak emission and \( f_L \) is the lowest frequency limit with a signal 10dB below the peak emission, then the fractional bandwidth is defined as

\[
\eta = \frac{2(f_H - f_L)}{f_H + f_L}
\]  

(2.1)

For UWB, the limits of \( \eta \) are given by \( 0.20 < \eta \).

![Figure 2.1: Frequency spectrum of UWB and narrow band signals](image)
The FCC allocated a specific spectral mask for each category, as shown in Figure 2.2 and Figure 2.3 for communication systems. Observe that the limits change depending on the environment, indoor or outdoor.

![Figure 2.2: UWB indoor spectrum mask](image)

The spectrum mask shown in Figure 2.2 requires that the energy emitted from a UWB device not exceed -41.25 dBm/MHz. The mask shown in Figure 2.3 is for the UWB outdoor spectrum [20].

![Figure 2.3: UWB outdoor spectrum mask](image)
The differences between the indoor and outdoor masks are the strict attenuation requirements at 3.1 and 10.6 GHz. These strict requirements for outdoor UWB transmissions help protect GPS receivers, which are centered at 1.6 GHz [20].

Figure 2.4 presents the spectral mask for vehicular radar, and Figure 2.5 shows three masks for imaging.
There are many potential users of UWB, which can be classified in three different categories:

1. Communications and measurement systems,
2. Vehicular radar systems,
3. Imaging systems, including medical imaging, ground penetrating radar, through-walls imaging and surveillance systems.

Table 2.1 presents the restrictions of certain applications for each frequency range. Note that vehicular radar and communications and measurement systems are not restricted to certain operators.

**Table 2.1: Applications and restrictions of UWB imaging**

<table>
<thead>
<tr>
<th>Frequency Range</th>
<th>Application</th>
<th>Restrictions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>Ground penetrating radar (see or detect buried objects)</td>
<td>Law enforcement, fire and rescue, mining, construction, research</td>
</tr>
<tr>
<td>Medium</td>
<td>Through-wall imaging systems (detect location or movement of objects)</td>
<td>Law enforcement, fire and rescue</td>
</tr>
<tr>
<td></td>
<td>Surveillance systems (intrusion detection)</td>
<td>Law enforcement, fire and rescue, public utilities, industry</td>
</tr>
<tr>
<td>High</td>
<td>Ground penetrating radar (see or detect buried objects)</td>
<td>Law enforcement, fire and rescue, mining, construction, research</td>
</tr>
<tr>
<td></td>
<td>Wall imaging systems (detect objects contained in walls)</td>
<td>Law enforcement, fire and rescue, mining, construction</td>
</tr>
<tr>
<td></td>
<td>Medical Systems (imaging inside humans and animals)</td>
<td>Medical personnel</td>
</tr>
</tbody>
</table>

Instead of dividing the UWB spectrum into distinct bands that would be allocated to specific applications, the FCC allows them to operate in the same spectrum (with the exception of vehicular radar). As an additional restriction, UWB applications must not interfere with existing narrowband services, ideally at low enough power levels that the existing applications do not experience any degradation.
2.3 Ultra Wideband Signaling

UWB systems must be able to transmit and receive an extremely short duration burst of radio frequency (RF) energy – typically from a few tens of picoseconds to a few nanoseconds in duration. These bursts may be formed by one or a few cycles of an RF carrier wave. Therefore the waveform is extremely broadband, and it is often difficult to determine the real RF center frequency, and thus, the term "carrier-free".

There are basically two types of UWB communication: (i) impulse-based UWB (I-UWB) that is based on very short pulses and (ii) multicarrier UWB (MC-UWB) that is based on multiple simultaneous carrier signals.

2.3.1 Impulse-based UWB

Unlike classic communication systems, impulse-based UWB (I-UWB) does not use a carrier to convey information. The information is transmitted in a series of baseband pulses. Since the pulse durations are in the nanosecond range, the signal bandwidth is in the range of gigahertz.

Due to their short time duration, UWB pulses have some unique properties. In communications, UWB pulses can be used to achieve extremely high data rate in multi-user network applications. For radar applications, short pulses can provide very fine time resolution and precision for the measurement of distance and/or positioning.

Short pulses are relatively immune to multipath cancellation effects due to mobile and in-building environments. Multipath cancellation occurs when the direct path signal and an out of phase reflected wave simultaneously arrive at the receiver, thus causing a reduced amplitude response in the receiver. With very short pulses at short range, the reflected signal will arrive at the receiver after the direct signal is gone, and there is no cancellation. Therefore, I-UWB systems are well suited for high-speed, mobile wireless applications.
Since the bandwidth is large, the UWB energy density (power per Hertz) can be quite low. Low energy density translates into a low probability of detection which is of particular interest for military applications such as stealth communications and radar. At the same time, a low probability of detection also represents minimal interference to other systems and minimal RF health hazards. Figure 2.6 shows the typical spectrum of an impulse UWB signal.

Although the short time duration of an I-UWB pulse results in a high instantaneous power, FCC regulations ensure that a UWB signal appears mostly as noise to most other wireless devices. Thus, UWB can share the spectrum with existing applications such as IEEE 802.11a (WiFi).

UWB places some unique demands on the hardware, such as fast switching times for the transmitter and receiver (less than 100ps) and precise synchronization. In addition, transient problems of the antenna and the circuit become more relevant.

At the same time, the circuit may resemble a digital circuit, thus avoiding many problems associated with mixed-mode integrated circuits.
2.3.1.1 Binary Phase Shift Keying (BPSK)

The most common approach for modulation in I-UWB systems is BPSK. This method of modulation involves transmitting a single bit or chip of data with each pulse. A positive pulse represents a ‘1’, and a negative pulse represents a ‘0’ [21]. This is one of the simpler approaches, requiring that only two pulse shapes be generated. This simplicity results in less processing at the receiver.

Figure 2.7 shows the BPSK Modulation, that is a particular case of the PAM. In this scheme, the positive pulse may represent a +1 and the negative pulse may represent a -1. Obviously, these pulses may have other shapes.

![Figure 2.7: Binary phase shift keying](image)

2.3.1.2 Differential Phase Shift Keying (DPSK)

An alternative to BPSK is DPSK, which requires slightly more digital processing at the receiver end. The current pulse is based on the previous pulse. If a ‘1’ is to be
transmitted, the pulse will equal the previous pulse. And if a ‘0’ is to be transmitted, the pulse will be 180 degrees out of phase with the previous pulse. At the beginning of the bit stream, it is assumed that the previous pulse was a positive pulse. Figure 2.8 shows an example DPSK modulation scheme. Conceptually, DPSK can simplify an analog–correlator-based receiver by eliminating the template pulse generator. However, it is not easy for the receiver to control delay of the following pulse in order to perform correlation with two consecutive pulses.

Figure 2.8: DPSK modulation example

2.3.1.3 Pulse Position Modulation (PPM)

Pulse position modulation (PPM) is another alternative modulation method. Binary PPM involves transmitting the same pulse in one of two positions in the time domain in order to represent a ‘0’ or a ‘1’ [22]. This method may require a more complex receiver in order to determine the position of the received pulse.

As shown in Figure 2.9, the regularly spaced pulse train presents the reference time position of a pulse. In this particular case, if a pulse arrives before the reference, it can be considered as +1, and if the pulse arrives after the reference, it is considered as -1. Obviously, these pulses may have other representations. Figure 2.9 shows a pulse train with data values {-1, +1, -1}. 
2.3.2 Multicarrier UWB

Multicarrier communication was first used at the end of 1950s by the military. Instead of using a single pulse, multicarrier UWB (MC-UWB) divides the band into a few carriers. Figure 2.10 shows the typical spectrum of a MC-UWB signal.
Instead of filling the bandwidth with a single pulse, the spectrum is divided into sub-bands of approximately 500MHz. By interleaving the information across the sub-bands, MC-UWB is capable of maintaining the same transmission power as if it were a single signal using the entire bandwidth.

This approach allows information processing in a smaller bandwidth, thus reducing the complexity of the circuit, the power consumption, and the cost. Other advantages of this approach include an improvement in the spectral flexibility, inherent resilience to RF interference, and robustness to harmful multipath effects. Additionally, some associated circuits, such as the analog to digital converter (ADC), are also simplified. One drawback of this type of system is that the transmitter is more complex.
2.4 Modulation

The FCC has specified the spectral masks for communication applications, but it did not establish any particular modulation scheme. On the other hand, the IEEE 802.15.3a task group for wireless personal area networks (WPANs) considered two major candidates as the modulation standard: DS-CDMA and MB-OFDM. With the demise of the task group, the two proposals are now battling for supremacy in the market.

2.4.1 Direct Sequence Code Division Multiple Access

The Direct Sequence Code Division Multiple Access (DS-CDMA) proposal, proposed by Freescale and its associated companies, is fundamentally an impulse based approach [23].

DS-UWB is initially being developed for wireless personal area network (WPAN) applications. The DS-UWB proposal will enable devices to provide both the high performance capabilities as well as the low power/cost scalability required for high-data-rate multimedia and handheld applications. DS-UWB devices will operate under the UWB rules established by the FCC for the U.S. and under similar rules now under development in other parts of the world.

Initially, DS-UWB involved using the entire band from 3.1 to 10.6 GHz. However this approach was modified two divide the spectrum into two bands, one on each side of the 5GHz frequency band reserved for IEEE 802.11a, as illustrated in Figure 2.11. Typical DS-UWB devices occupy either 1.5 or 3 GHz of spectrum when transmitting.

The current FCC rules allow 7.5 GHz of spectrum, but at very low transmit power levels. In fact, DS-UWB emission levels will be at or below levels allowed for spurious or out-of-band emissions for other wireless technologies, roughly equivalent to a limit of -41.3 dBm/MHz of spectrum. Because of these low emission limits, a typical DS-UWB device will have a total transmit power of about -10 dBm over the signal bandwidth.
The DS-CDMA scheme uses BPSK modulation and a CDMA encoding scheme to support multiple users with superior coexistence properties.

![Figure 2.11: Spectral bands of the DS-CDMA proposal](image)

Some argue that this approach suffers from problems such as the near/far problem and that it requires a complex receiver. Further, signal processing at the high speeds of 100Mbps and above in the digital domain is a major concern for system designers. Timing synchronization, choice of technology (SiGe v/s CMOS), and sensitivity to ISI (inter-symbol interference) are also significant issues with this approach.

Nevertheless, Freescale argues that DS-CDMA has a faster time to market, since it has already developed chips using this technology for high data rate wireless applications. DS-CDMA also claims to achieve high speed, low power consumption, low cost, and small size.

### 2.4.2 Multi-Band Orthogonal Frequency Division Multiplexing

Texas Instruments proposed the Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) approach to support IEEE 802.15.3a. The document (03/268r3) [24], submitted in March 2004, suggests the use of the unlicensed band between 3.1 and 10.6 GHz for WPAN applications and is being considered in particular for wireless USB devices.
In this approach, the spectrum is divided into 14 bands (each with a bandwidth equal to 528 MHz), and devices are allowed to statically or dynamically select which bands to use for transmission. The data is then appropriately modulated using a concatenation of bands. All compliant transceivers must be able to tune to Band #1 and search for beacon signals.

The entire spectrum is divided into 4 distinct groups, as indicated in Figure 2.12. Only Group A is intended for first generation devices because of current technology limitations. Other groups have been reserved for future use.

![Figure 2.12: Spectral bands of the OFDM proposal](image)

The OFDM symbols can be transmitted in multiband OFDM as shown in Figure 2.13. The first symbol is transmitted in channel 1 (or Band #1), the second symbol is transmitted in channel 2 (or Band #2), and the third symbol is then transmitted in channel 3 (or Band #3); and the sequence is repeated again and again. As can be observed from the figure, a cyclic prefix is inserted at the beginning of each symbol and a guard interval is also appended to each symbol. The inclusion of the guard interval allows the use of a single transmitter and a single receiver chain. It also ensures sufficient switching time for both transmitter and receiver to switch to the next channel.
The use of sub-bands allows the operation of this system anywhere, since it can turn off sub-bands that interfere with other devices. Another advantage of a multiband approach is its ability to efficiently capture multipath signals.

MB-OFDM is thought of to be a more practical solution for global regulation, less sensitive to timing synchronization errors and easily realizable in CMOS. Additionally, this approach may reuse many techniques known for narrowband systems.

However, opponents question the circuit complexity, especially the transmitter and there may exist Multiple Access Interference – MAI. Further, applications such as a RFID would not be easily implemented in a multiband approach.

Although this competition is yet to be resolved by the market, both the groups have implemented their respective proposals to verify the feasibility.
2.5 Applications

The potential of UWB systems is extremely vast because of the inherently high data rate and low power dissipation due to possible simple architecture. Conventional narrowband circuits consume more power compared and can currently achieve, at most, the 54 Mbps data rate of IEEE 802.11g. The unique dual capabilities of data communication and ranging further expand the application possibilities for UWB [3], [15]. The current major commercial application of UWB is indoor home networking, although there are other applications, such as radio frequency identification (RFID), imaging, and vehicular radar systems.

High data rate wireless personal area networks (WPANs) are the main focus of many companies and the IEEE 802.15.3a standardization committee. WPANs will virtually eliminate all wires from the computers to peripherals, such as monitors, printers, cameras, PDAs or any other device. WPANs will also create a new set of applications and devices. These peripheral devices will communicate with each other through a wireless UWB network in a similar manner to current high-speed USB devices.

The UWB has high potential to be applied to various applications. One of the good examples is employing the UWB to apply test patterns into a fabricated chip through power lines [45], [46]. Due to the low radiation power level of the UWB signal, which is comparable to background noise, UWB signals applied to power lines do not incur significant performance degradation of normal chip operation.

Another area of UWB application is the RFID market, which in turn has many applications. One such application is the use of RFID as a tracking device in offices, hospitals, stores, etc. for locating and tracking inventory. RFID can also be applied to personnel identification, which could be used to identify an employee or to grant access to certain areas by opening doors. Yet another application is the replacement of bar codes. In bar code scanning, the bar code must be visually accessible by the reader, which complicates the scanning process for many applications. The use of the RFID would eliminate this problem since there is no need of visual contact, but only a need for the reader to be within a certain proximity. In the case of groceries, RFID could replace the
bar code; and at home, this same RFID could even inform a microwave oven of the required time and power to cook the food.
Chapter 3: Circuit-Level Implementation – CMOS Low Noise Amplifier Design for Ultra Wideband

3.1 Introduction

The low noise amplifier (LNA) is the most critical block for the receiver’s signal chain in any communication system, because it dominates the overall noise figure of the received signal. There are three important issues in LNA design for UWB applications. First is the wideband impedance matching for both maximal power transfer and optimal noise characteristic. Second is low power implementation with high power gain. According to the DS-UWB proposal for 802.15.3a [23], the target performance of our proposed LNA is listed in Table 3.1, which supports the direct-conversion DS-UWB transceiver architecture shown in Figure 3.1. Since one of the biggest advantages of UWB systems is the low-power and low-cost implementation, the LNA should be able to operate at low supply voltage, and occupy as small an area as possible. The third issue is gain flatness to avoid any signal distortion over such a wide bandwidth.
Figure 3.1: Direct-conversion DS-UWB transceiver architecture

Table 3.1: Target specification of UWB LNA

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency range with 1dB gain flatness</td>
<td>3 ~ 5 GHz</td>
</tr>
<tr>
<td>Power gain (S21)</td>
<td>&gt; 15 dB</td>
</tr>
<tr>
<td>Return loss (S11 and S22)</td>
<td>&lt; -10 dB</td>
</tr>
<tr>
<td>Noise figure (NF)</td>
<td>&lt; 3 dB</td>
</tr>
<tr>
<td>Input referred third order intercept point (IIP3)</td>
<td>&gt; -23 dBm</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>&lt; 18 mW</td>
</tr>
</tbody>
</table>

In terms of wideband impedance matching, the most popular methods are feedback topology, the distributed impedance matching method, bandpass filter (BPF) configuration matching network, and common-gate topology. Each method has advantages and disadvantages, so it is difficult to choose one method for UWB LNA.
design. Feedback topology, for example, has good noise and impedance matching performance, but negative feedback degrades the achievable power gain. BPF configuration matching achieves high power gain with superior impedance matching performance in addition to great frequency selection characteristics. On the downside, additional passive components required for filter implementation in the input matching network increases the noise figure. Distributed impedance matching method is perhaps the easiest way to achieve wideband matching by using multiple narrowband LNAs at the cost of large area. Common-gate topology is often not considered due to limited noise figure and power gain.

In this chapter, we will introduce two UWB LNA implementation methods; one is with improved BPF matching method as presented by the author in [25], and another employs a unique matching method, which utilizes both feedback, and BPF matching method, as presented by the author in [26]. The proposed UWB LNA is applicable not only to carrier-based UWB systems, such as MB-OFDM and DS-CDMA, but also to impulse-based UWB systems, and even digital UWB receiver as proposed in Chapter 4. Our research addresses a systematic approach for RF CMOS implementation in terms of an optimal noise performance and a wideband impedance matching. The ultimate goal is to accelerate CMOS design cycles for UWB systems. Our LNA is targeted to the 3 GHz ~ 5 GHz frequency range as given in Table 3.1. The bandwidth of 3 GHz to 5 GHz is the lower frequency range suggested by both MB-OFDM [24] and DS-UWB [23] for initial implementation purposes in current technologies.
3.2 Motivation

Whenever a new communication technique is introduced, the trend of circuit implementation is to move from high-performance to low-cost solutions. Since the FCC allocated spectrum for UWB applications, researchers and engineers have witnessed such a trend. The hot issues during the infancy of a new technology are verifying its usefulness and gathering enough market interest for a long life, so engineers concentrate on physical system implementation with more plausible fabrication technologies. In the case of UWB, these technologies were SiGe and GaAs, rather than CMOS, because the time-to-introduction was more critical than the time-to-market. However, after exploring the possibilities for commercial implementation, CMOS arises as the technology of choice to satisfy the low-cost demands of the market.

The major difficulties of RF CMOS circuit implementation are its relatively lower unity-gain-frequency and poor noise performance. Since these difficulties have discouraged designers from implementing RF devices at UWB frequencies, a much larger challenge is the lack of systematic design procedures for RF CMOS circuit implementation. Recent research in UWB CMOS low noise amplifier (LNA) design can be found in [27], and [28], but each encounters challenges due the inherent limits of CMOS. The LNA introduced in [27] employs a Chebyshev filter for input matching and a source follower for output matching. Though this LNA is a low power implementation, it provides a relatively low power gain of 10 dB, and its noise figure (NF) is also as high as 9dB in the upper UWB frequency ranges. Another general approach for wideband matching is reported in [28]. The distributed amplifier technique guarantees reasonably good performance in matching and power gain, but occupies more space and consumes high power due to the multiple stages. For these reasons, RFIC engineers are still demanding UWB LNAs with a lower noise figure, a wider supporting bandwidth, and a higher power gain with limited supply power and the proposed LNAs in this dissertation are focused on these demands.
### 3.3 CMOS UWB LNA Design Strategies

In general, it is very difficult to establish a systematic method for LNA design that satisfies low noise factor, impedance matching, and high gain all simultaneously. The major difficulty comes from the fact that the optimal source impedance for optimal noise likely does not coincide with the matching condition for maximum power delivery. So it is very important to confirm initial design decisions of the circuit parameters, even though the two matching conditions are not completely correlated. Also, over-simplified circuit models force a trial-and-error strategy for optimizing the circuit. Therefore, accurate circuit evaluation is required to avoid the tedious *Spice monkey business* in the circuit optimization design stage.

The overall LNA design strategy including the input and output impedance matching network is shown in Figure 3.2. The two proposed LNAs are both based on a source degenerative topology and cascode topology, which are widely used for narrowband LNAs. Note that the available power gain in source degenerative topology increases as the size of $L_s$ in Figure 3.2 decreases by reducing the negative feedback effect.

![Figure 3.2: General LNA design strategy with source degenerative topology](image)
The goal of this strategy is to make $Z_{opt}$ equal to $Z_{in\_eq}^\star$, so it can achieve both maximal power gain and optimal noise performance simultaneously. In the next section, a systematic procedure to achieve this goal will be explained.
3.4 Transistor Sizing and Bias Condition

In this section, we will introduce a useful technique to determine the width of transistor and bias condition, such as transconductance $g_m$, bias current $I_{DS}$, and effective voltage $V_{eff}$ (also referred to as overdrive voltage). The technique is applicable for the two proposed LNA architectures.

Since the size of a transistor and the bias condition determine power dissipation, it is often recommended to decide them with a certain power budget. However, we should evaluate the size of a transistor versus the bias condition carefully, because they are also related to impedance seen by the input gate (at gate of $M_1$). Thus, the best choice is to determine the size and bias condition so as to satisfy both impedance matching and noise matching with limited bias current. In fact, there is limited technical freedom for this choice. According to the MOSFET noise analysis [refer to Appendix C], the generator (sometimes driving source) admittance for optimal noise performance is shown in (3.1) and (3.2).

$$G_{opt} = \alpha \omega C_{gs} \sqrt{\frac{\delta}{5\gamma}} \left(1-|c|^2\right)$$  \hspace{1cm} (3.1)

$$B_{opt} = -\omega C_{gs} \left(1+\alpha |c| \sqrt{\frac{\delta}{5\gamma}}\right)$$  \hspace{1cm} (3.2)

where $\alpha = g_m/g_{ds0}$, and noise parameters $c$, $\delta$, and $\gamma$. Please refer to Appendix C for further explanation of these parameters.

For the sake of simplicity, we ignore the correlation of noise so that $c$ has to be 0. Therefore, we can simplify (3.1) and (3.2) as below,

$$R_{opt} \approx \frac{1}{\alpha \omega C_{gs}} \sqrt[5]{\frac{\gamma}{\delta}}$$  \hspace{1cm} (3.3)

$$X_{opt} \approx \frac{1}{\omega C_{gs}}$$  \hspace{1cm} (3.4)

Furthermore, (3.4) can be modified to (3.5) by taking the source degenerative inductor into account.
Note that expressions (3.3) to (3.5) represent real and imaginary terms of impedance, unlike the expressions (3.1) and (3.2) for admittance.

From the above relationship, it is noticed that the imaginary term of noise optimal generator impedance is inversely proportional to gate-source capacitance, which is always positive so that noise matching can be achieved with inductive generator impedance. However, increasing $L_s$ at the cost of gain can reduce the inductive term of generator impedance. According to the above observation, it is clear that optimal noise condition and maximum power delivery are obtained simultaneously when $Z_{\text{opt}} = Z_{\text{in\_eq}}^*$, where $Z_{\text{in\_eq}}$ is the equivalent input impedance seen by input gate of amplifying transistor as described below,

$$
Z_{\text{in\_eq}} = R_{\text{in\_eq}} + jX_{\text{in\_eq}} = \frac{g_m L_s}{C_{gs}} + j \left( \omega L_s - \frac{1}{\omega C_{gs}} \right)
$$

(3.6)

Note that the equivalent input impedance is for the case of a source degenerative topology [refer to Appendix D].

However, it is not easy to maintain both $Z_{\text{opt}}$ and $Z_{\text{in\_eq}}^*$ close to the values over a wide frequency range. Thus we define the inequality as shown in (3.7) to ensure higher gain. From (2.6), we can observe that the real term of $Z_{\text{in\_eq}}$ is proportional to $L_s$. Smaller resistive input impedance seen by the gate leads to higher gain due to reduction in the negative feedback. As a result, the real part of $Z_{\text{in\_eq}}$ should be smaller than $Z_s$. However, since $Z_{\text{opt}}$ should be close to $Z_{\text{in\_eq}}$, the real part of $Z_{\text{opt}}$ also should be smaller than $Z_s$. For improving the power gain further, the real part of $Z_{\text{in\_eq}}$ is chosen to be smaller than the real part of $Z_{\text{opt}}$.

$$
R_{\text{in\_eq}} \leq R_{\text{opt}} \leq Z_s
$$

(3.7)

where $Z_s$ is the source impedance, $R_{\text{in\_eq}}$ and $R_{\text{opt}}$ are real parts of $Z_{\text{in\_eq}}$ and $Z_{\text{opt}}$ respectively.
Since the reactance term of $Z_{opt}$ and $Z_{in\_eq}^*$ are almost always matched according to (3.3), (3.4) and (3.6), the inequality (3.7) will force the plot of $Z_{in\_eq}$ to be positioned to the outer side of the plot of $Z_{opt}$ in the Smith chart until the frequency exceeds the frequency range of interest.

As mentioned earlier, we determine the bias condition with limited power budget. For simplicity, we ignore the overlapped channel length $L_{ov}$, and define $g_m$ and $C_{gs}$ as shown in (3.8) and (3.9). Using (3.6), (3.7), (3.8), and (3.9), the effective voltage $V_{eff}$ is expressed in (3.10) [refer to Appendix A].

$$g_m = \mu_n \frac{W}{L} \frac{C_{ox}}{V_{eff}} \quad (3.8)$$

$$C_{gs} = \frac{2}{3} \frac{WLC_{ox}}{V_{eff}} \quad (3.9)$$

$$V_{eff} \leq \frac{2Z_{L}L^2}{3L_n \mu_n} \quad (3.10)$$

Note that minimum channel length $L$ is assumed in (3.10). Once we determine the maximum effective voltage $V_{eff\_max}$ as implied in (3.10), we can specify the minimum $g_m$ as $g_m \geq 2I_{DS}/V_{eff\_max}$.

Assuming $\gamma \approx 2$, $\delta \approx 4$ [refer to Appendix C], and $\alpha \approx 5$ because $g_{ds} \approx 0.2g_m$ in the active region, (3.3) can be further simplified as

$$R_{opt} \approx \frac{1}{\sqrt{10}\omega C_{gs}} \quad (3.11)$$

Finally, we determine a minimum channel width $W$ as (3.12) based on (3.7), (3.9), and (3.11).

$$W \geq \frac{3}{2\sqrt{10}\omega Z_{s}L C_{ox}} \quad (3.12)$$

Again, minimum channel length is assumed in (3.12). Since the parameters are defined in certain range, they must be optimized later. Based on the parameters selected so far, $Z_{opt}$ and $Z_{in\_eq}$ are shown in Figure 3.3 over the frequency range of 100MHz to 20GHz, and one can notice that $Z_{in\_eq}^*$ is almost matched to $Z_{opt}$, and that the plot of
$Z_{\text{in, eq}}$ is positioned outside the circle of $Z_{\text{opt}}$ in the Smith chart up to 6GHz, which exceeds our frequency range of interest.

The obtained conditions so far should be applied to $M_1$ in Figure 3.2. Hereafter, any circuit parameters belonging to $M_1$ and $M_2$ will be distinguished by subscript 1 and 2 at the end of the parameter notations respectively.
3.5 **Type I UWB Low Noise Amplifier**

3.5.1 **Overall Architecture**

Figure 3.4 shows the overall LNA schematic of our Type I design, including the input and output impedance matching networks. The proposed Type I LNA is based on the BPF matching method, and it can achieve 15.5 dB power gain with only a single stage amplifier while satisfying input and output impedance matching constraints. Though the schematic shows six inductors, only four inductors are fabricated as shown in Figure 3.5, which is a microphotograph of the fabricated LNA. The remaining two inductors, $L_s$ and $L_{series\_in}$, are very small so they are implemented by bonding wires.

![Figure 3.4: Overall schematic of Type I LNA](image)
3.5.2 Input Impedance Matching

For wideband impedance matching, we have to transform the source impedance $Z_s$ (sometimes referred to as the generator impedance), which is normally a real 50Ω, to the conjugate of the circuit input impedance, $Z_{in_{eq}}^*$ over the frequency range of interest. Let us start with the equivalent input circuit of the source degenerative topology as explained in Appendix D. In general, the equivalent input circuit of the source degenerative topology is considered as a series connection of an inductor, a capacitor, and a resistor as shown in Figure 3.6. However the resistance, $R_{in_{eq}}$ is selected to be smaller than the generator impedance as explained (3.7), so a $(1:n)$ impedance inverting is required.
One can choose any types of bandpass filter for their uses, such as Butterworth, Chebyshev, and Bessel. The required parameters for a lowpass filter synthesis are listed in Table 3.2 [91], [92], [93].

Table 3.2: Element values for lowpass prototype filter synthesis

<table>
<thead>
<tr>
<th>Order</th>
<th>Butterworth</th>
<th>Chebyshev</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$\varepsilon_1$</td>
<td>$\varepsilon_2$</td>
</tr>
<tr>
<td>1</td>
<td>2.000</td>
<td>1.000</td>
</tr>
<tr>
<td>2</td>
<td>1.414</td>
<td>1.414</td>
</tr>
<tr>
<td>3</td>
<td>1.000</td>
<td>2.000</td>
</tr>
<tr>
<td>4</td>
<td>0.7654</td>
<td>1.848</td>
</tr>
</tbody>
</table>

First, we derive a 2\textsuperscript{nd} order Butterworth type BPF from a low pass filter prototype terminated with $R_{\text{in}_{eq}}$ at both ends as illustrated in Figure 3.7.
The component values of the LPF prototype are determined by

\[ L_{LPF} = \frac{\varepsilon_1 R_{in\_eq}}{\omega_c} \]  \hspace{2cm} (3.13)

\[ C_{LPF} = \frac{\varepsilon_2}{R_{in\_eq} \omega_c} \]  \hspace{2cm} (3.14)

where \( \varepsilon_1 \) and \( \varepsilon_2 \) are both \( 1.414 = \sqrt{2} \) from Table 3.2, and for BPF transformation,

\[ L_{BPF1} = r L_{LPF} \]  \hspace{2cm} (3.15)

\[ C_{BPF1} = \frac{1}{\omega_c^2 L_{BPF1}} \]  \hspace{2cm} (3.16)

\[ L_{BPF2} = \frac{1}{\omega_c^2 C_{BPF2}} \]  \hspace{2cm} (3.17)

\[ C_{BPF2} = r C_{LPF} \]  \hspace{2cm} (3.18)

where \( \omega_c \) is the center frequency of the frequency range of interest defined as \( \omega_L + (\omega_H - \omega_L)/2 = \omega_L + BW/2 \), and \( BW \) is the bandwidth required. Note that \( \omega_H \) and \( \omega_L \) are the upper and lower cut-off frequencies respectively. The symbol \( r \) is defined by \( \omega_c / BW \). Since we are interested in signal reflection, not 3 dB bandwidth, the center frequency is chosen as \( \omega_c \), unlike typical bandpass filter design [29], which defines \( \omega_c = \sqrt{\omega_H \omega_L} \). The BPF synthesized with the newly defined center frequency \( \omega_c \) has minimum power reflection at \( \omega_c \) so that it satisfies the impedance matching constraints over the entire bandwidth of interest. The effect of the modified \( \omega_c \) choice strategy is shown in Figure 3.8. As shown in Figure 3.8(a), using the typical choice of \( \omega_c \) for BPF synthesis, power reflection reaches its minimum value at a frequency lower than 4GHz, and exceeds –10dB at 5GHz. However, as shown in Figure 3.8(b), using the newly defined \( \omega_c \), power reflection reaches its minimum value at 4GHz, and remains lower than –10dB from 3 to 5 GHz.
Figure 3.8: Effect of different choice of $\omega_c$

Note that $C_{in\_eq}$ and $L_{in\_eq}$ are equivalent to $C_{gs}$ and $L_s + L_g$ respectively, where $L_g$ is the extra inductor connected to the gate. BPF components $C_{BPF1}$ and $L_{BPF1}$ must be equivalent to $C_{in\_eq}$ and $L_{in\_eq}$. Furthermore, expressions (3.13), (3.15) and (3.16) determines the choice of $L_s$ as depicted in (3.19).
\[ L_s \geq \frac{BW_{\text{min}}}{\sqrt{2\omega_c^2 g_m}} \]  

(3.19)

where \( BW_{\text{min}} \) is the minimum required bandwidth. Note that (3.19) assumes an input equivalent resistive term \( R_{\text{in, eq}} \) defined by \( R_{\text{in, eq}} = \frac{g_m L_s}{C_{gs}} \). Thus, once the bias condition is selected, it also guides the choice of the degenerative source inductor \( L_s \), which is recommended to be as small as possible for higher gain at the cost of linearity as explained in Appendix D.

By definition, the power loss around the cut-off frequency is about 3dB. However, 3dB power loss is unacceptable in terms of power reflection and hence excessive bandwidth is considered to guarantee an S11 lower than \(-10\)dB over the frequency range of interest. For example, if the frequency range of interest is 3 GHz to 5 GHz, a 3dB bandwidth of 2 GHz \( \sim \) 6 GHz with 4 GHz center frequency should be considered to achieve less than -10dB power reflection in the 3 GHz to 5 GHz frequency band.

Once we design a bandpass filter with \( R_{\text{in, eq}} \) terminated at both the ends, \( R_{\text{in, eq}} \) at the input side should be transferred to \( Z_s \), if it is not equal to \( Z_s \). An impedance inverter is applicable in order to transfer the resistive termination \( R_{\text{in, eq}} \) to the generator impedance \( Z_s \) as shown in Figure 3.10.

Figure 3.9 shows four impedance inverters, which are useful as an alternative implementation of a transformer [47], [90]. Note that one of the reactances is negative and must be combined in passive network with a reactance of at least equal positive value. Insertion of the inverter can be made at any convenient place by considering the compensation of the negative reactance.
As $R_{in\_eq}$ is smaller than $Z_s$, the inverting factor $n$ in Figure 3.10 is less than unity. Therefore, the inductance $\frac{n-1}{n} L_{BPF2}$, which is connected to $L_{in\_eq}$ in series, is a negative value resulting in a smaller overall inductance when combined with the positive inductance of $L_{in\_eq}$. In general, $R_{in\_eq}$ tends to be close to $Z_s$, so $n$ is slightly less than unity according to the definition $n = \sqrt{\frac{R_{in\_eq}}{Z_s}}$. As a result, the other series inductor, $\left(\frac{1-n}{n^2}\right) L_{BPF2}$, becomes small enough to be implemented either by proper routing in layout or by a bonding wire in packaged product.
3.5.3 Output Impedance Matching

Once we complete an input impedance matching, gain flatness becomes reliant on output impedance matching. One common technique employs a source follower stage following a major amplifying stage as shown in Figure 3.11. The source follower provides an easy output matching method because the output impedance is simply defined by \( 1/g_{ms} \), where \( g_{ms} \) is the gate-source transconductance of the source follower.

![Figure 3.11: Source follower for output buffer](image)

However, since the gain of a source follower is always less than 0\(dB\), it decreases overall gain increases noise figure and degrades linearity. Furthermore, even though the extra buffer stage provides less than unity gain, it consumes extra power and occupies extra space. Also, a multiple stage amplifier design requires reasonable conjugate impedance matching between stages, further complicating the design procedure.

For the above reasons, a single stage amplifier design, providing both input and output impedance matching, is more desirable. The single stage increases power efficiency by avoiding miscellaneous power waste through the intermediate matching between stages. Further, the single stage increases overall gain, since it does not have to overcome the gain loss incurred by the source follower. Finally, the single stage implementation decreases supply voltage through its improved power efficiency, and it can do so even under a limited DC bias current.
We introduce two practical output impedance matching methods suitable for UWB LNA design. The first approach is a general matching method similar to the input impedance matching method explained previously, while the second supports mid-range wideband applications, such as lower band UWB applications occupying the 3GHz to 5GHz frequency range. The mid-range wideband matching method relaxes the complexity of a matching network allowing a smaller circuit size.

### 3.5.3.1 Bandpass Filter Output Matching Method

First, we need to derive an equivalent output circuit with an RF choke inductor (RFC) as in Figure 3.12. Note that $R_{out}$ is equal to $g_{m2}R_{ds2}R_{ds1}$ in a cascode topology, where $R_{ds1}$ is the output impedance of M1. Recall that larger output impedance effectively leads to larger gain, thus larger $R_{ds2}$ and $R_{ds1}$ are desired. Also, note that the cascode transistor provides high isolation between input and output and contributes output impedance n the amount of $R_{ds2}$. $C_{out}$ is mostly junction capacitance at drain of M2 [refer to Appendix A], and it can be reduced by multi-fingering.

![Figure 3.12: Equivalent output circuit](image)

The approach to develop the output matching network is to transfer the large output resistive impedance to $Z_{out}$ (normally 50 Ω) after building a bandpass filter as explained in the previous section. Note that the ratio $n$ is defined as $n^2:1 = R_{out}:Z_{out}$.

We deploy an inductor, RFC and capacitors $C_{out}$ and $C_{ext}$ for BPF configuration with $R_{out}$ terminated at both ends and transfer $R_{out}$ to $Z_{out}$, which is normally 50Ω. Note that $C_{ext}$ is an extra capacitor to provide proper capacitance in addition to $C_{out}$ for the BPF configuration. The only restriction of the matching network development is that $C_{ext}$
should be large enough to cancel the negative capacitance extracted by the impedance inverting represented as $(1-n)C_{BPFOutl}$ in Figure 3.13. Note that $n$ is greater than unity in this case because $R_{out}$ is much larger than $Z_{out}$ in most cases, resulting in a negative capacitance value of $(1-n)C_{BPFOutl}$.

From (3.14) and (3.18),

$$C_{BPFOut2} = \frac{r^2 2}{\sqrt{2} \omega_c r R_{out}}$$

(3.20)

and from (3.13), (3.15), and (3.16),

$$C_{BPFOut1} = \frac{1}{\sqrt{2} \omega_c r R_{out}}$$

(3.21)

Finally, since $C_{ext}$ should cancel out the synthesized capacitance, $(1-n)C_{BPFOutl}$ after impedance inverting (Case b) in Figure 3.9,

$$C_{ext} + (1-n)C_{BPFOutl} = C_{BPFOut2} - C_{out} + (1-n)C_{BPFOut1} \geq 0$$

(3.22)

Thus, as a result, we can derive the maximum value of $C_{out}$ as

$$C_{out} \leq \frac{2r^2 - n + 1}{\sqrt{2} r \omega_c R_{out}}$$

(3.23)

Equation (3.23) implies that larger $R_{out}$ requires smaller $M_2$ in order to obtain smaller $C_{out}$, since larger $R_{out}$ generates not only larger denominator in (3.23), but also a larger negative term $n$ in the numerator. However, the restriction given in (3.23) cannot be satisfied sometimes due to minimum size requirement of $M_2$ to drive enough DC bias current in an amplifying transistor. It is also worth mentioning that the series inductor expressed as $\frac{L_{BPFOut1}}{n^2}$ is considerably small enough to allow utilization of a bonding wire as an inductor instead of an integrated inductor. Figure 3.2 illustrates the design procedure of the general wideband output impedance matching network development.
3.5.3.2 Impedance Mapping Output Matching Method

The second method overcomes the size restriction of $M_2$ in (3.23), but it is applicable only to mid-range wide bandwidth, which is mainly determined by the quality factor of the equivalent output parallel $RCL$ circuit. To be considered mid-range wide bandwidth, the qualify factor of the equivalent parallel $RLC$ circuit should be lower than unity for 3 to 5 GHz frequency band.

The second method starts with the assumption that the output impedance of the cascode stage $M_2$ can be approximated to only its resistive term, $R_{out}$, around a resonant frequency of the equivalent output circuit. The basic approach is to transfer the $R_{out}$ at the resonant frequency to the load impedance $Z_{out}$ through a bandpass filter as in the previous method. However, the simple impedance transformation of $R_{out}$ to $Z_{out}$ at the resonant frequency with bandpass filtering does not provide the required wideband matching. Therefore instead of mapping $R_{out}$ to $Z_{out}$, we adjust the value $R_{out\_eq}$, which is slightly smaller than $R_{out}$, in order to increase the amount of bandwidth we cover with matching.
Conceptually, we map two strategic impedances that each lie at the frequencies between the center frequency of the band of interest and the two stop frequencies to $Z_{out}$. This mapping covers a wider bandwidth with reasonable impedance matching, and Figure 3.14 depicts the concept.
Figure 3.14: Impedance mapping for output matching
According to the mapped plot in Figure 3.14(b), the matching is not perfect. However, the relaxed matching is adequate, as the plot creates a circle around the center point in the Smith chart where the perfectly matching points should be positioned. With the proper arrangement as explained in this section, the mapped impedance points are within the maximum required standing wave ratio (SWR) circle, which is normally 1.5 for reasonable matching, as indicated in Figure 3.14(b). In general, we select two impedances at the frequencies between the center frequency of $\omega_c$, and the lower/upper stop frequency of $\omega_L / \omega_H$ and they are $\omega_1 = (\omega_L + \omega_c)/2$ and $\omega_2 = (\omega_H + \omega_c)/2$.

After developing the bandpass filter and the impedance inverter, a new RFC is derived as the parallel connection of the initial load inductor of RFC$_{init}$, which resonates at the center frequency $\omega_c$ with $C_{out}$, and the filter constructing shunt inductor, $L_{BPFout2}$. Figure 3.15 shows the new RFC. Note that the parallel combination of RFC$_{init}$ and $L_{BPFout2}$ synthesizes a new smaller RFC resulting in smaller size in area.

Note that $C_{BPFout2} + (1 - n)C_{BPFout1} = 0$ is preferable to reduce the number of capacitors, since this condition allows the capacitors to be omitted from Figure 3.15.
3.6 Type II UWB Low Noise Amplifier

3.6.1 Motivation

The design methodology of the Type I LNA is suitable for a stand-alone, packaged LNA chip with reasonable performance. However, there are some challenges we need to address for used in a fully integrated UWB transceiver chip. Namely, the Type I LNA utilizes two bonding wires as part of the input impedance matching network, and one is in the path of gate bias voltage supply as shown in Figure 3.16. An internally integrated bias voltage generator in the fully integrated transceiver will not allow the use of the bonding wire in the bias voltage supply path. For this reason, we either have to fabricate all required inductors, or reduce the number of inductors.

![Figure 3.16: Bonding wire usage](image)

The Type II LNA introduced in this section is more feasible for a fully integrated transceiver design, and it performs better by reducing the number of passive components at the input.
As mentioned earlier, accurate circuit evaluation is essential to reduce any time-consuming efforts for circuit optimization. Thus, we evaluate accurate modeling of the Miller effect in source degenerative topology with a cascode device. This section presents a detailed methodology for utilizing the Miller effect in implementing an input matching network.

### 3.6.2 Overall Architecture

The *Type II* LNA shown in Figure 3.17 employs a simple architecture for its input matching, and it is similar to conventional narrowband LNA designs [30]. The difference between the proposed wideband matching and classical narrowband matching is that the proposed method uses the Miller effect, while others try to minimize or ignore the Miller effect.

![Figure 3.17: Overall architecture of Type II LNA](image)

As introduced earlier, the proposed input impedance matching method takes advantage of both feedback analysis and a BPF configuration for minimization of the number of passive components, for optimization of power, and for noise matching. Also, the *Type II* UWB LNA architecture does not incorporate a source follower for output
matching like the Type I LNA, so the Type II LNA can enhance signal linearity even for very low supply power.

The microphotograph of the fabricated chip is shown in Figure 3.18, and its die size is 740 $\mu m \times 850 \mu m$.

3.6.3 Miller Effect in Cascode Topology

The Miller effect implies that the effective capacitance is increased by negative voltage gain between the input and output [48], [49]. However, since the input impedance of the cascode device M2 is capacitive, the voltage gain is high at low frequency and low at high frequency. This implies the effective Miller capacitance will be high in low
frequency and low in high frequency. Therefore, the Miller effect creates not only a single capacitor, but also an inductor in parallel with the Miller capacitor.

The input impedance $Z_{\text{Load}}$ of the cascode device $M_2$ seen at the source of $M_2$ is described as (3.24).

$$Z_{\text{Load}} = \frac{R_{ds2} + Z_L}{1 + g_{m2}R_{ds2} + sC_{gs2} \left( R_{ds2} + Z_L \right)}$$

(3.24)

$Z_L$ is the output load connected at the drain of $M_2$, and this is assumed as pure resistor over the frequency of interest if the output has perfectly matched to $Z_{\text{out}}$, which is normally 50 $\Omega$.

The load impedance of the cascode device, therefore, can be expressed as an $R$ and $C$ parallel circuit as shown in Figure 3.19, and its values are

$$C_{\text{Load}} = C_{gs2}$$

(3.25)

$$R_{\text{Load}} = \frac{R_{ds2} + Z_L}{1 + g_{m2}R_{ds2}}$$

(3.26)

Figure 3.19: Input impedance of cascode device $M_2$

The resistance term of the cascode load is equal to $1/g_{m2}$, when $R_{ds2}$ is infinite. Note that the $R_{ds2}$ is relatively large for a low power design due to the relation of $R_{ds} = \frac{1}{\lambda I_{DS}}$, where $\lambda$ is the depletion length coefficient (channel length modulation), and $I_{DS}$ is the bias DC current, which is small for a low power design.
The effective transconductance for a source degenerative topology can be obtained as

\[ G_m = \frac{g_{m1}}{1 + g_{m1}L_s s + C_{g_{m1}}(L_s s)^2} \]  

(3.27)

Thus, the overall open voltage gain \( A_{vo} \) is

\[ A_{vo} = -G_m Z_{Load} \]

\[ = \frac{-g_{m1}(R_{d_{s2}} + Z_L)}{(1 + g_{m1}L_s s + C_{g_{m1}}(L_s s)^2)(1 + g_{m2}R_{d_{s2}} + C_{g_{s2}}(R_{d_{s2}} + Z_L)s)} \]  

(3.28)

According to the non-constant open voltage gain between the gate and drain of \( M_1 \), the Miller capacitor is not a simple capacitor any more, rather an \( RLC \) combination circuit.

The Miller capacitance \( C_{mil} \) is

\[ C_{mil} = (1 - A_{vo})C_{gd1} \]

\[ = \left( 1 + \frac{g_{m1}(R_{d_{s2}} + Z_L)}{(1 + g_{m1}L_s s + C_{g_{m1}}(L_s s)^2)(1 + g_{m2}R_{d_{s2}} + C_{g_{s2}}(R_{d_{s2}} + Z_L)s)} \right) C_{gd1} \]  

(3.29)

Finally, the overall Miller impedance caused by the non-constant voltage gain is

\[ Z_{mil} = \frac{1}{sC_{mil}} \]

\[ \approx \frac{s^2 L_s (C_{g_{d1}}g_{m2} + C_{g_{s2}}g_{m1}) + s(C_{g_{s2}} + L_s g_{m1}g_{m2}) + g_{m2}}{s^3 C_{gd1} L_s (C_{g_{d1}}g_{m2} + C_{g_{s2}}g_{m1}) + s^2 C_{gd1} (C_{g_{s2}} + L_s g_{m1}g_{m2}) + sC_{gd1}(g_{m1} + g_{m2})} \]  

(3.30)

Note that non-dominant terms are eliminated for the sake of simplicity.

The impedance caused by the Miller effect, as illustrated in Figure 3.20, and the values of individual components are defined as

\[ C_{mil1} = \frac{C_{gd1}(g_{m1} + \alpha)}{\alpha} \]  

(3.31)

\[ C_{mil2} = \frac{C_{gd1}(g_{m1} + \alpha)}{g_{m1}} \]  

(3.32)
\[ L_{mil1} = \frac{L_s g_{m1} (C_{gr1} \alpha + C_{gr2} g_{m1})}{\alpha (g_{m1} + \alpha)} \quad (3.33) \]

\[ R_{mil1} = \frac{g_{m1} (C_{gr2} + L_s g_{m1} \alpha)}{C_{gd1} (g_{m1} + \alpha)^2} \quad (3.34) \]

where \( \alpha = 1/R_{\text{Load}} \).

Note that the resistive term \( R_{mil1} \) is related to the quality factor of the inductive term \( L_{mil1} \), and it is relatively small enough to be ignored.

Figure 3.20: Equivalent input circuit

Since the values of \( R_{\text{eff}}, C_{\text{eff}}, \) and \( L_{\text{eff}} \) in Figure 3.20 is not the same as the conventional AC equivalent input circuit of the source degenerative topology as explained in Appendix D, we will evaluate the accurate values of \( R_{\text{eff}}, C_{\text{eff}}, \) and \( L_{\text{eff}} \) in next section.
3.6.4 Modified Input Impedance by Feedback

Now, we re-evaluate the input impedance of the inductive degenerative topology, including Miller effect by capacitive negative feedback, so as to specify the values of $R_{eff}$, $C_{eff}$, and $L_{eff}$ in Figure 3.20.

The input impedance of the open RLC circuit is well known as

$$Z_{ino} = sL_s + \frac{1}{sC_{gs1}} + \frac{g_{m1}I_s}{C_{gs1}}$$

(3.35)

For details about (3.35), one can refer to Appendix D.

From feedback systems, we can obtain the modified input impedance of the feedback system as shown in Figure 3.21, and its expression is given in (3.36).

$$Z_{inc} = \frac{Z_{ino}(Z_f + Z_{load})}{Z_{ino}(1 + G_m) + Z_L + Z_f}$$

(3.36)

Note that the closed loop input impedance includes the Miller effect.

The feedback impedance $Z_f$ is $(1/sC_{gd1})$, which is the gate-to-drain capacitor. By using the effective transconductance and load impedance as obtained above, the overall expression of the input admittance $Y_{inc}$ of the closed loop circuit after simplification is
\[ Y_{inc} = Y_{mil} + \frac{1}{R_{eff} + sC_{eff} + \frac{1}{sL_{eff}}} \] (3.37)

where \( Y_{mil} \) is \( 1/Z_{mil} \), the admittance of the equivalent Miller load, which includes \( C_{mil1}, C_{mil2}, L_{mil1}, \) and \( R_{mil1} \) in Figure 3.20, and,

\[ R_{eff} = \frac{g_{m1}L_s}{C_{gs1}} \left( 1 + \frac{C_{gd1}R_{ds2} + 2C_{gr2}R_{ds2}}{g_{m1}L_s \left( 1 + g_{m2}R_{ds2} \right)} \right) \] (3.38)

\[ C_{eff} = C_{gs1} \] (3.39)

\[ L_{eff} = L_s + \beta \] (3.40)

where

\[ \beta = \frac{R_{ds2} + Z_L}{C_{gs1} \left( 1 + g_{m2}R_{ds2} \right)} \] (3.41)

and

\[ \chi = C_{gd1} \left( g_{m1} \left( L_s + g_{m2}L_sR_{ds2} \right) + C_{gr2} \left( R_{ds2} + Z_L \right) \right) + C_{gr2} \left( 2g_{m1} \left( L_s + g_{m2}L_sR_{ds2} \right) + C_{gr2} \left( R_{ds2} + Z_L \right) \right) \] (3.42)

Thus, we can see the original \( RLC \) series circuit given by (3.35) is modified by the feedback effect. The feedback effectively increases the inductive term \( L_{eff} \) and resistive term \( R_{eff} \) from the original open circuit input impedance \( Z_{ino} \).

For large \( R_{ds2} \), the equivalent circuit can be further simplified from (3.38) and (3.40) as

\[ R_{eff} \approx \frac{g_{m1}L_s}{C_{gs1}} \left( 1 + \frac{C_{gd1} + 2C_{gr2}}{g_{m2}} \right) \] (3.43)

\[ L_{eff} \approx L_s + \frac{C_{gd1}C_{gr2} + C_{gr2}^2 + C_{gd1}g_{m1}g_{m2}L_s + 2C_{gr2}g_{m1}g_{m2}L_s}{C_{gs1}g_{m2}^2} \] (3.44)

Therefore, the overall input impedance can be expressed as in Figure 3.20.

Note that \( C_{mil1} \) can be ignored at high frequency and that \( R_{mil1} \) also can be ignored due to its small value. Thus, the overall circuit can be considered as the combination
circuit of a parallel LC and a series LC circuit. The circuit also can be considered as a part of bandpass filter. In our Type II LNA, we could build a 3rd order Chebyshev bandpass filter over the target frequency range of interest by adding properly sized $L_g$ and $C_{in}$ as shown in Figure 3.20.

### 3.6.5 Input Impedance Matching Network Synthesis

According to the equivalent input circuit, which contains series RLC and parallel RLC circuit as shown in Figure 3.20, we consider a bandpass filter structure as an input impedance matching network as same as Type I LNA design. However, for Type II LNA, we derive a 3rd order Chebyshev type BPF from a low pass filter prototype terminated with $R_{eff}$ at both ends as illustrated in Figure 3.22 according to the required bandwidth and the obtained equivalent circuit,

![Diagram of equivalent circuits](image)

**Figure 3.22: Frequency transformation from LPF prototype to BPF**

From Table 3.2, the component values of the LPF prototype are determined by

$$L_{LPF1} = \frac{\varepsilon_1 R_{eff}}{\omega_c}$$  \hspace{1cm} (3.45)

$$C_{LPF2} = \frac{\varepsilon_2}{R_{eff} \omega_c}$$  \hspace{1cm} (3.46)

$$L_{LPF3} = \frac{\varepsilon_3 R_{eff}}{\omega_c}$$  \hspace{1cm} (3.47)

where $\varepsilon_1=0.6291$, $\varepsilon_2 = 0.9702$, and $\varepsilon_3=0.6291$, and for BPF transformation,

$$L_{BPF1} = rL_{LPF1}$$  \hspace{1cm} (3.48)
\[ C_{BPF1} = \frac{1}{\omega_c^2 L_{BPFF1}} \]  
(3.49)

\[ L_{BPFF2} = \frac{1}{\omega_c^2 C_{BPFF2}} \]  
(3.50)

\[ C_{BPFF2} = rC_{LPFF2} \]  
(3.51)

\[ L_{BPFF3} = rL_{LPFF3} \]  
(3.52)

\[ C_{BPFF3} = \frac{1}{\omega_c^2 L_{BPFF3}} \]  
(3.53)

Note that BPF components \( C_{BPFF1} \) and \( L_{BPFF1} \) must be equivalent to \( C_{eff} \) and \( L_{eff} \). Furthermore, expressions (3.45), (3.48), and (3.49) determine the choice of \( L_{eff} \) as depicted in (3.54).

\[
L_{eff} \geq \frac{BW_{\text{min}}}{\varepsilon C_{gs}} \]  
(3.54)

where \( BW_{\text{min}} \) is the minimum required bandwidth. Note that (3.54) assumes an input equivalent resistive term \( R_{eff} \) defined by \( R_{eff} = g_m L_s / C_{gs} \), with ignorance of the increasing factor \( \frac{C_{gs1} + 2C_{gs2}}{g_{m2}} \) in (3.43). Thus, once the bias condition is selected, it also guides the choice of the degenerative source inductor \( L_s \), which dominates the value of \( L_{eff} \). Also, it is recommended to be as small as possible for higher gain at the cost of linearity as explained in Appendix D.

In order to obtain proper components value for the input impedance matching network as defined in (3.48) ~ (3.53), we need to observe the relationship between components values. From (3.31), (3.33), (3.50), and (3.51), we can derive the relationship as below.

\[
L_{BPFF2}C_{BPFF2} = L_{mil1}C_{mil2} = \frac{1}{\omega_c^2} \]  
(3.55)

\[
= L_s C_{gs1} + \frac{L_s \alpha C_{gs2} g_{m1}}{\alpha} \]
In (3.55), we have a controllability of $C_{gs2}$, which is determined by size of the cascode device $M_2$, once we determine the bias condition and the size of $M_1$ according to the noise optimum condition. In the same manner, from (3.44), (3.48), and (3.49), we also can establish the relationship between $L_{eff}$ and $C_{eff}$ as below.

$$L_{BPF1} C_{BPF1} = L_{eff} C_{eff} = L_{eff} C_{gs1} = \frac{1}{\omega_c^2}$$

$$= L_s C_{gs1} + \frac{C_{gd1} C_{gs2} + C_{gs2}^2 + C_{gd1} g_{m1} g_{m2} L_s + 2 C_{gs2}}{g_{m2}}$$

(3.56)

In (3.56), we can satisfy the relationship by adjusting $C_{gd1}$ and $g_{m2}$. Note that $C_{gd1}$ can be controlled by proper layout scheme or with an extra capacitor if necessary.

### 3.6.6 Output Impedance Matching

We employ the same basic method for output impedance matching as for the Type I LNA. However, since we observe some instability of the Type I LNA during measurement, we have inserted $R_L$ in Figure 3.17 to decrease the quality factor in the $LC$ tank to prevent possible oscillation. We will discuss the unwanted local oscillation of the Type I LNA in the next section.
3.7 Layout Techniques for Isolation

Unlike digital design, which uses a heavily doped bulk to address latch-up, most silicon-based RF chips are fabricated in a process that uses a lightly doped bulk. A lightly doped substrate provides high resistance resulting in high isolation. However, the isolation problem is still a concern for sensitive circuits, such as LNAs and mixers. A direct-conversion receiver architecture suffers from LO leakage, and this causes a DC offset. Thus, the isolation problem (basically a substrate coupling problem) needs to be carefully addressed for a direct-conversion architecture.

In fabrication process technology, a triple well (also referred to as a “deep n-well”) is a common option for CMOS. Figure 3.23 shows a cross-section of a triple well compared to regular CMOS process for a digital circuit. The triple well isolates the n-type devices that would be normally fabricated over a p-substrate.

![Figure 3.23: Triple well technique][50]

In the following sections, we will discuss effective methods to increase isolation besides the triple-well process. These methods will ultimately improve overall noise characteristics.

3.7.1 Shielding

One of the most effective layout schemes is to isolate sensitive signal lines and passive components from noisy circuits by shielding. Shielding often prevents crosstalk between sensitive signal lines or passive components and a noisy area in the vicinity by breaking lateral and fringing electric fields.
In the case when a quiet and a noisy signal lines cross, an extra layer in between the two lines can form a shield. The extra layer should be tied to a quiet power supply, which is normally ground as shown in Figure 3.24. A shield also can be in the form of an n-well or in the form of diffusion layers underneath the passive components as shown in Figure 3.25, which illustrates a cross-section of a poly-poly capacitor used for sensitive circuitry. As shown in Figure 3.25, the n-well beneath the component provides shielding. Note that in this case, the n-well is connected to VDD.

Figure 3.24: Isolating ground shield between two signal lines
3.7.2 Guard Ring

Guard rings around a noise source provide a low-resistance path to AC ground for the noise and help minimize the amount of noise injected into the substrate. The guard ring mechanism is shown in Figure 3.26.

Figure 3.26: Guard ring mechanism

Figure 3.27 and Figure 3.28 show guard rings for individual components. Note that the guard rings for individual components are built inside either deep n-well (DNW), or isolated P-well (IPW). However, we can also improve isolation for a block, which is group of components as shown in Figure 3.29. The guard ring for a block is established in P-substrate.
Figure 3.27: Guard ring for RF-PMOS

Figure 3.28: Guard ring for RF-NMOS

Figure 3.29: Guard ring established in P-substrate to isolate a noisy RF block
3.8 Measured Results

The proposed LNAs are implemented in TSMC 0.18μm CMOS technology. The Type I LNA is packaged in Micro Lead Frame (MLF) packaging by Amkor technology® [52], so the Type I LNA is measured with a PCB and the results are extracted by accounting for the performance degradation of a signal trace in the PCB and the SMA port. The measurement setup for the Type I LNA is shown in Figure 3.30.

As we will discuss later, we observe some unintended local oscillation at frequencies very close to our target frequency range. Since it was very difficult find the source of the oscillation, we decided not to package the Type II LNA for better observation. For the Type II LNA, we measured the chip in two ways: chip-on-board (COB) measurement and a probe station. The COB method requires wire bonding
directly from the die to the PCB, so another PCB was designed. Figure 3.31 shows the measurement setup for the *Type II* LNA with COB method.

![Figure 3.31: Measurement setup for the Type II LNA with the COB method](image)

### 3.8.1 Power Gain and Noise Figure

Figure 3.32 shows the measurement results of power gain (S21) and NF for the *Type I* and *Type II* LNAs. The *Type I* LNA gives a maximum power gain of 15.5dB, but it could not satisfy the required 1dB signal bandwidth (3 to 5 GHz). One reason for this failure is because of unintended resonance at 2.5 GHz and at 6.2 GHz, which is manifested as an unusually high NF with strangely low power gain around 2.5 GHz and 6.2 GHz. Also, an uneven power gain response can be observed in the target frequency band (3 ~ 5 GHz). The uneven response may be due to poor calibration of equipments used or to uncharacterized effects from PCB, soldering, and SMA ports. The LNA achieves only a maximum NF of 3.3 dB over the 3 GHz to 5 GHz frequency range, which exceeds our specification.
The *Type II* LNA was measured in the COB method, and by a probe station. Therefore we could obtain better results that match closely with simulation results. Also, as shown in Figure 3.32(b), the S21 measurement is fairly even. The power gain remains around 16 dB over the frequency range of interest, and we achieved a maximum NF of 2.3 dB. The measured S21 and NF satisfy our specification listed in Table 3.1. The lower NF of *Type II* LNA results from the simple input matching network and optimal noise matching.
Figure 3.32: Power gain ($S_{21}$) and Noise figure (NF)
3.8.2 Input and Output Matching Performance

Figure 3.33 shows the measured input and output reflection of the two proposed LNAs. The Type I LNA achieves less than -8.6 dB and -10dB of input and output reflection respectively, and these numbers are acceptable for the RF front-end. The input and output matching performance of the Type II LNA are excellent thanks to the well-defined matching network implementation. The measured results show less than -10.5 dB and -13.1 dB of input and output reflection respectively.

However, one can still observe uneven response from the Type I LNA, especially over the frequency range of interest, while the Type II responds smoothly. From this observation, we learned that any uncertainty in PCB, soldering, SMA port, or SMA cable for the connection between the board and the equipment can effect measurements. The circuit is more sensitive to harmful side-effects in the frequency range where it gives high power gain.
Figure 3.33: Input and Output matching performance (S11 and S22)
3.8.3 Linearity (P1dB and IIP3) Performance

The 1dB compression point (P1dB) indicates the amount of power that a device can produce [53]. A device is assumed to operate in a linear manner at low signal levels, and the output signal will begin to tail off as the input signal increases. When the difference between the theoretical output (calculated from the gain at low signal levels) and actual output becomes 1dB, the input power or output power is measured and referred to as the ‘input 1dB point’ or ‘output 1dB point’ respectively, as shown in Figure 3.34.

![Figure 3.34: 1dB compression point](image)

The third order intercept point (IP3) describes the amount of third-order intermodulation distortion (IMD) expected in a device [54], [94]. Due to imperfect linearity of an integrated circuit, it produces harmonics. Since third order products fall near the frequency range of interest, they are more important than second order products. In general, a two-tone test can measure a device’s third order IMD. The two-tone test applies two finely spaced fundamental tones $f_1$ and $f_2$, located within the band of interest. These fundamental tones along with the third order IMD produced by the device can be observed by a spectrum analyzer as shown in Figure 3.35.
The levels of fundamental and third order output are plotted and the two lines are extended to a theoretical point that considers the device to be linear until the lines cross each other. Since the IP3 is determined by extrapolation from measured values, it can change depending on the signal level from where the plots are extrapolated. The IP3 plot is illustrated in Figure 3.36.
Since input referred third order intercept point (IIP3) is more meaningful than output referred third order intercept point (OIP3) for LNA evaluation, we performed the two-tone test to evaluate the IIP3. The two-tone test results for the IMD for the LNAs are shown in Figure 3.37. The Type I LNA could achieve slightly better linearity than the Type II LNA thanks to the Type I’s greater bias current. It is well known that greater current dissipation and larger transistor size can improve the device linearity [31]. As a result, Type I LNA gives -15 dBm of input referred P1dB and -7 dBm of IIP3, while Type II LNA achieves -23 dBm of input referred P1dB with -9 dBm of IIP3.
Figure 3.37: Linearity performance

(a) Type I LNA

(b) Type II LNA
3.8.4 Performance Summary

The *Type II* LNA gives better performance in all aspects except linearity, even with its slightly lower power dissipation. Table 3.3 summarizes the performance comparison of our LNAs with comparable other LNA designs targeted for UWB applications. It can be observed that the *Type II* LNA achieves a higher power gain and a lower noise figure than the previously reported designs, while the power dissipation is comparable. In terms of current consumption, *Type I* LNA draws 10mA from a 0.9V supply and *Type II* LNA draws 6.4mA from a 1.2V supply.

<table>
<thead>
<tr>
<th>Table 3.3: Performance comparison</th>
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<tr>
<td>Tech</td>
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<tr>
<td>Type I</td>
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<td>[32] (2004)</td>
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The LNAs reported in [27] and [32], both use LC filter configuration for the input impedance matching network with an inductive source degenerative topology like our *Type I* LNA. In these designs, the input impedance is matched to 50 Ω resistive impedance, so they do not require impedance inverting unlike our *Type I* LNA. The large resistive input impedance implies a large source degeneration inductance. The negative feedback increases as the inductance increases and limits achievable power gain in this topology. Consequently, the reported designs could achieve only less than 10 dB power.

---

* 1dB bandwidth. Others are 3dB bandwidth
† Power dissipation only in a core amplifier
gain in CMOS. The LNA fabricated in SiGe provides excellent performance in terms of both the noise figure and the power gain at the cost of price [32]. Power consumption is also higher in order to overcome the negative feedback problem mentioned earlier. The work in [28] introduces a distributed matching technique, which employs multiple narrow band LNAs to cover the wide bandwidth. The distributed matching technique inherently consumes more power, and occupies large space due to the multiple LNAs, therefore it is not desired for low power applications such as UWB in spite of the extremely wide bandwidth coverage. The LNA introduced in [97] is the most recently reported work at this time. It adopts a feedback topology for wideband input impedance matching.

All previous works in CMOS except [97] were aimed to show the feasibility of UWB LNA implementation in CMOS and therefore the bandwidth is much wider than ours. These designs cannot be considered for commercial applications because the noise figure is over 6 dB and the power gain is less than 10 dB. The design reported in [97] and our work are both targeted for commercial applications and very similar bandwidth specifications. Therefore only meaningful comparison can be made between our work and the design reported in [97]. The power gain achieved in [97] is lower than 10 dB because it fully relies on feedback topology to provide the wide input impedance matching. On the other hand, our Type II LNA, only partially utilizes feedback to increase the resistive input impedance therefore much higher gain was achieved.
Chapter 4:
System-Level Architecture – Frequency Domain Approach

4.1 Digital I-UWB Receiver

4.1.1 Challenges in Digital I-UWB Receiver

Some major challenges in digital I-UWB receiver design stem from the I-UWB channel, the narrow pulse shape, and narrowband interference. First, the I-UWB channel inherently suffers a relatively large delay spread as compared to the pulse width. The delay spread is normally at least tens of nanoseconds [33] compared to typical pulse widths of hundreds of picoseconds. During the large delay spread it is possible that hundreds of multipath reflections may be seen by the receiver. Thus, for a standard RAKE receiver, many correlators are necessary to exploit available multipath diversity. Such a large number of RAKE fingers is not practical for an analog correlator because it adds excessive complexity in hardware and control operations.

With a digital receiver, the narrow pulse shape presents a challenge. Signal processing requires ADC’s operating at least as fast as the signal’s Nyquist rate. For I-UWB signals, this rate is at least several GHz, which is very difficult to achieve with contemporary VLSI technologies. For this reason, all proposed digital I-UWB receivers employ a parallel ADC architecture [34], [35], [36].

Finally, the UWB spectrum is allocated over the spectrum of existing narrowband applications, so it is inevitable for a UWB system to encounter in-band interference from narrowband devices. Therefore, an I-UWB receiver needs to employ sophisticated
interference suppression algorithms. Again, these algorithms require ADCs that are not only fast but have a wide dynamic range. This ensures the capture of I-UWB signals that have a lower power level than that of the narrowband interference. The next three subsections describe existing methods that address the challenge of converting I-UWB signals to the digital domain.

Section 4.3 presents a brief review of sampling theory for a better understanding of frequency domain sampling. Section 4.4 translates the process to hardware, and it explains a method to convert the received signal to a frequency domain representation through a filtering operation. Section 4.5 and 4.6 describes the integration of a frequency domain sampler into a conceptual system architecture.

### 4.1.2 Time-interleaved ADC

A time-interleaved ADC employs multiple parallel ADCs driven by multiple clocks that are separated by small time difference as shown in Figure 4.1 [34]. This approach reduces the required speed of the ADC by the number of parallel ADCs. For example, two ADCs in parallel reduce the required ADC speed by half. However, since each ADC sees the full bandwidth of the input signal, sample/hold circuitry becomes difficult to design. Additionally, the time-interleaved approach is very sensitive to sampling jitter, since the relative clock delays must be precise. Finally, the time-interleaved ADC requires an exceptionally large dynamic range in the presence of narrowband interferers.
4.1.3 Frequency Channelized ADC Using Bandpass Filters

Unlike the time-interleaved ADC, the frequency channelized ADC with BPFs clocks parallel ADCs simultaneously. Therefore this approach is less sensitive to timing jitter [35]. Also, the approach relaxes the dynamic range of the ADCs because it is now possible to exclude or suppress any frequency channel with strong narrowband interference. However, it is very difficult to maintain consistent frequency responses of the ADCs in different frequency channels. Additionally, design of high frequency BPFs is very difficult, and it is expensive to ensure consistent performance across the frequency channels. The most significant drawback for this channelization technique is that it cannot avoid the aliasing caused by the non-ideal finite frequency response of the BPFs. In other words, the frequency responses of the BPFs are not ideal rectangles, so they overlap and interfere with each other in the frequency domain.

The architecture of the frequency channelized ADC with BPFs is shown in Figure 4.2. Note that \( H \left( j\Omega \right) \) is the frequency response of the BPF assigned to each sub-band. The sampling clock \( f_{\text{clk}} \) should be at least twice the bandwidth of the BPF to conform to the Nyquist sampling rate.
4.1.4 Frequency Channelized ADC Using Lowpass Filters

The frequency channelized ADC with lowpass filters (LPFs) is suggested to improve performance over the frequency channelized ADC with bandpass filters. Figure 4.3 shows the operation of this approach [36]. Instead of employing BPFs, it downconverts sub-bands such to a zero center frequency, so all sub-bands require the same LPF. A LPF is easier to design and cheaper than a BPF, so it simplifies the overall circuit complexity even considering the additional downconverting mixers. Also, the approach is more robust to sampling jitter and relaxes the sample/hold circuitry because it processes the received signal in a low frequency range.

Figure 4.2: Frequency channelized ADC using BPF
However, since the approach employs downconverting, mixer phase noise may be present. This causes serious problems if the mixer phase noise includes spurious frequency tones caused by poor circuit isolation. Therefore, the circuit isolation should be carefully considered in this architecture, otherwise multiple local oscillation signals denoted as $\exp(-j2\pi kf_{clk}t)$ will generate numerous spurious tones through self-mixing and cross-mixing. Also, the non-linearity of the mixer itself can contribute to the spurious tone generation.

![Diagram](image)

Figure 4.3: Frequency channelized ADC using LPF
4.2 Signal Analysis in the Frequency Domain

A continuous-time periodic signal $x(t)$ with a period $T_p$ is expressed as

$$x(t) = \sum_{k=-\infty}^{k=\infty} c_k e^{j2\pi F_0 k t}$$  \hspace{1cm} (4.1)

$$c_k = \frac{1}{T_p} \int_{t_0}^{t_0+T_p} x(t) e^{-j2\pi F_0 k t} dt$$  \hspace{1cm} (4.2),

where $F_0 = 1/T_p$ is the fundamental frequency of the signal, and a coefficient $c_k$ represents a spectral component of the signal [55]. Note that the $c_k$'s are usually complex values, and $c_k$ and $c_{-k}$ are complex conjugates. The period $T_p$ is the observation window of the received signal, which is often a fraction of the pulse repetition interval (PRI) for typical I-UWB signals.

Noting that $\omega_0 = 2\pi F_0 = \frac{2\pi}{T_p}$ and using the periodic characteristics of a sinusoidal function, (4.2) leads to the relation given in (4.3)

$$c_k = \frac{1}{T_p} \left[ \int_{t_0}^{t_0+T_p} x(t) \cos(k\omega_0 t) dt - j \int_{t_0}^{t_0+T_p} x(t) \sin(k\omega_0 t) dt \right]$$

$$= \frac{1}{T_p} \left[ \int_{t_0}^{t_0+T_p} x(\tau) \cos(k\omega_0 (T_p - \tau)) d\tau + j \int_{t_0}^{t_0+T_p} x(\tau) \sin(k\omega_0 (T_p - \tau)) d\tau \right]$$  \hspace{1cm} (4.3),

$$= \frac{1}{T_p} \left[ x(t) \ast \cos(k\omega_0 t) + j x(t) \ast \sin(k\omega_0 t) \right]_{t_0+T_p}$$

where $k$ is an integer and ‘*’ is the convolution operation. Also noting that

$$\mathcal{L}\{\cos(k\omega_0 t)\} = \frac{s}{s^2 + (k\omega_0)^2}$$  \hspace{1cm} (4.4)\text{and}

$$\mathcal{L}\{\sin(k\omega_0 t)\} = \frac{k\omega_0}{s^2 + (k\omega_0)^2}$$  \hspace{1cm} (4.5),

where $\mathcal{L}\{\}$ represents Laplace transform, (4.3) can be expressed as
where \( X(s) \) is Laplace transform of \( x(t) \). Equation (4.6) provides the starting point for the design of a frequency domain sampler.


4.3 Sampling Theorem Revisited

If a continuous-time periodic signal \( x(t) \) is band limited, its Fourier coefficient \( c_k = 0 \) for \(|k| > M\) as shown in Figure 4.4(a), where \( M \) is some positive integer. Similarly, if a Fourier coefficient \( c_k = 0 \) for \( M < |k| < N/2 \) and the sampling frequency \( f_s = NF_0 \) as shown in Figure 4.4 (b), then a periodic discrete-time signal has the fundamental period \( N \) in the time domain and is periodically band limited. Suppose now that the sampling frequency \( f_s = F_s = NF_0 \) (which implies \( N \) samples during the fundamental period \( T_p \)) as in Figure 4.4 (b), then the resolution of spectral components \( 2\pi/N \) is equivalent to \( F_0 \) due to the relationship \( \frac{2\pi}{N} = \frac{f_s}{N} = \frac{NF_0}{N} = F_0 \). Note that the normalized frequency \( 2\pi \) corresponds to \( f_s = F_s = NF_0 \).

In the same manner, the resolution of the spectral components for the signal in Figure 4.4(c) is \( 2\pi/aN \) for the sampling frequency \( f_s = aF_s = aNF_0 \). However, the resolution of the spectral components still remains the same \( F_0 \) due to the relationship \( \frac{2\pi}{aN} = \frac{f_s}{aN} = \frac{aNF_0}{aN} = F_0 \). An important fact is that the Fourier coefficients \( c_k \) for all three signals in the figure are identical for \(|k| \leq M\). This suggests that these \( 2M \) samples are all that are necessary to describe the received signal. In other words, the effective sampling rate of a band limited periodic signal can be increased arbitrarily simply by padding the frequency samples with zeros. We exploit this property to accurately sample the received signal at lower sampling rates than time-domain ADCs.
Figure 4.4: Signals in time and frequency domain
4.4 Frequency Domain I-UWB Receiver

CMOS implementation of UWB receivers is highly desirable for many UWB applications, in which low cost and/or low-power consumption are critical. As mentioned previously, I-UWB is preferable due to its simpler hardware and more accurate ranging. However, the wideband nature of I-UWB leads to a major challenge for CMOS implementation of I-UWB receivers. The challenge stems from the fact that I-UWB is based on narrow pulses, and conventional over-sampling of such pulses requires extremely high-speed ADCs. For this reason, most existing I-UWB receivers for high data rate rely on analog correlators [2]. Time domain processing with analog correlators prevents the receiver from fully exploiting the advantages of digital communications. As a result, the performance is degraded by reduced data rate, reduced range, or increased bit error rate (BER).

We briefly reviewed previous research on digital I-UWB receivers, which extract digital information from received I-UWB signal. While all previous research focuses on sampling a time domain signal, we propose a new method called frequency domain sampling to perform analog-to-digital conversion, and it encounters none of the shortcomings of the previous methods. Unlike time-interleaving and channelization, the key idea of frequency domain sampling is to sample the frequency spectrum rather than signal shape in time. This allows for a relaxation of the ADC speed requirement [37]-[42]. Our frequency domain approach lowers the required sampling rate to the pulse repetition rate, but it also increases the effective sampling rate.

Note that the ADC output of previous methods is a sampled signal in the time domain, whereas the ADC outputs for our method are spectral components in the frequency domain. Figure 4.5 contrasts the characteristics of the filters for two approaches. As shown in Figure 4.5, our method does not require the ideal, flat-top bandpass filters necessary for the time-domain sampling, and hence it does not incur the aliasing problem [56].
4.4.1 Frequency Domain Sampling

Expressions (4.3) and (4.6) imply that a coefficient $c_k$ can be obtained by sampling the outputs of analog filters with transfer functions of (4.7) and (4.8).

\[
image(c_k) = \frac{k \omega_0}{s^2 + (k \omega_0)^2} \quad (4.7)
\]

\[
real(c_k) = \frac{s}{s^2 + (k \omega_0)^2} \quad (4.8)
\]

A filter with the transfer function of (4.7) can be implemented using an LC resonator, and the factor of ‘s’ is a differentiator. The resulting structure of a filter bank is shown in Figure 4.6, and a filter bank captures one spectral component of the received signal.
In fact, the filter bank implementation is the major issue for the architecture. Figure 4.7 shows a general Biquad filter configuration [57], and its voltage responses are depicted in (4.9), and (4.10).

\[ \frac{V_L}{V_{in}} = \frac{-H}{s^2 + (1/Q)s + 1} \]  
\[ (4.9) \]

\[ \frac{V_B}{V_{in}} = \frac{-Hs}{s^2 + (1/Q)s + 1} \]  
\[ (4.10) \]

Comparing (4.7) and (4.8) with (4.9) and (4.10), one can notice that (4.7) and (4.8) are a special case of (4.9) and (4.10) with infinite Q. Therefore, one can obtain a real spectral term from the BPF output, and an imaginary spectral term from the LPF output, if Q is infinite in the Biquad filter.

Even though it is very difficult to make Q factor infinite in real circuit implementation, it can be achieved in our case by simply eliminating the 1/Q feedback path in Figure 4.7. Figure 4.8(b) shown one circuit example with simple op-amps [58]
(though it is not feasible for UWB applications due to the limited speed of op-amps in current technology [59]). Note that Figure 4.8(b) is modified from Figure 4.8(a), and it achieves infinite Q by eliminating \( R_1 \).

\[ \text{(a) General OP-AMP based Biquad filter} \]

\[ \text{(b) Modified OP-AMP based Biquad filter for Frequency Domain filter bank} \]

Figure 4.8: OP-AMP based Frequency Domain filter bank implementation

A frequency domain sampler consists of multiple filter banks followed by multiple ADCs as shown in Figure 4.9. Each filter bank \( f_i \) captures a spectral component at frequency \( f_i \) of the received signal, where \( f_i = kF_0 \) for an integer \( k \). Further, \( f_i \) should reside in the in-band spectrum. Note that \( f_0 \) is not necessarily the same as the fundamental frequency \( F_0 \). The number of filter banks is determined by a time-window size \( T_p \). A
larger time window captures more multipaths, but it decreases the fundamental frequency \( F_0 \), which, in turn, increases the total number of filter banks.

Each filter bank requires two ADCs and the sampling rate of the ADCs is the inverse of the PRI. A salient point of the proposed frequency domain sampler is that the ADC speed is determined by the PRI, not the over-sampling rate and the width of received pulses. Thus, the ADCs operate much a lower frequency to enable CMOS implementation. Note that ADCs can be time-shared by spreading the samples over a PRI.

![Figure 4.9: Frequency domain sampler](image)

### 4.4.2 Time Domain Signal Reconstruction

It is possible to reconstruct a signal in the time domain from the spectral samples obtained from a frequency domain sampler. Conceptually, this can be done by performing an IFFT (Inverse Fast Fourier Transform) operation on the spectral components with an adequate number of zeros padded [60]. In this conceptual design, note that the effective sampling frequency is determined by the number of zeros. Figure 4.10 shows a time domain signal reconstructed through a 128-point IFFT, in which the time-window size is 1 ns, the number of filter banks is seven, and 114 zeros are padded. The reconstructed signal is close to the original signal, especially during the main portion of the pulse (whose spectrum is mostly in-band). The discrepancy between the original
signal and the reconstructed one is due to the elimination of out-of-band spectral components, which is not a concern.

![Reconstructed time domain signal](image)

**Figure 4.10: Reconstructed time domain signal**

### 4.4.3 Correlation and Convolution

A correlation operation of two real signals $x(t)$ and $\tilde{x}(t)$ in the time domain is a multiplication in the frequency domain as expressed below [61].

$$R(\tau) = \int x(t)\tilde{x}(t+\tau)dt = F^{-1}\left\{X^*(f)\tilde{X}(f)\right\}$$  \hspace{1cm} (4.11)

The peak correlation value for a received signal and the template occurs at $\tau=0$ in the time domain if the receiver and transmitter are synchronized. The correlation value at $\tau=0$ is equivalent to the index-0 output of an IFFT block, which is the sum of all spectral components, i.e., the multiplication result. In a similar manner, the convolution operation in the time domain is also a multiplication in the frequency domain. Hence, the
correlation and convolution operations can be performed efficiently in the frequency domain. This suggests that the time-domain reconstruction may not be necessary.

### 4.4.4 Architecture

The frequency domain approach enables sampling of the received signal in the frequency domain and can be applied to any communication system, including narrowband systems. In this section, we present a system architecture for I-UWB receivers employing frequency domain sampling.

Figure 4.11 shows the overall architecture for an I-UWB receiver using a frequency domain approach. The proposed I-UWB receiver consists of an ultra wideband LNA, a frequency domain sampler, an energy harvester block, and a decision block.

![Figure 4.11: Proposed I-UWB receiver architecture](image)

The energy harvester block collects the energy dispersed on multipaths, and its function is identical to the RAKE function used for narrowband communications systems [62] - [66]. The communication channel is estimated after achieving synchronization, and the equalizer performs inter-symbol interference cancellation to recover an ideally interference-free representation of the desired symbol. Most of the components in the energy harvester block serve to improve performance, so they are discussed in Section 4.5.
4.4.5 Performance

In this section, we present simulation results for the performance of the proposed frequency domain UWB receiver and compare the results with conventional UWB receivers employing analog correlators. Two receivers, one for the single band covering the entire spectrum allocated by the FCC [1] and the other one covering only the lower-band are modeled in Matlab and simulated for the Intel UWB channel model CM#4 [33]. Please refer to Appendix E for further information of the UWB channel model. The system specifications of the two receivers are as follows.

**Single-band UWB receiver:**
- Pulse width: 145 ps
- Bandwidth: 7.5 GHz (3.1 GHz – 10.6 GHz)
- Pulse shaping: Band-pass filtered Gaussian monocycle pulse
- PRI: 10 ns
- Number of filter banks: 7
- Time window size: 1 ns

**Lower-band UWB receiver:**
- Pulse width: 242 ps
- Bandwidth: 2.08 GHz (3.1 GHz – 5.18 GHz)
- Pulse shaping: Band-pass filtered Gaussian monocycle pulse
- PRI: 10 ns
- Number of filter banks: 6
- Time window size: 3 ns

Note that channel coding was not employed for the receivers, and no inter-symbol interference (ISI) is assumed.

Figure 4.12 shows simulation results for the single-band UWB receivers. The simulation results indicate that the proposed receiver performs better than the analog receiver for the entire range of the SNR simulated, and the performance gap increases with increasing SNR. The proposed receiver improves the SNR by 3.5 dB at BER=10\(^{-1}\) when compared with the analog receiver. The improved performance is attributed to the
multipath energy harvesting in our receiver, when more than two pulses are received in a time window duration.

![Figure 4.12: Performance of the single band UWB receivers](image)

Figure 4.13 shows the performance for lower-band receivers. Like single-band receivers, the proposed receiver performs better than the analog receiver for the entire range of the SNR in the figure. The performance improvement of the proposed receiver is about 3 dB at BER=10^{-1} over the analog receiver. Note that the performance of both the proposed and analog lower-band receivers degrades compared with the single-band receivers. This is caused by the increase of the inter-pulse interference due to a wider pulse width for the lower-band receivers and also by the reduced spectral energy.
Figure 4.13: Performance of the lower-band UWB receivers
4.5 Frequency Domain Baseband Signal Processing

Section 4.4 presented a new way to digitize a UWB impulse signal in the frequency domain. The frequency domain receiver eliminates the need for a high-speed analog-to-digital converter (ADC). One drawback of the conceptual system architecture is that it requires an inverse fast Fourier transform (IFFT) to translate the spectral information to the time domain. Traditionally, baseband signal processing relies on a time domain representation of the data, and such baseband operations include RAKE processing of multipaths, synchronization, and equalization. The translation to the time domain and the subsequent time domain operations for a frequency domain receiver implementation would complicate hardware and increase power dissipation.

Our proposed energy harvester addresses this shortcoming. All signal processing, including synchronization, clock recovery, channel estimation, matched filtering, and equalization, is performed in the frequency domain. Therefore, the proposed energy harvester eliminates the need for an IFFT block to reduce the hardware complexity of the proposed I-UWB receiver. This section focuses on baseband signal processing in the frequency domain. The processing performs the basic function of mitigating ISI, which is critical for high data rate applications.

First, we introduce a synchronization and clock recovery operation in the frequency domain. Then the results are used to configure a frequency domain matched filter and a frequency domain equalizer for channel estimation.

4.5.1 Background

In I-UWB systems, the pulse rate is the inverse of the pulse repetition interval (PRI). Therefore, a high data rate requires a short pulse repetition interval (PRI), but this causes ISI due to the long delay spread of UWB signals. It is observed in [33] that the delay spread of UWB signals may last as long as 250 ns, which results in significant ISI for pulse rates higher than 4 Mbps ( = 1 / 250 ns) [refer to Appendix E].
The channel response \( h(t) \) is expressed as the channel impulse response \( c(t) \) convolved with the impulse response of the transmitter’s pulse shaping filter \( g(t) \)

\[
h(t) = c(t) * g(t)
\]

(4.12),

where the operator \( * \) represents the convolution operation. Therefore, the received signal for the \( \alpha \)th single impulse without ISI is expressed as

\[
r_\alpha(t) = I_\alpha h(t) + \eta(t), \quad \alpha = 1, 2, 3, ...
\]

(4.13),

where \( I_\alpha \) is either 1 or \(-1\) for BPSK (Binary Phase Shift Keying) and \( \eta(t) \) is the additive white Gaussian noise (AWGN). However, as shown in Figure 4.14, the signals overlap because the PRI is shorter than the delay spread. The overlapped signals are expressed as

\[
r(t) = \sum_\alpha I_\alpha h(t - \alpha PRI) + \eta(t)
\]

(4.14).

Suppose that we observe each pulse only during the period of the time window as indicated in Figure 4.14. Then, the time domain expression in (4.14) is equivalent to (4.15) in the frequency domain within a time window.

\[
R = \sum_\alpha I_\alpha H_\alpha + \Gamma, \quad \alpha = 1, 2, 3, ...
\]

(4.15)

In (4.15), \( H_\alpha = \mathcal{F}\{h(t - \alpha PRI)|_{t \leq T_{\text{window}}}} \) is the frequency domain channel response, and \( \Gamma \) is the expression of the noise in the frequency domain.

Figure 4.14: Channel condition under ISI
4.5.2 Synchronization

For an I-UWB receiver based on analog correlation, the synchronization should be precise in time to match the template signal and to fully capture narrow pulses. However, our proposed synchronization method must address a slightly different issue in the frequency domain, as explained next.

Suppose that one pulse sent by the transmitter constitutes one symbol. A received I-UWB signal within a time window is composed of the current symbol overlapped with multiple previous symbols. If a receiver can resolve each symbol, it is possible to accumulate the signal energy from each symbol to maximize the recovered signal energy. Thus, the criterion adopted for the frequency domain synchronization scheme is to find the position of a time window within a pulse repetition interval (PRI) with the greatest signal energy.

A packet contains a known preamble sequence, which is used to perform synchronization and channel estimation. *We assume that the autocorrelation of the preamble sequence is a delta function* [67], so that any circular shifted preamble sequence results in low (ideally zero) autocorrelation with the intended preamble sequence. This assumption is usually valid and allows a parallel search of the preamble sequence.

Suppose that the length of the preamble sequence is \( m \). Then, there are \( m \) possible circular shifted sequences. Let \( CS_i \) be the sequence obtained through the circular shift-right operation of the original preamble sequence by \( i \) positions. The proposed approach for synchronization is as follows. We extract the spectral components of the received signal \( r(t) \) and correlate them with each individual sequence \( CS_i, i=0,1,...,m-1 \). The correlation process is illustrated in Figure 4.15. Note that the length of the preamble sequence is five in the figure.
Next, the energy of $m$ correlated values is computed and recorded. Note that the correlation operation in the frequency domain is multiplication. Then, we advance the time by the time step by $w$ and repeat the process. After we sweep the entire period of the preamble sequence, the time position which yields the maximum energy is the desired synchronization time. We describe this process below.

Suppose that we start the synchronization operation at an arbitrary reference time $T_{ref}$, and suppose that the received signal $r_{n,k}(t)$ under consideration for correlation is offset from the reference time $T_{ref}$ by $n \cdot PRI + k \cdot w$ as expressed in (4.16).

$$r_{n,k}(t) \bigg|_{T_{ref} + n \cdot PRI + k \cdot w \leq T_{ref} + n \cdot PRI + k \cdot w + T_{window}} = r_{n,k}(T_{ref} + n \cdot PRI + k \cdot w + t) \bigg|_{0 \leq t \leq T_{window}}$$

The spectral components $R_{n,k}$ of the time domain received signal $r_{n,k}$ are equivalent to the output data from the frequency domain sampler, and they are expressed as

$$R_{n,k} = \mathcal{F}\left\{r_{n,k}(T_{ref} + n \cdot PRI + k \cdot w + t)_{0 \leq t \leq T_{window}}\right\}$$

Let us denote that $CS_i(n)$ is the $n_{th}$ bit (which is 0 or 1; positive or negative in signal polarity) of the sequence $CS_i$. The energy of the received signal $r_{n,k}(t)$ after correlation with $CS_i$ is expressed in as
\[ E_{i,k} = e \left\{ E \left\{ R_{n,k} C S_i(n) \right\}_{n=0,1,...,m-1} \right\} \]  

(4.18),
in which \( E \{ \} \) represents the mean function, and the function \( e \{ \} \) calculates the energy of the function inside the bracket. Note that \( e \{ H(f) \} = |H(f)H^*(f)| \).

The objective of the synchronization process is to determine the values of \( i \) and \( k \) in (4.18) as described below.

The value of the optimal time window index \( k \) is denoted as \( k_0 \) and it represents the number of time steps necessary to determine the time window position in the time axes. The time with the maximum signal energy is measured relative to the reference time \( T_{ref} \), and the energy is obtained as the combined energy of the individual components.

\[ k_o = \max_k \left( \sum_{i=0}^{m-1} E_{i,k} \right) \]  

(4.19)
The function \( \max_k \) returns the value \( k \) giving the maximum value.

The optimal value of \( i \) is denoted as \( i_o \), and it represents the number of circular shifting operations. The value of \( i_o \) implies the starting point of the preamble sequence that results in the highest correlation at the time window index \( k_0 \), and it is obtained as

\[ i_o = \max_i \left( E_{i,k_o} \right) \]  

(4.20)
Resultantly, the synchronized starting time \( T_{synch} \), which gives the highest signal correlation energy, is expressed as below.

\[ T_{synch} = T_{ref} + k_o \cdot w - i_o \cdot PRI \]  

(4.21)
Let us consider the search time, which may be expressed as

\[ T_{search} = (PRI + T_{window})(m \cdot PRI + w) / w \]  

(4.22)
The search period is the minimum time period in which there exists a time window \( T_{window} \) with the maximum energy. As indicated in Figure 4.14, it can be seen readily that the search period is less than \((PRI+T_{window})\). As the search time step is \( w \), the term \((PRI + T_{window})/w\) in (4.22) is the required number of repetitions to sweep the entire search period. The correlation period with a preamble sequence of length \( m \) is \((m \times PRI + \)
Note that the extra term $w$ is the required time to slide the time window by $w$ to adjust for the next correlation period after completing the current correlation cycle.

With the expression in (4.22), a designer can decide an appropriate synchronization time to meet performance requirements by adjusting the time step $w$ and the length $m$ of the preamble code sequence.

Finally, we elaborate on the reliability of the correlation energy. As explained earlier, if the correlation energy achieved from a certain circular shifted preamble sequence has less energy than the noise energy, then it degrades the receiver performance. This occurs if the noisy correlation results are taken as the true channel response. Therefore, it is a good strategy to eliminate such erroneous terms. The noise energy in the received signal is defined as the variation of the received signal as

$$N_{i,k} = E\left\{ \left( R_{n,k}CS_i(n) \right)_{n=0,1,\ldots,m-1} \right\} - E\left\{ R_{n,k}CS_i(n) \right\}_{n=0,1,\ldots,m-1}^2 \quad (4.23)$$

In (4.23), $N_{i,k}$ is the noise energy induced to the $i$th previous symbol at the $k$th time window position. Note that the $i$th circular shifted preamble sequence is applied to the surviving ISI of the symbol transmitted $i$ PRIs previously. Therefore, the survival correlation energy terms are selected by comparing them with the noise energy as

$$E_{i,k} = \begin{cases} E_{i,k} & \text{if } E_{i,k} \geq N_{i,k} \\ 0 & \text{otherwise} \end{cases} \quad (4.24)$$

The receiver ignores correlation terms with less energy than the noise.

### 4.5.3 Clock Recovery

The clock recovery circuit tracks the optimal sampling point of the received signal within a PRI under time variant and frequency selective channel conditions. Clock recovery starts after the initial synchronization, so we can discuss the steady state response of the clock recovery scheme.

The clock recovery scheme is based on a fundamental PLL architecture with two modifications [68], [69], [70]. First, to handle time-variant channel conditions, the
template, which is the virtual channel response used for signal correlation, is updated according to channel conditions [71], [72], [73]. Second, to handle the frequency selective channel, the circuit considers variations of the signal-to-noise ratio (SNR) over the entire frequency band. The circuit tracks the reference phase with highest SNR among spectral components.

![Figure 4.16: Structure of clock recovery circuit](image)

Figure 4.16 shows the structure of the clock recovery circuit, which is similar to a time domain clock recovery circuit. Compared to time domain approach, the basic difference is that the proposed circuit detects phase error from sampled spectral components. This results from the time shift property of the Fourier transform, which states that the amount of time shift is represented as phase rotation in frequency domain.

\[
\mathcal{F}\{f(t - t_0)\} = e^{-j\omega t_0}F(\omega)
\]  

(4.25),

where \(t_0\) is the amount of timing error caused by either clock drift or by the dynamic channel environment, and \(\mathcal{F}\{\cdot\}\) represents the Fourier transform operation.

Note that the expressions for the sampled spectral component \(\Re(\omega_m, t_0)\) and the reference phase \(\Re(\omega_p)\) refer to the \(m^{th}\) spectral component in an array of multiple spectral components. This is because the proposed frequency domain sampler generates
an array of spectral components with each spectral component produced by one filter bank.

Thus, the $m^{th}$ harmonic spectral component of the received signal, $\Re(\omega_m, t_0)$, with timing error $t_0$, appears as

$$\Re(\omega_m, t_0) = e^{-\omega_0 t_0} \Re(\omega_m)$$

(4.26),

where $\omega_m = m\omega_0$ with fundamental frequency $\omega_0$, and $\Re(\omega_m)$ is the $m^{th}$ harmonic spectral component among the received signal spectral array when perfectly synchronized.

From (4.26), a simple conjugate multiplication can detect phase error due to timing error as in (4.27).

$$\Re(\omega_m, t_0) \Re(\omega_m)^* = e^{-\omega_0 t_0} \Re(\omega_m) \Re(\omega_m)^* = |\Re(\omega_m)|^2 e^{-\omega_0 t_0}$$

(4.27)

Practical operation requires only narrow range of controlling phase, which allows a linear approximation of (4.27) as

$$|\Re(\omega_m)|^2 e^{-\omega_0 t_0} = |\Re(\omega_m)|^2 \left( \cos \omega_m t_0 - j \sin \omega_m t_0 \right) \approx |\Re(\omega_m)|^2 \left( 1 - j \omega_m t_0 \right)$$

(4.28).

Another distinguishing feature of the clock recovery circuit is phase compensation for the template signal, which is the result of channel estimation. After correlation, the newly sampled signal is then compensated for its phase error and fed into a noise reduction filter. The de-noised signal updates the template to improve performance under time-variant channel conditions. Thus, the clock recovery block should be incorporated with the channel estimation block discussed in next section.

**4.5.4 Channel Estimation**

ISI causes frequency selective gains, non-linear phase response, and time dispersion; therefore, an equalizer and a matched filter are indispensable to achieve high performance, and channel estimation is an essential component of each of these [74], [75].
During synchronization, the receiver performs a channel estimation operation based on the known preamble sequence.

The channel estimation process extracts the response of the channel to an input pulse, and we propose to estimate the frequency domain channel response $H$. From (4.14), one can notice that the channel response $h(t)$ describes the signal waveform of the received signal when the information data is ‘1’ while ignoring the noise term. Therefore, the frequency domain channel response $H$ represents the frequency spectrum corresponding to the time domain signal waveform within a time window when the information data is ‘1’. As a result, averaging the products of the received signal and the preamble code over the preamble period can derive the frequency domain channel response $H$. Note that the averaging operation is necessary in order to minimize the noise effects. The averaging operation during the preamble is given as

$$H_{i,k} \approx E\left\{ R_{n,k} CS(n) \right\}_{n=0,1,\ldots,m-1}$$ (4.29)

Thus, the receiver needs to store the average values of the received signal for each $k$ during the preamble, and then it selects a proper channel response with respect to the choice of $k_0$. The receiver can also perform the channel estimation operation after synchronization. This eliminates the need for storage of average results for every $k$, but it incurs the cost of a slightly increased preamble length to allow the receiver enough time to prepare for data communication. The proposed receiver assumes the former method that stores the results for each $k$. From here on, we will omit the term $k$ from (4.29) because $k$ is fixed to the constant value $k_0$ after accomplishing the synchronization.

The strongest correlation energy from a received signal in a time window results from applying the proper preamble sequence that is synchronized with the currently received chips (or symbols) $R_n$. As mentioned previously, the average value of the correlation result implies a spectral channel response $H_0$ corresponding to the current symbol. Note also that the spectral channel response $H_0$ is the representation of the received signal during a time window. The multipaths of this current symbol may last well into future time windows. For example, in the second time window in Figure 4.14, one can observe the combined signal waveform of two distinct signal waveforms assuming there is no transmitted signal before the first pulse. One waveform is a remnant
of first transmitted pulse caused by delay spread, and the other waveform is the strongest multipath component of second transmitted pulse. In this time window, the second pulse experiences a channel response $H_0$, and the first pulse experiences a channel response $H_1$. Note that the channel response is a discrete response, which is valid only during a time window – not between time windows. Therefore, to minimize ISI, the receiver subtracts the current $H_0$ from each future time window as follows.

$$H_0 \equiv E \left\{ R_n \cdot CS_0(n) \right\}_{n=0,1,\ldots,m-1}$$

(4.30)

$$H_1 \equiv E \left\{ CS_1(n) \cdot (R_n - H_0 \cdot CS_0(n)) \right\}_{n=0,1,\ldots,m-1} \mid_{t=0}$$

(4.31)

Equations (4.30) and (4.31) assume that $CS_0(*)$ is a synchronized preamble sequence. Since the preamble data in future time windows is known, the receiver can estimate the channel after successively extracting each $H_0$. From the previous example, in the second time window, the multipath component of the second pulse delivers more energy through channel response $H_0$ than the remnant of the first pulse corresponding to $H_1$. Thus, $H_1$ can be properly evaluated after eliminating the effect of the first pulse as expressed in (4.31).

### 4.5.5 Matched Filter and Equalization

Once the channel response is obtained, it can be applied as coefficients in a matched filter and an equalizer. The equalization is an extended correlation operation [76], [77]. Therefore, the channel profile (or channel response for the given time window) used for the equalization is conceptually equivalent to the template signal used for the time-domain correlation operation. From here on, the term “channel profile” will replace the term “template” to explain an equalization operation. A matched filter provides the inverse of the channel response without ISI. Ignoring the ISI, the response of the matched filter in the time domain is defined as $h^*(-t)$, and its frequency domain expression is $H^*$.

Assuming that $\left| H \right|^2 = 1$, the output of the matched filter for one symbol without ISI is given as
\[ \tilde{I} \cong RH^* \]  

(4.32).

Note that (4.11) is equivalent to a correlation operation in the frequency domain as expressed in (4.32), except that the template signal is replaced with \( H \), the channel response.

Since the matched filter does not consider ISI in the received signal, the ISI effect should be suppressed before the matched filtering. To cancel the post-cursor multipath interference, the estimated symbol is fed back to the input of the matched filter with a proper delay and subtracted from the received signal containing future symbols. This approach is similar to the decision feedback equalization (DFE) method in the time domain [43]. The result of the feedback subtraction and matched filtering are shown in (4.33) and (4.34), respectively.

\[
\tilde{R}_r = R_r - \sum_{d=1}^{L-1} \tilde{I}_{r-d} H_d 
\]

(4.33)

\[
\tilde{I}_r = \tilde{R}_r H^*_0
\]

(4.34)

In (4.33) and (4.34), \( \tilde{R} \) is the intermediate received signal before matched filtering. Note that \( L \) in (4.33) is the maximum number of available channel responses, including any dummy channel responses with less energy than the noise, in order to process the signal in a consecutive manner.

As shown in Figure 4.14, a symbol is spread over several time windows. If we treat the operation of (4.33) and (4.34) as a finger operation in a RAKE structure, we can combine fingers to form a complete RAKE-like structure to accumulate the dispersed symbol energy while mitigating ISI as in (4.35) and (4.36). The RAKE structure operates over multiple PRIs and mitigates ISI, so it is termed a multi-PRI RAKE‡.

\[
\tilde{R}_{r+j} = R_{r+j} - \sum_{d=1}^{L-j-1} \tilde{I}_{r-j-d} H_{j+d}
\]

(4.35)

‡ This nomenclature is used to avoid confusion with the inherent RAKE property of a frequency domain sampler, which acts as a RAKE only within a single time window within one PRI.
\[
\tilde{I}_r = \sum_{j=0}^{L-1} \tilde{R}_{r+j} H^*_j
\]  

(4.36)

A DFE structure based on (4.33) and (4.34) is denoted as an effective finger, and it is shown in Figure 4.17 in the dotted box. Individual effective figures are combined together as described in (4.35) and (4.36) to form a multi-PRI RAKE structure.

Figure 4.17: Decision feedback structure

However, the processed signals still suffer from pre-cursor multipath interference except the term of \(j=0\) in (4.35) and (4.36). Therefore, it is possible to minimize the pre-cursor ISI effect by predicting future symbols. As a result, (4.35) is modified to
\[
\tilde{R}_{r+j} = R_{r+j} - \sum_{d=1}^{L-j-1} \tilde{I}_{r+d} H_{d+j} - \sum_{g=1}^{j} \hat{I}_{r+g} H_{j-g}
\]  
(4.37)

with the definition of the predicted symbol \( \hat{I} \) as

\[
\hat{I}_{r+g} = \text{sgn} \left( R_{r+g} H_0^* \big|_{g=1,2,...,L-1} \right)
\]
(4.38),

where the function \( \text{sgn}(\ast) \) represents the hard decision.

Since it requires a feedforward of predetermined information, the improved scheme is named decision feedforward-backward equalization (DFBE). The improved structure is shown in Figure 4.18.
4.5.6 Performance

The frequency domain I-UWB receiver is modeled in Matlab including the front-end and the above signal processing blocks.

As an initial simulation of channel estimation, Figure 4.19 shows the estimated channel response in time domain by the proposed channel estimation method with a PRI of 10 ns that causes significant ISI. The preamble uses a sequence length of $m=25$. The proposed channel estimation method effectively suppresses ISI, and the estimated channel response closely matches the channel response of single pulse without ISI.

![Figure 4.19: Estimated channel response](image)

To evaluate the performance of the proposed equalization scheme, the proposed scheme will be compared with an analog correlator receiver. For fair comparison, the analog correlator receiver experiences no ISI, and our proposed system will experience severe ISI. To obtain an upper bound on performance, the simulation will also consider a
fictional receiver that can capture as much energy from multipaths as a frequency domain receiver captures during a time window. Thus, from the theoretical performance of BPSK, we can expect the performance of the fictional receiver to be

\[ P_b = Q\left(\sqrt{\frac{2T_{\text{window}}}{\text{PRI}}} \epsilon_b / N_0\right) \]  \hspace{1cm} (4.39),

where \( P_b \) is the average probability of error, \( \epsilon_b \) is the energy delivered by the I-UWB signal, and \( T_{\text{window}}/\text{PRI} \) is the portion of energy captured by the frequency domain receiver. This fictional receiver does not encounter any ISI.

There are two factors that degrade performance from the upper boundary. The first is that the receiver cannot fully capture the available signal energy due to the non-equal distribution of the signal energy over the delay spread. The second source of degradation occurs when the wrong decision or wrong prediction is fed through the DFE or DFBE. The performances of DFE and DFBE are shown in Figure 4.20. According to the simulation results as shown in Figure 4.20, DFBE gives better performance than DFE by 1 dB at BER=10^{-2}, Also, DFE and DFBE improve performance over the analog correlator by 6 dB and 5 dB at BER=10^{-2}. 
Figure 4.20: Performance comparison of DFE and DFBE

Beside the two performance degradation factors for the equalizations as explained earlier, two factors affect the performance of the clock recovery block. The first is a BER variation over phase error or time offset. The second is a phase error probability, which can be represented as phase error probability density function (PDF), and it is normally denoted as a steady-state response. For example, we show a BER variation plot at $E_b/N_0 = 9$dB in Figure 4.21. In the plot, a perfect Gaussian monocycle pulse is assumed for both the received signal and the template signal.
Figure 4.21: BER variation $BER(\phi)$ at $E_b/N_0 = 9$dB

As a result, the simulation should prove a nominal BER over phase error predicted as

$$BER = \int_{-\pi}^{\pi} BER(\phi)p(\phi)d\phi$$  \hspace{1cm} (4.40),

where $p(\phi)$ is a phase error PDF. The phase error PDF, $p(\phi)$, is mainly controlled by a loop filter, and it is also a function of the inserted noise variation. It is also worth mentioning that the pulse shape determines the BER variation, $BER(\phi)$. 

4.6 Frequency Domain I-UWB Receiver with 1-bit ADCs

In the previous sections, we have developed a frequency domain I-UWB receiver and improved its performance for high data rates. Now we would like to simplify the design to achieve low power and low cost. Therefore, we introduce a modified frequency domain I-UWB receiver incorporating 1-bit ADCs instead of multi-bit ADCs, and it is named mono-FDR. 1-bit ADCs, or equivalently comparators, are lower in circuit complexity, faster, and much more power efficient as compared to higher resolution ADCs. Further, the 1-bit ADCs are inherently linear and eliminate various non-linear effects such as integral and differential non-linearity errors. This architecture aims to integrate these 1-bit ADCs without significant degradation of system performance. Further, it is expected that the high speed achievable for 1-bit ADCs enables a designer to adopt a higher processing gain to boost the system performance in other applications. Considering the advantages of 1-bit ADCs over multi-bit ADCs, the introduced mono-FDR is a tempting architecture for many low-power applications such as wireless sensor networks and radio frequency identification (RFID).

Section 4.6.1 reviews the architecture of the proposed receiver. Section 4.6.2 describes the operations of the proposed method.

4.6.1 Architecture

The proposed architecture is shown in Figure 4.22. The only difference from the multi-bit ADC version in Figure 4.11 is that the ADCs are replaced with comparators. However, the names of the individual blocks within the energy harvester are changed: the “channel estimator” becomes “a weight function generator”, and the “equalizer” becomes a “correlator.” This is because even though the operations are equivalent, the implications are changed by the 1-bit representation of the received signal.
4.6.2 Operation

An important issue for employment of 1-bit ADCs is the generation of the template signals denoted as the channel profile. Several schemes have been proposed for acquisition of template signals. A simple scheme uses the transmitted pulse shape, but it does not account for the channel conditions and results in poor performance [2]. A better approach, which is considered in this dissertation, is to dynamically generate a template signal during every preamble period.

A template signal can be obtained as the ensemble average of a sequence of received signals during a preamble period. In the case of multi-bit ADCs, the line spectrum of the template signal is the average values of the individual ADC outputs. When 1-bit ADCs are employed, the ADCs capture only the sign bits of the line spectrum. Therefore, the individual ADC outputs fail to yield the line spectrum of the template signal using only the sign bits. To circumvent the problem, the proposed method computes the confidence levels of the individual line spectrum of the template signal and uses these confidence levels as weights in the correlation operation. These confidence intervals will be computed during synchronization so as to add minimal overhead to the packet size.
4.6.3 Confidence Level of the Line Spectrum

The pair of 1-bit ADCs for a filter bank samples only the signs of the real and imaginary spectral components. To make the analysis tractable, it is assumed that the noise of an output of a filter bank is AWGN (additive white Gaussian noise) and the two noise terms of real and imaginary outputs are independent.

The Fourier coefficient extracted from a filter bank $k$ for a received signal $r(t)$ at a certain time under complex AWGN is expressed as (4.41).

$$R_k = A_k e^{j\theta_k} + N_k,$$  

where $N_k = n_k + j\eta_k$ \hspace{1cm} (4.41)

Thus, the real and imaginary signals of a filter bank before sampling can be formulated as below.

$$I_k = A_k \cos \theta_k + n_k$$ \hspace{1cm} (4.42)

$$Q_k = A_k \sin \theta_k + \eta_k$$ \hspace{1cm} (4.43)

The $I_k$ and $Q_k$ terms represent the real and imaginary terms. The PDF of both $n_k$ and $\eta_k$ are $p(n) = \frac{1}{\sqrt{\pi N_0}} e^{-n^2/N_0}$. Therefore, the conditional PDFs of noise $n$, under the transmission of $R_k = A_k e^{j\theta_k}$ are:

$$p(n \mid A_k \cos \theta_k) = \frac{1}{\sqrt{\pi N_0}} e^{-\left(\frac{\pi - A_k \cos \theta_k}{\sqrt{\pi N_0}}\right)^2}$$ \hspace{1cm} (4.44)

$$p(n \mid A_k \sin \theta_k) = \frac{1}{\sqrt{\pi N_0}} e^{-\left(\frac{\pi - A_k \sin \theta_k}{\sqrt{\pi N_0}}\right)^2}$$ \hspace{1cm} (4.45)

The probabilities for detecting the real signal as ‘1’ and ‘-1’ for 1-bit ADCs are obtained as:
\[ P(1 \mid A_k \cos \theta_k) = \int_0^\infty p(n \mid A_k \cos \theta_k) dn \]
\[ = \frac{1}{\sqrt{\pi N_0}} \int_0^\infty \exp \left[ - \frac{(n - A_k \cos \theta_k)^2}{N_0} \right] dn \]
\[ = \frac{1}{\sqrt{2\pi}} \int_{-\frac{A_k \cos \theta_k}{\sqrt{N_0/2}}}^{\infty} e^{-x^2/2} dx \]
\[ = Q\left(-\frac{A_k \cos \theta_k}{\sqrt{N_0/2}}\right) = 1 - Q\left(\frac{A_k \cos \theta_k}{\sqrt{N_0/2}}\right) \]  
(4.46)

\[ P(-1 \mid A_k \cos \theta_k) = \int_{-\infty}^0 p(n \mid A_k \cos \theta_k) dn \]
\[ = Q\left(\frac{A_k \cos \theta_k}{\sqrt{N_0/2}}\right) \]  
(4.47)

In the same manner, the probabilities for detecting the imaginary signal are obtained as:

\[ P(1 \mid A_k \sin \theta_k) = 1 - Q\left(\frac{A_k \sin \theta_k}{\sqrt{N_0/2}}\right) \]  
(4.48)

\[ P(-1 \mid A_k \sin \theta_k) = Q\left(\frac{A_k \sin \theta_k}{\sqrt{N_0/2}}\right) \]  
(4.49)

Therefore, the expected values for the real and imaginary signals for the 1-bit ADC can be calculated from (4.46) to (4.49) and are given below.

\[ E[I_k] = P(1 \mid A_k \cos \theta_k) - P(-1 \mid A_k \cos \theta_k) \]
\[ = 1 - 2Q\left(\frac{A_k \cos \theta_k}{\sqrt{N_0/2}}\right) \]  
(4.50)

\[ E[Q_k] = P(1 \mid A_k \sin \theta_k) - P(-1 \mid A_k \sin \theta_k) \]
\[ = 1 - 2Q\left(\frac{A_k \sin \theta_k}{\sqrt{N_0/2}}\right) \]  
(4.51)
\(E[I_k]\) and \(E[Q_k]\) are the expected values of the real and imaginary terms, respectively. The expected values indicate the confidence level of the spectrum for an extracted Fourier coefficient \(R_k\) and are one for a noiseless channel. To increase the confidence level, the outputs of the 1-bit ADCs are averaged over a preamble sequence for each packet of data. The confidence level is illustrated in Figure 4.23 as dashed area.

![Figure 4.23: Confidence level](image)

The two expected values of a filter bank indicate the confidence level of the spectral component and are called weight terms of the spectral component. The weight \(W^k\) for a filter bank \(k\) is defined as \(W^k = E[I_k] + jE[Q_k]\) for the associated spectral component and these are used for correlation in the next section.

### 4.6.4 Spectral Code Correlation

Instead of performing correlation with the received signal and a template as an analog correlator does, the proposed method performs correlation with the received signal samples and weight terms. This process is called spectral code correlation in this dissertation. This process assumes that the UWB channel performs encoding in a frequency domain, named spectral channel encoding as shown in Figure 4.24.
The *channel spectral code* $S_{ik}$ of a filter bank $k$ for a transmitted data symbol $D_i$ is defined as the outputs of 1-bit ADCs in the following manner.

$$S_{ik} = \text{sgn}(I_i) + j \text{sgn}(Q_i)\big|_{D_i}$$  \hspace{1cm} (4.52)

$$S_i = [S_{i0}^0 \quad S_{i1}^1 \quad \cdots \quad S_{iM-1}^M]$$  \hspace{1cm} (4.53)

$M$ is the total number of the filter banks, and the *symbol code* $S_i$ is the collection of the channel spectral code $S_{ik}$. The weight function $W$ is a collection of weight terms for individual filter banks and is expressed as

$$W = [W^0 \quad W^1 \quad \cdots \quad W^{M-1}]$$  \hspace{1cm} (4.54)

The weight function reflects the confidence level on the individual elements of the symbol code. In (4.55), the correlation is performed between the symbol code $S_i$ and the conjugate version of the weight function $W$ for the transmitted symbol $D_i$. Also, the sign of the real term is examined to estimate the transmitted values.
\[
\hat{D}_i = \text{real} \left\{ S_i W^* \right\} \\
= \text{real} \left\{ \begin{bmatrix} S_i^0 & S_i^1 & \cdots & S_i^{M-1} \end{bmatrix} \begin{bmatrix} W_0^* \\ W_1^* \\ \vdots \\ W^{M-1*} \end{bmatrix} \right\} \\
= \text{real} \left\{ \sum_{m=0}^{M-1} S_i^m W^{m*} \right\} 
\] (4.55)

In (4.55), \( \hat{D}_i \) is the estimated transmit symbol.

### 4.6.5 Performance

We simulated the performance of our UWB receiver for two different cases: 1-bit ADCs and ideal ADCs. We also simulated a system with a conventional analog receiver that uses an analog correlator in an environment without ISI in which all multipath signals die out before the next pulse is received. It should be noted that a spreading gain is not applied to any of the systems. Also, since no ISI is assumed, the simulation does not employ equalization.

- Pulse repetition interval: 10 ns
- Modulation scheme: BPSK (Binary Phase Shift Keying)
- Packet size: 100 Kbits for 1 ms duration
- Preamble size: 1 Kbits for 10 \( \mu \)s duration
- Channel model: CM4 of IEEE 802.15.3a
- Signal bandwidth: 3.1 – 5.16 GHz
- Observation window size: 3 ns
- Number of filter banks: 6

Figure 4.25 shows the simulation results. The simulation results indicate the employment of 1-bit ADCs degrades the performance of our receiver by about only 3 dB
at BER of $10^{-1}$ compared to ideal ADCs. The degradation of the performance by 3 dB should be considered as small, since the quantization noise increases by 6 dB per reduction of one bit. The performance of our receiver with 1-bit ADCs is comparable to that of the analog correlator receiver, even if ISI is not considered for the analog receiver. The superiority of our receiver is attributed to the effectiveness of the RAKE operation in the case of multiple pulses within a time window duration.

![Graph showing Bit Error Rate vs. $E_b/N_0$ (dB)](image)

**Figure 4.25: Performance of our receiver and an analog correlator receiver**

Since the proposed mono-FDR is intended for low-power and low-data rate applications, spreading gain can be considered to overcome any performance degradation incurred by employment of 1-bit ADCs. Furthermore, the proposed mono-FDR can take advantage of a longer time window thanks to the reduced circuit complexity, which implies greater signal energy capture.

Also, we have observed the system performance in cooperating with DFBE and DFE, which are introduced in Section 4.5.5. According to the simulation results, the frequency domain receiver with 1-bit ADCs degrades the performance by around 3dB for
both DFBE and DFE, compared to the frequency domain receiver with ideal ADCs as shown in Figure 4.26. However, the frequency domain receiver with 1-bit ADCs still gives better performance than the conventional analog correlator receiver by 1dB at BER=10⁻¹ even though the analog correlator receiver does not suffer from ISI. If consider the increased circuit complexity and processing cost, the small improvement of performance with DFBE probably is not worth it, so we choose the DFE scheme for the frequency domain receiver with 1-bit ADCs.

Figure 4.26: Performance Simulation Results
Chapter 5:
Conclusion

Compared to narrowband radios, UWB radios have many advantages, such as high data rate, accurate ranging ability, resistance to multi-path interference, and the ability to overlay existing spectrum. Due to the challenges in designing high-speed, wide-bandwidth components, initial implementations of UWB systems were based on high-speed technologies such as SiGe and GaAs, which incur relatively high power dissipation and cost. However, commercial implementations of UWB systems demand low-power and low-cost. Therefore, CMOS is the technology of choice. However, CMOS implementation encounters some major challenges for UWB design. In this dissertation, we have investigated a system-level as well as a circuit-level approach for low-power, low-cost, digital implementation of a CMOS UWB receiver.

In Chapter 3, we introduced a systematic design approach for low power CMOS LNAs targeted towards UWB radios. Our approach has the ultimate goal of accelerating CMOS design cycles for UWB systems. Specifically, we propose a methodology of CMOS LNA design that considers impedance matching as well as noise or power optimization. To verify the methodology, we designed two single-stage LNAs in 0.18\(\mu m\) CMOS technology. Measurements results from fabricated designs indicate that the proposed LNAs could achieve as high as 16 dB power gain and as low as 2.2 dB of noise figure with only 6.4mA current dissipation from a 1.2V supply voltage.

Besides UWB LNA implementation, which is a key part in a receiver chain, we also introduce frequency domain sampling method in Chapter 4. The proposed sampling method is highly effective especially for I-UWB systems, because it can reduce the sampling speed dramatically, and the sampling rate can even be eventually lowered down to the pulse repetition rate. Due to the possibility of low power implementation of UWB radios by the frequency domain approach, it is also adopted in Ad-Hoc sensor network
[78], which limits an available power budget. We also investigated several frequency domain signal processing techniques, such as synchronization, clock recovery, and equalization. These signal processing techniques take advantage of sampling in frequency domain without translation from frequency domain to time domain. Finally, we proposed an all-digital frequency domain receiver that uses only 1-bit ADCs. We concluded that using 1-bit ADCs degrades the BER performance by only 3 dB when compared to using ideal ADCs.

The dissertation has addressed two of the most pressing problems in CMOS implementation of UWB radios viz. extremely high-speed sampling and low noise, low power LNA design. The reduction of sampling speed could be achieved by processing signals in the frequency domain and low-noise, low-power LNAs could be designed based on a systematic optimization procedure. A digital UWB receiver can be implemented in CMOS with the proposed UWB LNA as a RF front-end and multiple filter-banks immediately following the UWB LNA. The reduced length of receiver chain contributes to lower power dissipation and lower overall system noise figure.
A.1 CMOS Operation

There are two major types of transistors implemented in Silicon: the metal-oxide-semiconductor field-effect-transistor (MOSFET) and the bipolar-junction-transistor (BJT) [79], [80], [95]. Although each one offers unique features and areas of application, the MOSFET (or just MOS) is more widely used and presents many advantages over the BJT in many applications.

It requires less silicon area and its fabrication process is relatively simpler. Also, its operation requires less power. It is possible to implement many analog and digital circuits using almost exclusively MOS transistors. All these properties allow packing a large number of devices in a single integrated circuit.

Figure A-1 shows the physical structure of the $n$-channel MOS transistor, or just $n$MOS transistor. The transistor is fabricated in a $p$-type silicon substrate. Two heavily doped $n$-type regions, indicated as $n^+$, are created in the substrate and will act as the source and drain (in terms of structure, source and drain can be interchanged). A thin layer of silicon oxide (SiO$_2$), of thickness $t_{ox}$ (typically between 2 and 50 nm), is formed on the surface of the substrate, between the drain and the source regions. The silicon oxide is an excellent electrical isolator. Metal (or polysilicon, which is conductor) is deposited on top of the oxide layer to form the gate electrode. Metal contacts are also made in the source and drain regions, in addition to contact to the bulk, also known as the substrate or body. Therefore, the four contacts were formed: D-drain, S-source, G-gate and B-bulk.
The gate region has a length $L$ and a width $W$, which are two important design parameters of the MOS transistor. Usually $L$ is in the range of $0.1\mu m$ to $3\mu m$ while $W$ is in the range of $0.2\mu m$ to $100\mu m$.

There is also the $p$-channel MOS transistor, or just $p$MOS transistor, in which the dopings are reversed to the $n$MOS transistor.

Figure A-1: Physical structure of an nMOS transistor
A.2 Forming the Channel

As can be observed from the Figure A-2, the substrate forms \(pn\) junctions with the drain and the source. In normal operation both junctions must be kept reverse-biased, or at least out of the forward condition all the time. Since the drain is biased at a positive voltage, it is only necessary to connect the bulk to the ground in order to keep both junctions cut off.

With no bias applied to the gate, there are two back-to-back diodes between drain and source, and consequently, there is no current. This is true since each \(pn\) junction forms a diode. In fact, the resistance between drain and source under this circumstance is in the range of \(10^{12} \Omega\).

When a positive voltage is applied between gate and source - \(V_{GS}\), holes (which are positively charged) are repelled from the surface of the substrate. As the voltage increases, the surface becomes completely depleted of charge. The voltage at which this occurs is known as threshold voltage – \(V_t\).

If \(V_{GS}\) is further increased, electrons (which are negative charges) accumulate near the surface, under the gate, and an \(n\) region is created, thus forming a channel between drain and source, as indicated in Figure A-2. The channel was formed by inverting the substrate surface from \(p\) type to \(n\) type. Figure A-2 also shows the depletion region that forms around the channel and the two junctions.
The symbols for the nMOS transistor are given in Figure A-3, although other symbols may be found in the literature. The symbol in Figure A-3(a) corresponds to the four terminal connections, and the symbol in Figure A-3(b) corresponds to the three terminal connections, where source and substrate are shorted.
A.3 Triode Condition

Now, if a very small voltage $v_{DS}$ is applied between drain and source, as indicated in Figure A-4, there will be a current flow through the channel. The current through the channel, named drain current - $i_D$ is directly dependent on the voltage $v_{GS}$ and the voltage $v_{DS}$. If $v_{GS}$ increases, the channel becomes deeper and more current can flow. If $v_{DS}$ is increased, based on Ohm’s Law, there will be more current, since the channel behaves as a resistance. If follows that the transistor is operating as a linear resistance whose value is controlled by $v_{GS}$. The resistance is very high for $v_{GS} \leq V_t$ and it decreases as $v_{GS}$ increases. This condition of operation is known as ohmic, linear or triode.

![Figure A-4: Conduction under very small $v_{DS}$](image)
A.4 Saturation Condition

As $v_{DS}$ increases, the difference $v_{DS} - v_{DS}$ becomes smaller at the edge between the gate and the drain diffusion, and therefore the channel becomes shallow. Therefore, the channel assumes a tapered shape, as indicated in Figure A-5. Since the channel becomes smaller at the drain end, its resistance increases, and therefore, the transistor does not operate ideally as a linearly controlled resistor.

At the condition $v_{DS} = v_{GS} - V_t$, the channel ceases to exist at the drain side, as shown in Figure A-6. This situation is known as pinch off. At this point, further increases in $v_{DS}$ moves the end of the channel further away from the drain, as presented in Figure A-7. This condition of operation is referred as saturation, therefore $v_{DS}$ is referred as

$v_{DSAT} = v_{GS} - V_t.$
Once the transistor enters the saturation region of operation, the drain current $i_D$ becomes independent of the $V_{DS}$. 

**Figure A-6:** Conduction under $v_{DS} = v_{GS} - V_t$

**Figure A-7:** Conduction under $v_{DS} > v_{GS} - V_t$
Figure A-8 summarizes the conditions of operation of an nMOS transistor. Close to $v_{DS} = 0$, current $i_D$ is directly proportional to $v_{DS}$ with slope proportional to $v_{GS} - V_t$. As $v_{DS}$ approaches $v_{DS} = v_{GS} - V_t$, the curve of bends because the channel resistance increases. After the $v_{DS} = v_{GS} - V_t$, the current becomes independent of $v_{DS}$.

![Figure A-8: Operation condition of an nMOS transistor](image)
A.5 Deriving the $i_D - v_{DS}$ Relationship

Consider the biasing depicted in Figure A-9. Since the channel potential varies from zero at the source to $v_{DS}$ at the drain, the local voltage difference between gate and the channel varies from $v_{GS}$ to $v_{GS} - v_{DS}$. Therefore, the channel density, or charge per unit length, is given as:

$$Q_d(x) = WC_{ox}[v_{GS} - v(x) - V_f]$$  \hspace{1cm} (A.1)

where $v(x)$ is the potential at $x$ and $C_{ox}$ is the capacitance, per unity area, formed by the gate and the channel.

![Figure A-9: Biasing of an nMOS](image)

Since, by definition, current is proportional to charge time velocity, and considering the current is the same along the channel, then:

$$i_D = -WC_{ox}[v_{GS} - v(x) - V_f]v$$  \hspace{1cm} (A.2)

The minus signal is due to the negative charge of electrons. The velocity of carriers at low fields is the product of mobility ($\mu$) and the electric field ($E$). Noting that $E(x) = -dV/dx$ and representing the electrons mobility by $\mu_n$, then expression (A.2) can be rewritten as:

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\[ i_D = WC_{ox}[\psi_{GS} - \psi(x) - \nu_i] \mu_n \frac{dV(x)}{dx} \]  
\hspace{1cm} \text{(A.3)}

Now integrating along the channel, one obtains:
\[ \int_0^L i_D dx = \int_0^{\nu_{sat}} WC_{ox}[\psi_{GS} - \psi(x) - \nu_i] \mu_n dV(x) \]  
\hspace{1cm} \text{(A.4)}

Thus, the expression for the drain current in the triode region is:
\[ i_D = \mu_n C_{ox} \frac{W}{L} [(\psi_{GS} - \nu_i)\nu_{DS} - \frac{\nu_{DS}^2}{2}] \]  
\hspace{1cm} \text{(A.5)}

The value of the current for the saturation operation can be obtained by replacing \( \nu_{DS} = \psi_{GS} - \nu_i \) into expression (A.5), as:
\[ i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (\psi_{GS} - \nu_i)^2 \]  
\hspace{1cm} \text{(A.6)}

As described earlier, the current does not depend on \( \nu_{DS} \). It can be observed from expressions (A.5), and (A.6) that the current is proportional to the ratio \( \frac{W}{L} \), which is known as the aspect ratio. The designer can alter the aspect ratio to obtain the desired \( i-V \) characteristic.

Observe that expression (A.6) was obtained using the value of \( L \), as given in Figure A-9. Nevertheless, when the transistor is saturated, the channel becomes shorter, as shown in Figure A-7. A reduction in the length of the channel, known as channel length modulation, means a variation in the resistance, and therefore a variation in the current \( i_D \).

Expression (A.6) can be modified in order to include the variation in the channel length, represented as \( L - \Delta L \), as:
\[ i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L - \Delta L} (\psi_{GS} - \nu_i)^2 \]  
\hspace{1cm} \text{(A.7)}

\[ i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L - (\Delta L / L)} (\psi_{GS} - \nu_i)^2 \]

which can be approximated to:
\[ i_D \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( 1 + \frac{\Delta L}{L} \right) (\psi_{GS} - \nu_i)^2 \]  
\hspace{1cm} \text{(A.8)}
Since $\Delta L/L$ is proportional to $\nu_{DS}$ (the larger $\nu_{DS}$ the larger will be $\Delta L$), then:

$$i_D \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (\nu_{GS} - \nu_t)^2 (1 + \lambda \nu_{DS})$$  \hspace{1cm} (A.9)$$

where $\lambda$ is the parameter of proportionality.

The effect of channel length modulation can be seen in the $i_D - \nu_{DS}$ characteristic of a MOS transistor shown in Figure A-10. The dependence of $\nu_{DS}$ on $i_D$ in the saturation region can be seen is represent by $(1 + \lambda \nu_{DS})$ in expression (A.9) and can be observed in Figure A-10.

![Figure A-10: Effect of channel modulation on saturation current](image)

An extrapolation of $i_D - \nu_{DS}$ intercepts the $\nu_{DS}$ axis at $\nu_{DS} = - V_A$, known as Early voltage. For a given process, $V_A$ is proportional to $L$, selected by the designer. Typically, $V_A$ is in the range of 5 V/\(\mu\)m to 50 V/\(\mu\)m.
A.6 Output Resistance

Figure A-10 and expression (A.9) show that an increase in $v_{DS}$ causes an increase in $i_D$, meaning a resistive behavior. The value of the resistance is given as:

$$
\frac{\partial i_D}{\partial v_{DS}}^{-1} = \left[ \frac{\lambda}{2} \mu_C \frac{W}{L} (v_{GS} - V_t)^2 \right]^{-1}
$$

(A.10)

which can be simplified to:

$$
r_o = \frac{1}{\lambda i_D} = \frac{V_A}{i_D}
$$

(A.11)

Therefore, a MOS transistor in the saturation region is not totally independent of $v_{DS}$ and presents an output impedance given by (A.11).

Considering the transistor operating in the triode region, as given by expression (A.5), if the value of $v_{DS}$ is sufficiently small, $v_{DS}^2$ can be neglected, and therefore:

$$
\frac{\partial i_D}{\partial v_{DS}} = \frac{\mu_n C_s W}{L} \left[ (v_{GS} - V_t) v_{DS} \right]
$$

(A.12)

This relationship represents the behavior of the MOS transistor as a linear resistance whose value is controlled by $v_{GS}$, as given by:

$$
\frac{v_{DS}}{i_D} = \left[ \frac{\mu_n C_s W}{L} \left( v_{GS} - V_t \right) \right]^{-1}
$$

(A.13)
A.7 Transconductance

The large signal behavior of a MOS transistor in the saturation region is given by expression (A.6). Nevertheless, for a given biasing, the designer may be interested in the small signal behavior of the transistor. For a given small variation in the $v_{GS}$, around the biasing, there will be a variation in the $i_D$ current, given by the transconductance, as:

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS}=v_{GS}}$$  \hspace{1cm} (A.14)

which results in:

$$g_m = \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)$$  \hspace{1cm} (A.15)

Observe the transconductance depends on the ratio $W/L$ and on the value of $v_{GS}$, and they can be controlled by the designer. By using expression (A.6), then expression can be written as:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} i_D}$$  \hspace{1cm} (A.16)

In this case, the transconductance depends on the ratio $W/L$ and the $i_D$ current. That expression can be written also as:

$$g_m = 2 \frac{i_D}{(v_{GS} - V_t)}$$  \hspace{1cm} (A.17)

It clearly does not depend on ratio $W/L$ but it depends on both $v_{GS}$ and $i_D$. 

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A.8 Body Effect

In many circuits, the substrate and the source are not at the same potential, as it is possible to stack transistors. In that case, the substrate is at lower potential than the source, and therefore the source-substrate junction becomes reversed biased. This reverse biasing widens the depletion layer, which in turn reduces the channel depth.

The effect of the bulk-source voltage \( V_{SB} \) can be easily represented by a change in the threshold voltage \( V_t \), as given by:

\[
V_t = V_{t0} + \gamma \left[ \sqrt{2 \phi_f + V_{SB}} - \sqrt{2 \phi_f} \right] \quad (A.18)
\]

where \( V_{t0} \) is the threshold voltage for \( V_{SB} = 0 \), \( \phi_f \) is a physical parameter (usually \( 2 \phi_f = 0.6V \)) and \( \gamma \) is a fabrication-process parameter given by:

\[
\gamma = \frac{\sqrt{2qN_A \varepsilon_s}}{C_{ox}} \quad (A.19)
\]

where \( q \) is the electron charge \( (1.6 \times 10^{19} \text{ C}) \), \( N_A \) is the doping concentration of the substrate and \( \varepsilon_s \) is the permittivity of silicon \( (1.17 \varepsilon_0 = 1.17 \times 8.854 \times 10^{-14} = 1.04 \times 10^{-12} \text{ F/cm}) \).

Any signal between substrate and source promotes a drain current component. The substrate acts as a second gate, and in turn will present a corresponding transconductance, named body transconductance, given as:

\[
g_{mb} = \left. \frac{\partial i_D}{\partial V_{DS}} \right|_{V_{GS}=V_{Jac}} \quad (A.20)
\]

From expressions (A.6), (A.17), and (A.18), then it is possible to state that:

\[
g_{mb} = \chi g_m \quad (A.21)
\]

where \( \chi \) is given by:

\[
\chi = \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} \quad (A.22)
\]

And it is in the range of 0.1 to 0.3.
A.9 Small Signal Model

Considering the output impedance, the transconductance and the body effect, the small signal model of an $n$MOS transistor is given by Figure A-11, known as hybrid-$\pi$ model.

If the source and the substrate are at the same potential, then the model can be simplified, as the term $g_{mb}V_{bs}$ goes to zero. The simplified hybrid-$\pi$ model is shown in Figure A-12.
## A.10 Summary of nMOS

Table A-1 summarizes the main nMOS equations.

### Table A-1: Summary of nMOS equations

<table>
<thead>
<tr>
<th>Condition</th>
<th>( v_{DS} \geq v_{GS} - V_t )</th>
</tr>
</thead>
<tbody>
<tr>
<td>i-v characteristic</td>
<td>( i_D \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2 )</td>
</tr>
<tr>
<td>Output resistance</td>
<td>( r_o = \frac{1}{\lambda i_D} = \frac{V_A}{i_D} )</td>
</tr>
<tr>
<td>Saturation</td>
<td></td>
</tr>
<tr>
<td>Transconductance</td>
<td>( g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L}} i_D )</td>
</tr>
<tr>
<td></td>
<td>( g_m = \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t) )</td>
</tr>
<tr>
<td></td>
<td>( g_m = 2 \frac{i_D}{(v_{GS} - V_t)} )</td>
</tr>
<tr>
<td>Body transconductance</td>
<td>( g_{mb} = \chi g_m = \frac{\gamma}{2\sqrt{2\phi} + V_{SB}} g_m )</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Condition</th>
<th>( v_{DS} &lt; v_{GS} - V_t )</th>
</tr>
</thead>
<tbody>
<tr>
<td>i-v characteristic</td>
<td>( i_D = \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t) v_{DS} - \frac{v_{DS}^2}{2} )</td>
</tr>
<tr>
<td>Output resistance</td>
<td>( r_{linear} = \frac{v_{DS}}{i_D} = \left[ \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t) \right]^{-1} )</td>
</tr>
<tr>
<td>Triode</td>
<td></td>
</tr>
<tr>
<td>Threshold voltage</td>
<td>( V_t = V_{t0} + \gamma \left[ \sqrt{2\phi} + V_{SB} - \sqrt{2\phi} \right] )</td>
</tr>
</tbody>
</table>
A.11 pMOS Transistor

In a pMOS transistor, a p channel is formed on an n substrate. Therefore, its operation is virtually the same as the nMOS transistor, except that all voltages and currents are opposite as in the nMOS transistor. Figure A-13 shows the symbols for the nMOS transistor, although other symbols may be found in the literature. The symbol in Figure A-13(a) corresponds to the four terminal connection, and the symbol in Figure A-13(b) corresponds to the three terminal connection, where source and substrate are shorted.

Figure A-13: Symbols for pMOS transistor
Appendix B - RF CMOS MODEL

The structure and the operation of a MOS transistor present parasitic capacitances that limit its frequency of operation [81]. The parasitic capacitances may result from the capacitor formed between the gate and the channel, between gate and source/drain, and between drain/source and substrate.

B.1 Gate Capacitances

The gate, the dielectric and the channel form a capacitor. When the transistor is working in the triode region with a small voltage $v_{DS}$, the channel will be of uniform depth, as shown in Figure A-4. Therefore, the gate-channel capacitance can be considered equally divided between the source and the drain, and their values are:

$$C_{gs} = C_{gd} = \frac{1}{2}WLC_{ox} \quad (B.1)$$

When the transistor is working in the saturation region, the channel presents a tapered shape and it is pinched off at the drain end, as presented in Figure A-7. It can be seen that the gate to channel capacitance is almost entirely modeled at the source, since the drain does not present a channel. It can be shown that the capacitances are:

$$C_{gs} = \frac{2}{3}WLC_{ox} \quad (B.2)$$

$$C_{gd} \approx 0 \quad (B.3)$$

If the transistor is cut off, there is no capacitance between gate and channel, since there is no channel for cut off. The entire capacitance is then between the gate and the substrate, therefore:

$$C_{gs} = C_{gd} = 0 \quad (B.4)$$

$$C_{gb} = WLC_{ox} \quad (B.5)$$
As can be observed from Figure A-1, the gate extends over the drain and the source areas. Therefore, there is an overlapping capacitance between the gate and the drain/source. Denoting the overlapping length by $L_{ov}$, then the overlap capacitance can be seen to be:

$$C_{gs_{ov}} = C_{gd_{ov}} = W L_{ov} C_{ox}$$  \hspace{1cm} (B.6)

For modern processes, $L_{ov}$ is usually in the range of 5% to 10% of $L$. 

B.2 Junction Capacitances

As shown by Figure A-2 there are two reversed biased junctions formed between the substrate and source/drain. Each junction consists of two semiconductors (drain/source and the substrate) and the depletion layer, thus forming a capacitor. The source-substrate capacitance can be found to be:

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{V_{SB}}{V_0}}}$$  \hspace{1cm} (B.7)

where $V_0$ is the junction built-in voltage (0.6 V to 0.8 V), $V_{SB}$ is the magnitude of the reversed bias voltage and $C_{sb0}$ is the capacitance at zero reverse bias voltage.

By the same way, the drain-substrate capacitance is given by:

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{V_0}}}$$  \hspace{1cm} (B.8)
**B.3 High Frequency Model**

The small signal model of the MOS transistor given in Figure A-11 can be updated to include the gate and the junction capacitances, as presented in Figure B-1 [82], [96]. Although this model represents the transistor for high frequencies, it is very complex for manual analysis.

![Diagram of Hybrid-π model including parasitic capacitances](image1)

**Figure B-1: Hybrid-π model including the parasitic capacitances**

If the source and the substrate are shorted, the model can be greatly simplified, as shown in Figure B-2.

![Diagram of Simplified high frequency model](image2)

**Figure B-2: Simplified high frequency model for source and substrate shorted.**
B.4 Unity Gain Frequency

An important figure of merit for the MOS transistor is the unity gain frequency that is defined as the frequency in which the short circuit current gain becomes unit. This definition is based in the common source configuration, as shown in Figure B-3.

![Figure B-3: Circuit model used to obtain the unity gain frequency](image)

The current $I_o$ in the short circuit is given by:

$$I_o = g_m V_{gs} - sC_{gs}V_{gs} \approx g_m V_{gs} \quad (B.9)$$

The approximation is due to the fact that $C_{gd}$ is very small and can be neglected. Also, from the circuit, $V_{gs}$ can be expressed as:

$$V_{gs} = \frac{I_i}{s(C_{gs} + C_{gd})} \quad (B.10)$$

Therefore, from expressions (B.9) and (B.10):

$$\frac{I_o}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})} \quad (B.11)$$

Since the magnitude of $\frac{I_o}{I_i}$ should be 1, as per definition, and considering physical frequencies ($s=j\omega$), then:

$$\omega_r = \frac{g_m}{(C_{gs} + C_{gd})} \quad (B.12)$$

Therefore, the unity gain frequency is:
$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$  \hspace{1cm} (B.13)

As can be observed, the unity gain frequency is directly proportional to $g_m$ and inversely proportional to the internal capacitances. Therefore, in terms of frequency response the transistor should have large $g_m$ and small capacitances.
Appendix C - RF CMOS NOISE MODEL

The two most important types of noise in MOS devices are the $1/f$ noise and the thermal noise [83],[84].

C.1 Thermal Noise

The main source of thermal noise in a MOS transistor is due to the resistive channel in the active region, and has a value of:

$$i_d^2 = 4kT \gamma g_m$$

(C.1)

where $k$ is the Boltzmann’s constant (about $1.38 \times 10^{-23} \text{ J/K}$), $T$ is the absolute temperature in kelvins and $\gamma$ is a constant that is approximately $2/3$ for long channel transistors and increase to the range $1-2$ for short channel devices.

The other source of thermal noise is the gate. Fluctuation in the channel potential couples capacitively into the gate terminal, which in turn translates into a noise gate current. Noise gate current can also be produced by the resistive material of the gate. This total noise gate can be ignored at low frequencies but becomes significant at high frequencies as it is the case of RF circuits. It has been shown the gate noise may be expressed as:

$$i_g^2 = 4kT \delta g_g$$

(C.2)

where $\delta$ is approximately $4/3$ for long channel transistors and increase to the range $2-4$ for short channel devices, and $g_g$ is given by:

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_m}$$

(C.3)

Mostly of the time, instead of using a current source at the gate, it is more convenient to consider an equivalent voltage source. The equivalent voltage source of expressions (C.2) and (C.3) is given by:
\[ v_g^2 = 4kT \delta r_g \]  \hspace{1cm} (C.4)

where \( r_g \) is given by:

\[ r_g = \frac{1}{5g_m} \]  \hspace{1cm} (C.5)
C.2 1/f Noise

The 1/f noise, also known as flicker noise or pink noise, arises mainly due to the surface imperfections that can trap and release charges. Since MOS devices are naturally surface devices, they produce much more 1/f than bipolar devices (which are bulk devices). This noise is also generated by defects and impurities that randomly trap and release charges. The trapping times are statistically distributed in such a way that lead to a 1/f noise spectrum.

The 1/f noise can be modeled by a voltage source in series with the gate, of value:

\[ V_f = \frac{\beta}{WLC_{ox}f} \quad (C.6) \]

For pMOS devices, \( \beta \) is typically about \( 10^{-28} \, C^2/m^2 \), but it can be up to 50 times larger for nMOS devices.

As can be observed from expression (C.6), the 1/f noise is smaller for larger devices. This occurs because the large capacitance smooths the fluctuation in the channel charge. Therefore, in order to achieve good 1/f performance, larger devices should be used.

The 1/f can also be modeled as a current source at the drain whose value is:

\[ I_f = \frac{\beta g_m^2}{WLC_{ox}^2 f} \approx \frac{\beta}{f} \omega_f^2 A \Delta f \quad (C.7) \]

where \( A \) is the area of the gate.
C.3 Noise Model

The noise model of an nMOS transistor is presented in Figure C-1, where the transistor is considered noiseless [85]. The decision of placing the noise sources as a voltage source at the gate, or as a current source at the drain is just a matter of convenience according to the circuit under analysis. As an example, the values of Figure C-1 could be:

\[ v^2 = v_g^2 = 4kT \delta r_g \]  \hspace{1cm} (C.8)

\[ i^2 = i_f^2 + i_j^2 = 4kT \gamma g_m + \frac{\beta g_m^2}{WLC_{ox,f}} \]  \hspace{1cm} (C.9)

![Figure C-1: Noise model of an nMOS transistor](image-url)
Appendix D - INDUCTIVE SOURCE DEGENERATION

The equivalent AC model of CMOS with inductive source degenerative topology is shown in Figure D-1 [86].

![Diagram of Equivalent AC model of inductive source degenerative topology]

Figure D-1: Equivalent AC model of inductive source degenerative topology

In Figure D-1, $L_s$ is inserted to improve linearity [87]. However, as one can notice from Figure D-1, as $L_s$ increases, $v_x$ also increases and therefore $v_{gs}$ is reduced, which means overall gain is decreased by the increased negative feedback, $v_x$ [88].

Since its input impedance is defined as $Z_{in} = v_{in}/i_{in} = v_{in}/I_g$, $v_{in}$ and $i_g$ should be defined. Due to the negative feedback caused by $L_s$, the input voltage, $v_{in}$ is

$$v_{in} = v_{gs} + v_x \quad \text{(D.1)}$$

Also, $v_{in}$ and $v_x$, which is the voltage at the point $x$ are

$$v_{gs} = \frac{i_g}{sC_{gs}} \quad \text{(D.2)}$$
\[ v_x = sL_i \]

(D.3)

Where \( i_x \) is

\[
    i_x = i_g + g_m v_{gs} \\
    = i_g + g_m \frac{i_g}{sC_{gs}} \\
    = i_g \left( 1 + \frac{g_m}{sC_{gs}} \right)
\]

(D.4)

Therefore, from (D.1) and (D.4), the input impedance \( Z_{in} \) is

\[
    Z_{in} = \frac{v_m}{i_g} \\
    = \frac{i_g}{sC_{gs}} + sL_i i_g \left( 1 + \frac{g_m}{sC_{gs}} \right) \\
    = \frac{1}{sC_{gs}} + sL_i + \frac{g_m L_i}{C_{gs}}
\]

(D.5)

According to (D.5), the equivalent circuit of the input impedance is a RLC series connection as shown in Figure D-2.

Figure D-2: Equivalent input impedance of inductive source degenerative
Appendix E - UWB CHANNEL MODEL

E.1 Saleh-Valenzuela Model

Saleh-Valenzuela (S-V) model is developed based on indoor multipath propagation measurement using 10 ns, 1.5 GHz, radar-like pulse with a time resolution of about 5 ns in a medium-sized office building [89]. In this model, the received signal rays (paths) arrive in clusters. Each received ray has uniformly distributed phase and Rayleigh distributed amplitude with a variance that decays exponentially with cluster and ray delays.

The cluster arrival times, which are the arrival times of the first rays of the clusters, are modeled as a Poisson arrival process with a fixed rate \( \Lambda \). Within each cluster, subsequent rays also arrive according to a Poisson process with a different fixed rate \( \lambda \). Typically, each cluster consists of many rays, and thus \( \lambda >> \Lambda \). The arrival time of the first cluster, \( T_0 \), and the arrival time of the first ray within the \( l \)th cluster, \( \tau_{0l} \), are defined as 0. Therefore, the cluster arrival time, \( T_l \), and ray arrival time, \( \tau_{kl} \), are described by the independent inter-arrival exponential probability density functions as given in (E.1) and (E.2).

\[
p(T_l|T_{l-1}) = \Lambda \exp[-\Lambda(T_l - T_{l-1})], \quad l > 0 \quad \text{(E.1)}
\]

\[
p(\tau_{kl}|\tau_{(k-1)l}) = \lambda \exp[-\lambda(\tau_{kl} - \tau_{(k-1)l})], \quad k > 0 \quad \text{(E.2)}
\]

The channel impulse response is given by

\[
h(t) = \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \beta_{kl} e^{j\theta_{kl}} \delta(t - T_l - \tau_{kl}) \quad \text{(E.3)}
\]

where \( \theta_{kl} \) is uniformly distributed random variable over \([0, 2\pi]\), and \( \beta_{kl} \) is Rayleigh distributed random variable whose mean square value \( E\{|\beta_{kl}|^2\} \) is defined as

\[
E\{|\beta_{kl}|^2\} \equiv E\{\beta^2(T_l, \tau_{kl})\} = E\{\beta^2(0,0)\} \cdot e^{-T_l/\Gamma} e^{-\tau_{kl}/\gamma} \quad \text{(E.4)}
\]
where $E_{\beta^2(0,0)}$ is the average power gain of the first ray of the first cluster, and $\Gamma$ and $\gamma$ are power-delay time constant for the clusters and the rays, respectively.
E.2 Intel UWB Channel Model

Intel proposed a modified S-V model with their measured data. They used frequency sweep from 2 ~ 8 GHz providing a minimum path resolution of 167 ps in their measurements. Distances from 1 ~ 20 meters were considered, which includes both line of sight (LOS) and non-line of sight (NLOS). Intel model employs a lognormal distribution rather than a Rayleigh distribution for the multipath gain magnitude, as the observations show that the lognormal distribution better fits the measurement data. In addition, independent fading is assumed for each cluster as well as each ray within the cluster [33].

Therefore, the channel impulse response can be expressed as

\[ h(t) = X \sum_{l=0}^{L} \sum_{k=0}^{K} \alpha_{k,l} \delta(t - T_l - \tau_{k,l}) \]  

(E.5)

where \( \alpha_{k,l} \) is the multipath gain coefficient, \( T_l \) is the delay of the \( l \)th cluster, \( \tau_{k,l} \) is the delay of the \( k \)th multipath component relative to the \( l \)th cluster arrival time, and \( X \) represents the log-normal shadowing. By definition, \( \tau_{0,l} \) is 0, and the distribution of cluster arrival time and the ray arrival time follow (E.1) and (E.2), respectively.

The channel coefficient \( \alpha_{k,l} \) is defined as

\[ \alpha_{k,l} = p_{k,l} \xi_l \beta_{k,l} \]  

(E.6)

where \( p_{k,l} \) is 1 or –1 with equal probability to account for signal inversion due to reflections, \( \xi_l \) reflects the fading associated with the \( l \)th cluster, and \( \beta_{k,l} \) corresponds to the fading associated with the \( k \)th ray of the \( l \)th cluster. \( \xi_l \) and \( \beta_{k,l} \) follow the lognormal distribution given in (E.7).

\[ 20\log_{10}(\xi_l \beta_{k,l}) \sim \text{Normal}(\mu_{k,l}, \sigma_1^2 + \sigma_2^2), \quad \text{or} \quad |\xi_l \beta_{k,l}| = 10^{(\mu_{k,l} + n_1 + n_2)/20} \]  

(E.7)

where \( n_1 \sim \text{Normal}(0, \sigma_1^2) \) and \( n_2 \sim \text{Normal}(0, \sigma_2^2) \) are independent and correspond to the fading on each cluster and ray, respectively. The mean square value of the channel coefficient \( E[\alpha_{k,l}^2] \) is defined as
\[ E \{ \alpha_{k,l}^2 \} = E \left\{ \left| \tilde{x}_{k,l} \beta_{k,l} \right|^2 \right\} = \Omega_0 e^{-T_i/\Gamma} e^{-\tau_{k,l}/\gamma} \]  
(E.8)

where \( \Omega_0 \) is the mean energy of the first ray of the first cluster, and \( \Gamma \) and \( \gamma \) are power-delay time constant for the clusters and the rays, respectively. \( \mu_{k,l} \) is given as

\[ \mu_{k,l} = \frac{10 \ln(\Omega_0) - 10 T_i / \Gamma - 10 \tau_{k,l} / \gamma - (\sigma_1^2 + \sigma_2^2) \ln(10)}{\ln(10)} \]  
(E.9)

Finally, as the log-normal shadowing of the total multipath energy is captured by the term, \( X \), the total energy contained in the terms \( \alpha_{k,l} \) is normalized to unity. This shadowing term is characterized as

\[ 20 \log_{10}(X) \propto \text{Normal}(0, \sigma_X^2) \]  
(E.10)

Intel model generates a real channel impulse response with given parameters. Intel proposed four sets of default parameters based on their measurement data. Table E-1 summarizes the input parameters and their default values. Default parameter set #1 (CM1) is based on LOS (0–4m) channel measurements, set #2 (CM2) is based on NLOS (0–4m), set #3 (CM3) is based on NLOS (4–10m), and set #4 (CM4) is generated to fit a 25 nsec RMS delay spread to represent an extreme NLOS multipath channel. These characteristics are obtained with sampling period of 167 psec.
### Table E-1: Parameter set for Intel UWB channel model

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Description</th>
<th>Unit</th>
<th>Default set #1</th>
<th>Default set #2</th>
<th>Default set #3</th>
<th>Default set #4</th>
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<tr>
<td>cluster_lambda</td>
<td>cluster arrival rate</td>
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<td>0.4</td>
<td>0.0667</td>
<td>0.0667</td>
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<td>0.5</td>
<td>2.1</td>
<td>2.1</td>
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<tr>
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<td>5.5</td>
<td>14.00</td>
<td>24.00</td>
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<tr>
<td>ray_decay</td>
<td>ray decay factor</td>
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<td>6.7</td>
<td>7.9</td>
<td>12</td>
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<tr>
<td>cluster_sigma</td>
<td>lognormal fading term for cluster</td>
<td>dB</td>
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<td>4.8/$\sqrt{2}$</td>
<td>4.8/$\sqrt{2}$</td>
<td>4.8/$\sqrt{2}$</td>
</tr>
<tr>
<td>ray_sigma</td>
<td>lognormal fading term for ray</td>
<td>dB</td>
<td>4.8/$\sqrt{2}$</td>
<td>4.8/$\sqrt{2}$</td>
<td>4.8/$\sqrt{2}$</td>
<td>4.8/$\sqrt{2}$</td>
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</table>

Figure E-1 through Figure E-8 present the impulse response and the power delay profile of the Intel model with the default parameter sets.
Figure E-1: Impulse response with parameter set #1

Figure E-2: Power delay profile with parameter set #1

Figure E-3: Impulse response with parameter set #2

Figure E-4: Power delay profile with parameter set #2

Figure E-5: Impulse response with parameter set #3

Figure E-6: Power delay profile with parameter set #3
Figure E-7: Impulse response with parameter set #4

Figure E-8: Power delay profile with parameter set #4
Bibliography


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About the Author

Hyung-Jin Lee was born in Seoul, Korea on May 14, 1973. He received a Bachelor of Science in Electrical and Electric Engineering from Hanyang University in Seoul, Korea in February 2000. He also graduated with a Master of Science in Electrical Engineering from Virginia Tech in May 2003. From 1999 to 2000, he was a Senior Engineer in NDream, Inc. in Seoul, Korea, and he was in charge of developing human voice recognition systems with speaker dependent and independent recognition algorithm, he developed.

Since 2000, he has worked under Dr. Dong Ha’s advisory at the Virginia Tech VLSI for Telecommunications (VTVT) laboratory and researched low-power, high-performance CMOS radio frequency integrated circuit (RFIC) design, high speed CMOS analog integrated circuit design and system level architectures especially aimed for Ultra Wideband (UWB) CMOS communication systems. His current interests include gigahertz CMOS RFIC design for applications such as high data rate wireless personal area network (WPANs) and radio frequency identification (RFID) with UWB technique.

During his Ph.D. work, he published four IEEE conference papers regarding to CMOS RFIC design, and over a dozen IEEE conference papers in regard to low power VLSI design for communication systems. One of his papers appeared in IEEE International Solid-State Circuit Conference in 2006. He has contributed a couple of magazine article, and also applied for a couple of patent disclosures relating to his research.

He plans to graduate in the spring of 2006. After receiving his Ph.D. degree, he is arranged to join Intel Inc. in Hillsboro, Oregon.