Multiphase Voltage Regulator Modules with Magnetic Integration to Power Microprocessors

Peng Xu

Dissertation submitted to the Faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in
Electrical Engineering

Fred C. Lee, Chairman

Dan Y. Chen                Jason Lai
Alex Q. Huang              Guo-Quan Lu

January 15, 2002
Blacksburg, Virginia
Multiphase Voltage Regulator Modules with Magnetic Integration to Power Microprocessors

by

Peng Xu

Fred C. Lee, Chairman

Electrical Engineering

(ABSTRACT)

Advances in very large scale integration (VLSI) technologies impose challenges for voltage regulator modules (VRM) to deliver high-quality power to modern microprocessors. As an enabling technology, multiphase converters have become the standard practice in VRM industry. The primary objectives of this dissertation are to develop advanced topologies and innovative integrated magnetics for high-efficiency, high-power-density and fast-transient VRMs. The optimization of multiphase VRMs has also been addressed.

Today’s multiphase VRMs are almost universally based on the buck topology. With increased input voltage and decreased output voltage, the multiphase buck converter suffers from a very small duty cycle and cannot achieve a desirable efficiency. The multiphase tapped-inductor buck converter is one of the simplest topologies with a decent duty cycle. However, the leakage inductance of its tapped inductors causes a severe voltage spike problem. An improved topology, named the multiphase coupled-buck converter, is proposed. This innovative topology enables the use of a larger duty cycle
with clamped device voltage and recovered leakage energy. Under the same transient responses, the multiphase coupled-buck converter has a significantly better efficiency than the multiphase buck converter.

By integrating all the magnetic components into a single core, in which the windings are wound around the center leg and the air gaps are placed on the two outer legs, it is possible for multiphase VRMs to further improve efficiency and cut the size and cost. Unfortunately, this structure suffers from an undesirable core structure and huge leakage inductance. An improved integrated magnetic structure is proposed to overcome these limitations. All the windings are wound around the two outer legs and the air gap is placed on the center leg. The improved structure also features the flux ripple cancellation in the center leg and strongly reverse-coupled inductors. Both core loss and winding loss are reduced. The steady-state current ripples can be reduced without compromising the transient responses. The overall efficiency of the converter is improved. The input inductor can also be integrated in the improved integrated magnetic structure.

Currently, selecting the appropriate number of channels for multiphase VRMs is still an empirical trial-and-error process. This dissertation proposes a methodology for determining the right number of channels for the optimal multiphase design. The problem formulation and general method for the optimization are proposed. Two examples are performed step by step to demonstrate the proposed optimization methodology. Both are focused on typical VRM 9.0 designs for the latest Pentium 4® microprocessors and their results are compared with the industry practice.
To my wife

Xiling
ACKNOWLEDGMENTS

I would like to express my sincere appreciation to my advisor, Dr. Fred C. Lee for his guidance, encouragement and support. Dr. Lee’s extensive vision and creative thinking have been the source of inspiration for me throughout this work. It was an invaluable learning experience to be one of his students. From him I have learned not only the extensive knowledge, but also the careful research attitude.

I am grateful to my committee members, Dr. Dan Y. Chen, Dr. Jason Lai, Dr. Alex Q. Huang and Dr. Guo-Quan Lu for their valuable suggestions and numerous help. I appreciate Dr. Dushan Boroyevich and Dr. Daan Van Wyk for their help in my CPES work.

It has been a great pleasure to work in the Center for Power Electronics Systems (CPES). I would like to acknowledge the CPES administrative and management staff, Ms. Teresa Shaw, Ms. Linda Gallagher, Ms. Lida Fitzgerald, Ms. Trish Rose, Ms. Ann Craig, Ms. Marianne Hawthome, Ms. Elizabeth Tranter, Ms. Lesli Farmer, Mr. Robert Martin, Mr. Steve Z. Chen, Mr. Dan Huff, Mr. Gary Kerr, Mr. Jeffery Baston, Mr. Mike King and Mr. Jamie Evans for their countless help.

I would like to thank my colleagues, Dr. Jinrong Qian, Dr. Qiong Li, Dr. Richard Zhang, Dr. Kunrong Wang, Dr. Kun Xing, Dr. Budong You, Dr. Jindong Zhang, Dr. Fengfeng Tao, Dr. Xingzhu Zhang, Dr. Dehong Xu, Dr. Weiyun Chen, Mr. Qun Zhao,
Mr. David Wen, Mr. Deng-Ming Peng, Mr. Wei Dong, Mr. Zhou Chen, Mr. Francisco Canales, Mr. Peter Barbosa, Mr. Yuanxuan Hu, Mr. Yong Li, Mr. Song Qu, Mr. Wenkang Wang, Mr. Sihua Wen, Mr. Rengang Chen, Mr. Yin Liu, Mr. Wei Xu, Miss Jinghong Guo, Mr. Zhenxue Xu and Mr. Bing Lu. Their friendships and help have made my stay at CPES pleasant and enjoyable.

I am especially indebted to my teammates in the VRM group, Dr. Xunwei Zhou, Dr. Pitleong Wong, Dr. Ming, Xu, Mr. Ho-Pu Wu, Mr. Jiabin Chen, Mr. Luca Amoroso, Mr. Bo Yang, Mr. Xiaowu Sun, Mr. Kaiwei Yao, Mr. Yuhui Chen, Mr. Faruk Nome, Mr. Jia Wei, Mr. Mao Ye, Mr. Yu Meng, Mr. Yang Qiu, Mr. Yuancheng Ren, Mr. Shuo Wang, Mr. Kisun Lee, Mr. Xin Zhang, Mr. Yuming Bai, Mr. Haifei Deng, Prof. Wei Chen and Prof. Xiaochuan Jia. It was a pleasure to work with such a talented, hard-working and creative group.

My heartfelt appreciation goes toward my parents, who have always encouraged me to pursue higher education.

With much love, I would like to thank my wife, Xiling Song, who has always been there with her love and encouragement.

This work was supported by the VRM consortium (Intel, Texas Instruments, ST Microelectronics, National Semiconductor, Delta Electronics, International Rectifier, IBM, Intersil, TDK, Hitachi, Hipro, Power-One) and the ERC program of the National Science Foundation under award number EEC-9731677.
TABLE OF CONTENTS

Chapter 1  Introduction……………………………………………………………….  1

1.1 Research Background..............................................................................  1

1.2 Multiphase Technology............................................................................. 7

1.3 State-of-the-Art VRM Design................................................................. 11
  1.3.1 12-V Input VRM.................................................................................. 11
  1.3.2 48-V Input VRM.................................................................................. 15

1.4 Technical Challenges for VRM Design..................................................... 19

1.5 Dissertation Outline.................................................................................. 20

Chapter 2  Topology Improvement for Multiphase VRMs.........................  26

2.1 Multiphase Buck Converter...................................................................... 27
  2.1.1 Small Duty Cycle Limitation............................................................... 28
  2.1.2 Influence of Duty Cycle on Ripple Cancellation............................... 29
  2.1.3 Influence of Duty Cycle on Efficiency............................................... 32

2.2 Multiphase Tapped-Inductor Buck Converter......................................... 40
  2.2.1 Design Consideration for Turns Ratio............................................... 40
  2.2.2 Limitation of Voltage Spike Problem............................................... 46

2.3 Multiphase Coupled-Buck Converter..................................................... 50
  2.3.1 Concept of Multiphase Coupled-Buck Converter.............................. 50
  2.3.2 Principle of Operation...................................................................... 53
  2.3.3 Design Consideration for Turns Ratio............................................... 58
<table>
<thead>
<tr>
<th>2.3.4</th>
<th>Efficiency Evaluation and Experimental Results</th>
<th>61</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.4</td>
<td>Concept Extension for Isolation Applications</td>
<td>70</td>
</tr>
<tr>
<td>2.5</td>
<td>Summary</td>
<td>76</td>
</tr>
<tr>
<td><strong>Chapter 3</strong> Magnetic Integration for Multiphase VRMs</td>
<td>78</td>
<td></td>
</tr>
<tr>
<td>3.1</td>
<td>Introduction</td>
<td>79</td>
</tr>
<tr>
<td>3.2</td>
<td>Integrated Magnetics for Multiphase VRMs</td>
<td>81</td>
</tr>
<tr>
<td>3.2.1</td>
<td>Integrated Magnetics for 12V VRM</td>
<td>81</td>
</tr>
<tr>
<td>3.2.2</td>
<td>Integrated Magnetics for 48V VRM</td>
<td>83</td>
</tr>
<tr>
<td>3.2.3</td>
<td>Limitation of Integrated Magnetics</td>
<td>86</td>
</tr>
<tr>
<td>3.3</td>
<td>An Improved Integrated Magnetics</td>
<td>88</td>
</tr>
<tr>
<td>3.3.1</td>
<td>Derivation and Analysis of Improved Integrated Magnetics</td>
<td>89</td>
</tr>
<tr>
<td>3.3.2</td>
<td>Inductor Coupling and Influence on Converter Performance</td>
<td>101</td>
</tr>
<tr>
<td>3.3.3</td>
<td>Demonstration of Proposed Integrated Magnetics for 12-V VRM</td>
<td>110</td>
</tr>
<tr>
<td>3.3.4</td>
<td>Demonstration of Proposed Integrated Magnetics for 12-V VRM</td>
<td>119</td>
</tr>
<tr>
<td>3.4</td>
<td>Integration of Input Filter into Proposed IM Structure</td>
<td>124</td>
</tr>
<tr>
<td>3.4.1</td>
<td>Concept of Built-In filter</td>
<td>125</td>
</tr>
<tr>
<td>3.4.2</td>
<td>Design of Built-in Filters</td>
<td>130</td>
</tr>
<tr>
<td>3.4.3</td>
<td>12-V VRM with Built-in Filter and Experimental Results</td>
<td>133</td>
</tr>
<tr>
<td>3.4.4</td>
<td>Improvement of 48-V VRM with Built-in Filter</td>
<td>136</td>
</tr>
<tr>
<td>3.4.4.1</td>
<td>Improved Push-Pull Forward Converter with Built-in Filter</td>
<td>136</td>
</tr>
<tr>
<td>3.4.4.2</td>
<td>Winding Design for Built-in Filter</td>
<td>139</td>
</tr>
<tr>
<td>3.4.4.3</td>
<td>Experimental Results</td>
<td>146</td>
</tr>
</tbody>
</table>
LIST OF FIGURES

Figure 1.1. Total number of transistors in the microprocessors has increased exponentially (Source: Intel Technology Symposium 2000, by Jerry Budelman)……2

Figure 1.2. Microprocessors roadmap for supply voltages (Source: Intel Technology Symposium 2000, by Ed Stanford)…………………………………………………… 3

Figure 1.3. Microprocessors roadmap for current demands and transition slew rates (Source: Intel Technology Symposium 2000, by Ed Stanford)…………………… 3

Figure 1.4. Power delivery architecture for low-end computer systems………………. 4

Figure 1.5. Plug-in VRM and embedded VRM [E2]…………………………………… 4

Figure 1.6. Power delivery architecture for high-end computer systems………………5

Figure 1.7. Power POD in Intel high-end servers [E3]………………………………… 6

Figure 1.8. Single-phase VRM………………………………………………………… 7

Figure 1.9. Multiphase VRM……………………………………….…………………… 9

Figure 1.10. Current ripple cancellation in multiphase VRMs………………………… 10

Figure 1.11. Multiphase buck converter (two-phases as an example)……………… 12

Figure 1.12. Push-pull forward converter with current-doubler rectifier………………17

Figure 1.13. Integrated magnetics for the current-doubler rectifier………………….. 18

Figure 2.1. Multiphase buck converter (two-phases as an example)………………. 27

Figure 2.2. Small duty cycle of multiphase buck converter…………………………… 29

Figure 2.3. Normalized output current ripple vs. duty cycle, \( \Delta I_{LN} = \frac{V_o}{LCH \cdot F_s} \)……………… 32
Figure 2.4. Loss contributions in four-phase buck VRM with $V_{IN}=5$ V and 12 V........ 38
Figure 2.5. Measured efficiency of four-phase buck VRM under $V_{IN}=5$ V and 12 V...39
Figure 2.6. Multiphase tapped-inductor buck converter (two-phase as an example).... 41
Figure 2.7. DC voltage gain of tapped-inductor buck converter as a function of the duty cycle D and the turns ratio $n$................................................................. 42
Figure 2.8. Equivalent circuits of tapped-inductor buck converter during transients: (a) step up, and (b) step down................................................................. 43
Figure 2.9. Inductor slew rates during step-up and step-down transients for tapped-inductor buck converter as a function of the turns ratio $n$......................... 45
Figure 2.10. Measured efficiency of four-phase tapped-inductor buck VRM......... 47
Figure 2.11. Measured waveform shows a huge voltage spike across the top switch in the four-phase tapped-inductor buck VRM............................................. 48
Figure 2.12. Voltage spike across the top switch is caused by the leakage inductance of the tapped inductor and the output capacitance of the top switch............. 49
Figure 2.13. Multiphase tapped-inductor buck converter with an additional active clamping circuit for each channel......................................................... 51
Figure 2.14. Active clamping circuits are formed between neighbor channels; however, the capacitor voltage is variable......................................................... 52
Figure 2.15. Proposed multiphase coupled buck converter.............................. 53
Figure 2.16. Simplified multiphase coupled-buck converter for steady-state analysis.... 54
Figure 2.17. Key operation waveforms of the multiphase coupled-buck converter...... 55
Figure 2.18. Equivalent circuits of the multiphase coupled-buck converter: (a) Stage I, (b) Stage II, (c) Stage III and (d) Stage IV…………………………………………………. 57

Figure 2.19. DC voltage gain of multiphase coupled buck converter as a function of the duty cycle D and the turns ratio n…………………………………………………. 58

Figure 2.20. Inductor slew rates (during step-up and step-down transients for the multiphase coupled-buck converter) as a function of the turns ratio n………………… 60

Figure 2.21. Loss contributions at full load for four-phase coupled-buck VRM and four-phase buck VRM……………………………………………………………………….. 65

Figure 2.22. Hardware pictures: (a) the four-phase coupled-buck VRM, and (b) the four-phase buck VRM……………………………………………………………………….. 66

Figure 2.23. The same transient response is found in (a) the four-phase coupled buck VRM and (b) the four-phase buck VRM……………………………………………………………………….. 68

Figure 2.24. The four-phase coupled-buck VRM has a higher efficiency than the four-phase buck VRM……………………………………………………………………….. 69

Figure 2.25. (a) The two-phase buck converter, and (b) its isolated counterpart – the push-pull converter with the current-doubler rectifier…………………………………… 70

Figure 2.26. Multiphase coupled-buck converter with labeled winding terminals…….. 71

Figure 2.27. Interchangeable configuration using discrete transformers and inductors instead of coupled inductors………………………………………………………….. 72

Figure 2.28. (a) Two-phase coupled-buck converter, and (b) its isolated counterpart – the push-pull forward converter with the current-doubler rectifier…………………… 73

Figure 2.29. Push-pull forward converter with the current-doubler rectifier…………… 74
Figure 2.30. Measured power-stage efficiency for both the push-pull and the push-pull forward VRMs................................................................. 75

Figure 3.1. Multiphase coupled-buck converter for 12V VRM.......................... 80

Figure 3.2. Push-pull forward converter with current-doubler rectifier............... 81

Figure 3.3. (a) The magnetics in the multiphase coupled-buck converter; (b) discrete magnetic implementation; (c) core simplification; and (d) winding simplification (W.Chen’s integrated magnetics [C26])................................................... 83

Figure 3.4. (a) Current-doubler rectifier; (b) discrete magnetic implementation; (c) O. Seiersen’s integrated magnetics [C15, C16]; and (d) W. Chen’s integrated magnetics [C26]........................................................................................................... 85

Figure 3.5. Core structure of the existing integrated magnetics......................... 87

Figure 3.6. Large leakage flux in the existing integrated magnetics................... 87

Figure 3.7. Test waveforms of the existing integrated magnetics...................... 88

Figure 3.8. Derivation of the improved integrated magnetic structure: (a) Original structure, (b) winding splitting, (c) polarity change, and (d) gap shifting................................................................. 90

Figure 3.9. Magnetic reluctance circuit of proposed integrated magnetics.......... 92

Figure 3.10. Equivalent electrical circuits of proposed integrated magnetic circuit: (a) in the form of coupled inductors, and (b) in the form of the transformer and the inductors................................................................. 93

Figure 3.11. AC fluxes in the core of proposed integrated magnetics............... 95
Figure 3.12. DC flux bias in the core structures of: (a) the existing integrated magnetics, and (b) the proposed integrated magnetics……………………………………………… 99

Figure 3.13. Flux waveforms: (a) in the existing integrated magnetics, and (b) in the proposed integrated magnetics……………………………………………………. 100

Figure 3.14. Voltage waveforms across two coupled inductors………………………… 103

Figure 3.15. Voltage and current waveforms during the load transient: (a) the coupling case, and (b) the non-coupling case…………………………………………………….. 106

Figure 3.16. Steady-state voltage and current waveforms for the coupling case (solid lines) and the non-coupling case (dashed lines)………………………………………… 108

Figure 3.17. Schematic of four-phase coupled-buck converter………………………… 110

Figure 3.18. Implementation of integrated magnetics in the four-phase coupled-buck VRM: (a) proposed structure, and (b) existing structure……………………………… 112

Figure 3.19. AC flux distributions: (a) in the existing structure, and (b) in the proposed structure…………………………………………………………………………….. 114

Figure 3.20. Core loss reduction in the center leg of proposed structure……………….. 115

Figure 3.21. Winding current distributions: (a) in the existing structure, and (b) in the proposed structure……………………………………………………………………….. 116

Figure 3.22. Winding loss reduction in the proposed integrated magnetic structure…. 117

Figure 3.23. Current waveforms: (a) in primary switches, and (b) in secondary switches……………………………………………………………………………… 118

Figure 3.24. Measured power-stage efficiency of four-phase coupled-buck VRM with existing and proposed integrated magnetic structures…………………………….. 119
Figure 3.25. Integrated magnetic designs: (a) existing structure, and (b) proposed structure........................................................................................................ 120

Figure 3.26. AC flux distributions: (a) in the existing structure, and (b) in the proposed structure........................................................................................................ 121

Figure 3.27. Winding current distributions: (a) in the existing structure, and (b) in the proposed structure........................................................................................................ 122

Figure 3.28. Experimental waveforms at full load: (a) with the existing structure, and (b) with the proposed structure........................................................................................................ 123

Figure 3.29. Measured power-stage efficiency for 48V VRM........................................ 124

Figure 3.30. Pulsing input and output currents of multiphase coupled-buck converter require additional L-C filters........................................................................................................ 126

Figure 3.31. Improved multiphase coupled-buck converter features built-in filters..... 126

Figure 3.32. Key operation waveforms of the improved multiphase coupled-buck converter........................................................................................................ 127

Figure 3.33. Integration of L-C filters in multiphase coupled buck converter: (a) with additional L-C filters, (b) capacitor shifting, and (c) inductor shifting................. 128

Figure 3.34. Derivation of improved coupled buck converter: (a) multiphase tapped-inductor buck converter with external L-C filters, and (b) multiphase coupled buck converter with built-in filters................................................................. 129

Figure 3.35. Two implementations for the input filter in the multiphase coupled-buck converter: (a) with external filter, and (b) with fully integrated filter................. 130

Figure 3.36. Simplified circuit model for the VRM input filter design......................... 132
Figure 3.37. Schematic of the four-phase improved coupled-buck converter .......... 134
Figure 3.38. Hardware of four-phase improved coupled-buck VRM ..................... 135
Figure 3.39. Measured waveforms of the improved coupled-buck VRM ............... 135
Figure 3.40. Measured efficiency of the four-phase improved coupled-buck VRM .... 136
Figure 3.41. Push-pull forward converter with proposed integrated magnetic structure:
   (a) implementation, and (b) electrical equivalent circuit, for which the split
   transformer windings are shown ......................................................... 137
Figure 3.42. Push-pull forward converter with built-in filter: (a) implementation; and (b)
   equivalent circuit .............................................................................. 138
Figure 3.43. Winding arrangements: (a) seven layers (I), (b) seven layers (II), (c) eight
   layers (I), (d) eight layers (II), (e) eight layers (III), and (f) nine layers .......... 140
Figure 3.44. Simulation results: (a) the primary-secondary leakage inductance (Lsp); and
   (b) winding AC resistances (reflected to the secondary side) ...................... 141
Figure 3.45. Controlling the leakage inductance by using different methods to interleave
   the windings ....................................................................................... 142
Figure 3.46. Simulation results for Figure 3.45’s windings: (a) the primary-primary
   leakage inductance (Lpp); and (b) winding AC resistances (reflected to the primary
   side) ..................................................................................................... 143
Figure 3.47. Controlling the leakage inductance by partially overlapping the
   windings .............................................................................................. 144
Figure 3.48. Simulation results for shifted windings: (a) the primary-primary leakage inductance (L_{pp}); and (b) winding AC resistances (reflected to the primary side)……………………………………………………………………………………………………… 145

Figure 3.49. 48V VRM prototype using the single-magnetic push-pull forward converter………………………………………………………………………………………………………………………………………………… 147

Figure 3.50. Experimental waveforms at full load for the single-magnetic push-pull forward converter: V_{ds} (top), I_{in} (middle), and V_{gs} (bottom)…………………………………… 147

Figure 3.51. Measured power-stage efficiency for conventional push-pull, push-pull forward and push-pull forward converters………………………………………………………… 148

Figure 4.1. Topology of the multiphase VRM………………………………………………………… 153

Figure 4.2. Optimization method for a given channel number (N_C): (a) critical inductance, (b) minimum efficiency requirement, and (c) objective function…….. 159

Figure 4.3. Method for finding the optimal channel number…………………………………… 163

Figure 4.4. Selecting the critical inductance value as the output inductance……… 166

Figure 4.5. Determining the maximum switching frequency for a selected channel number in accordance with the efficiency constraint…………………………………….. 168

Figure 4.6. Transient voltage deviation for selected channel numbers………………… 171

Figure 4.7. Determining the minimum required numbers of output capacitors for selected channel numbers in accordance with the transient constraint………………... 172

Figure 4.8. Cost breakdown for typical multiphase VRMs……………………………………….. 176

Figure 4.9. Influence of the channel number on the cost of multiphase VRMs……….. 180
LIST OF TABLES

Table 1.1. State-of-the-Art 12V VRM Designs………………………………………… 12

Table 3.1. Input filter designs: (Case I has no built-in filter, only an external filter; Case II has both a built-in and an external filter; and Case III has a fully integrated filter)…………………………………………………………………………. 133

Table 4.1. Industrial designs choose quite different numbers of channels for the same VRM 9.0 specification……………………………………………………………………………….. 154

Table 4.2. Maximum allowable switching frequency for selected channel number… 169

Table 4.3. Minimum required number of capacitors and corresponding switching frequency ranges for selected channel numbers…………………………………… 173

Table 4.4. Comparison of optimization results with industry practice……………… 174

Table 4.5. Optimization results using the same active area of semiconductors for MOSFETs and their comparison with industry practice………………………….. 175

Table 4.6. Optimal designs for selected channel numbers…………………………… 178