Driver Based Soft Switch for Pulse-Width-Modulated Power Converters

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Abstract

The work in this dissertation presents the first attempt in the literature to propose the concept of “soft switch”. The goal of “soft switch” is to develop a standard PWM switch cell with built-in adaptive soft switching capabilities. Just like a regular switch, only one PWM signal is needed to drive the soft switch under soft switching condition.

The core technique in soft switch development is a built-in adaptive soft switching circuit with minimized circulation energy. The necessity of minimizing circulation energy is first analyzed. The design and implementation of a universal controller for implementation of variable timing control to minimize circulation energy is presented. The controller has been tested successfully with three different soft switching inverters for electric vehicles application in the Partnership for a New Generation Vehicles (PNGV) project. To simplify the control, several methods to achieve soft switching with fixed timing control are proposed by analyzing a family of zero-voltage switching converters.

The driver based soft switch concept was originated from development of a base driver circuit for current driven bipolar junction transistor (BJT). A new insulated-gate-bipolar-transistor (IGBT) and power metal-oxide-semiconductor field-effect-transistor (MOSFET) gated transistor (IMGT) base drive structure was initially proposed for a high power SiC BJT. The proposed base drive method drives SiC BJTs in a way similar to a Darlington transistor. With some modification, a new base driver structure can adaptively achieve zero voltage turn-on for BJT at all load current range with one single gate. The proposed gate driver based soft switching method is verified by experimental test with both Si and SiC BJT. The idea is then broadened for “soft switch” implementation. The whole soft switched BJT (SSBJT)
structure behaves like a voltage-driven soft switch. The new structure has potentially inherent soft transition property with reduced stress and switching loss.

The basic concept of the current driven soft switch is then extended to a voltage-driven device such as IGBT and MOSFET. The key feature and requirement of the soft switch is outlined. A new coupled inductor based soft switching cell is proposed. The proposed zero-voltage-transition (ZVT) cell serves as a good candidate for the development of soft switch. The “Equivalent Inductor” and state plane based analysis method are used to simply the analysis of coupled inductor based zero-voltage switching scheme. With the proposed analysis method, the operational property of the ZVT cell can be identified without solving complicated differential equations. Detailed analysis and design is proposed for a 3kW boost converter example. With the proposed soft switch design, the boost converter can achieve up to 98.9% efficiency over a wide operation range with a single gate drive. A high power inverter with coupled inductor scheme is also designed with simple control compared to the earlier implementation. A family of soft-switching converters using the proposed “soft switch” cell can be developed by replacing the conventional PWM switch with the proposed soft switch.
To my wife: Lily
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Chapter 1 Introduction

1.1 Background

Power electronics is to use switching circuits to convert and control power flow. Power electronics technology is widely used in the areas of industrial motor drives control, switching mode power supplies, computers and communications, power systems, automotives, etc. More than 60% of electric power in the United State today is processed through some forms of power electronics [A12]. With the shortage of energy and ever increasing oil price, the need for higher power efficiency and greater performance is imminent. The growing market of computer and communication equipment has created an increasing demand for higher efficiency and higher power density power converters. The market share of power electronics industry is increasing at a dramatic rate. The market demands eventually drive the needs for more innovative technology in power electronics.

Power semiconductor switches are the key part of power electronics circuits. Every major breakthrough in new materials or a new device will result in a revolutionary improvement in the performance of power converters [A16]. The area of new materials, new device and the associated control, system integration and packaging technique have been the research focus in power electronics field.

The simplest way to control power semiconductor switches is by Pulse-Width-Modulation (PWM). The PWM technique is to control power flow by interrupting current or voltage by means of switch action with control of duty cycles. Conventionally, the voltage across or current through the semiconductor switch is abruptly interrupted, such a technique is so-called hard-switched PWM. Because of its simplicity, relatively small current stress and ease in control, hard-switched PWM techniques have been predominantly used in modern power electronics converters for decades. Thanks to the rapid developments of new power device technologies, the switching speed of power devices has improved significantly. From the SCR, BJT, GTO to IGBT and MOSFET, the power device switching transition time has decreased dramatically from sub-milliseconds to sub-microseconds. This enables PWM power converters to operate at a much higher switching frequency thus reducing the passive component size and eventually reduce the overall system cost. However, in association with the increased frequency, the converter switching loss also increases proportionally. The high dv/dt and di/dt caused by the increased speed will result in increased stress on device and system EMI noise.
These limitations restricted the conventional hard-switched PWM converters from operating at a higher frequency. In past several decades, lots of research works have been done to seek a better solution to shape the switch transition in order to overcome the inherent problem of hard switched PWM converters\[A1]-[A9].

1.2 Review of state of art soft commutation techniques

Numerous methods discussing control the transition of power devices have been proposed. They can be divided into the three major groups: Soft switching techniques [C1]-[C33][D1]-[D30], passive snubbers techniques[E1]-[E19] and active gate driver based $\frac{di}{dt}$ and $\frac{dv}{dt}$ control techniques[F1]-[F11]. Fig. 1.1 summarizes various soft commutation methods:

![Fig. 1.1 Summary of soft commutation methods](image)

1.2.1 Soft commutation with snubber circuits

Passive snubber methods reduce switching losses by limiting the active switches $\frac{di}{dt}$ and $\frac{dv}{dt}$ during switching transition with the assistant of passive components. Typically an inductor is placed on the turn-on path of the active switch to achieve zero current turn-on, and a capacitor is placed in the turn-off path of the active switch to achieve zero voltage turn off. In this case the zero current turn on and zero voltage turn off could be achieved for the main switch. However, this benefit is not free of penalty. Generally, a turn-on snubber will introduce extra voltage stresses during turn-off, and a turn-
off snubber will introduce extra current stress during turn-on. Extra snubber circuits have to ensure the proper removal of the stored energy during the switch transition. Depending on whether the energy stored in the inductor or capacitor is recycled or dissipated by means of resistor heat, the passive snubber method could be divided into two main categories: dissipative passive snubber circuits and no dissipative snubber circuits.

For dissipative snubber method, the energy stored in the snubber network is converted into heat and dissipated completely. Fig. 1.2(a) shows a typical RCD snubber example attempting to reduce switching stress spikes in the switching circuit due to diode reverse recovery. The inductor in series with switch is to limit the turn-on current slope and to reduce the diode reverse recovery problem. The energy stored in the inductor is transferred to capacitor $C_s$ when the device is turned off. Capacitor energy stored in each switching cycle needs to be dissipated through resistor $R_s$ and switch $S$. All the energy stored in the inductor and capacitor is eventually dissipated in resistors in the forms of heat. Because the excessive loss associated with this type of method, it is mostly used for low switching frequency. Fig. 1.2(b) shows the phase leg arrangement of a typical RCD snubber[E4].

(a) three-terminal PWM switch with RCD snubber  (b) inverter phase leg with RCD snubber

Fig. 1.2 Dissipative RCD passive snubber
The energy stored in the linear snubber inductor in series with the main power circuit is not recovered. The energy wasted could be very significant, thus offsetting the benefit of the turn-on snubber. As shown in Fig. 1.3, a saturable inductor, which stores substantially less energy than a linear inductor, could be used as turn-on snubber inductor [E10]. The inductor is designed to saturate after the switch voltage has dropped to its on-state level. This configuration has the advantage that only the energy associated with the inductor magnetizing inductance is lost. The diode reverse recovery current is controlled and turn-on loss is reduced at the expense of resetting losses of the saturable inductor.

Non-dissipative snubber should actually be called low-loss snubber or snubbers without fundamental dissipative components such as resistors. Energy is dissipated in the forms of conduction and switching losses. The lossless snubber network could be considered a path to dissipative snubber that the non-dissipative methods are concentrated on the method of regenerating energy from the passive reactive components. This type of snubber networks have lower loss, reliable, less expensive and somehow can get better performance than some of the active snubber method. Since no active device is involved, the overall cost could be lower than active snubber method. Papers [E16][E17] give a general topological analysis of these type of recovery circuits and synthesis procedure for creation of a family of passive lossless soft switching converters. There are two major groups of the proposed cells based on whether extra voltage stress is imposed on the main switches or not. The minimum voltage stress cells (MVS) minimize the voltage stress across the main switch. However, their soft switching range can be very limited. The non-MVS cells substantially extended the soft-switching range at the cost of extra stress to the main switch. Unfortunately, most approaches take too many transmission
loops to get the energy regenerated. There are too many diodes involved, and the circuit interconnection is very complicated that parasitic components may prevail and cause additional losses. The selection of passive component is lack of a general design rule for a wide load range, and it is very difficult for standard massive production. The overall performance could be very limited.

Fig. 1.4 A Non-MVS snubber cell

Fig. 1.5 A MVS snubber cell

Other efforts are made to simplify the component counts on the snubber networks. The coupled inductor based current steering concept is interesting in simplification the snubber design. Fig. 1.6 shows the cell diagram of a turn-on snubber for Power Factor Corrected (PFC) boost converter. The coupled inductor shifts the original output diode current to the alternative branch during the switch off period. The leakage inductor of the coupled inductor serves as the turn-on snubber for the auxiliary branch. This will result in a slowed di/dt and decrease diode reverse recovery related turn-on loss.
Though the snubber cell in Fig. 1.6 looks very simple, it does have some problems due to the undesirable resonance that occurs between the leakage inductor and the parasitic capacitor of auxiliary diode D when switch S turns on. In practice, a small RCD snubber circuit for diode D is generally needed to reduce the voltage stress. Besides, the switch turn-off is not improved. Another limitation of this circuit is the duty cycle limit for the cell. The switch needs sufficient time to wait for the current in leakage inductor to reset in order to avoid saturation of the coupled inductor. An improved version with turn-off snubber for this cell is introduced later[E15], but the solution creates more circuit components with an extra diode in the main current flow path, thus introducing higher conduction voltage drop. Fig. 1.7 shows the snubber cell of the improved version for a PFC boost converter.

In summary, the major advantage of passive snubber commutation method is simple in control. Only one gate signal is needed to drive the power switch. Research works are still undergoing to further simplify the switch network circuits[E9][E14]. The soft commutation with passive snubber methods is reliable because of extra passive component in the main power path to limit the di/dt. However, this will require passive components in the snubber network to withstand full power. For some converters with low switch frequency but high reliability, such as GTO based high power inverters, this method is dominantly used. However, the overall system efficiency could be reduced,
and the power stage is more complicated. The output diode reverse recovery problem is limited by series inductor but is not completely eliminated as in resonant converters. Extra voltage stress and ringing could be expected across the output diode. With further development in semiconductor technology, the cost of active switch become lower and lower, the extra cost associated with bulky passive component will make these methods less attractive unless for some particular applications.

### 1.2.2 Gate driver controlled commutation

Unlike the passive snubber network approach, the gate side control method does not require extra elements in the main power circuit\[F1]-\[F11]. The basic concept of gate controlled di/dt and dv/dt approach is to control the speed of gate charging so as to control the switch transition. This method sounds more attractive since a more compact design could be achieved without adding extra power components in the main power circuits. The basic goal for gate driver control is to limit di/dt during switch turn-on and to limit dv/dt during switch turn-off. The basic equation to describe the switch transition could be given as follows \[A11\]:

\[
\frac{dV_{ce}}{dt} = -\frac{I_g}{C_{gc}} - \frac{V_{goff} - (V_{th} + \frac{I_c}{g_m})}{C_{gc} * R_g}
\]

\[
\frac{dI_c}{dt} = -\frac{V_{gon} - (V_{th} + \frac{I_c}{2 * g_m})}{C_{gc} * R_{gon} * \frac{1}{g_m} + L_s}
\]

where:
- \(C_{ge}\): device gate-emitter capacitance (F)
- \(C_{gc}\): device gate-collector capacitance (F)
- \(g_m\): device transconductance (A/V)
- \(L_s\): device terminal parasitic inductance (H)
- \(V_{th}\): gate threshold voltage (V)
- \(V_{gon}\): Turn on voltage level
- \(V_{goff}\): Turn-off voltage level

From the above equation, we can see the easiest way to control the switching transition is by adjusting the gate resistors, either dynamically or statically. Fig. 1.8 shows a conventional way of gate
control by separating the turn-on and turn-off charging paths with higher turn-on resistor Ron, a lower turn-off resistor Roff. The penalty with slow turn-on is the significantly increased switching loss. In addition, this kind of design will only be able to optimizing the driver circuit at a fixed switching condition. When load current or blocking voltage changes, the gate drive resistor is not changed accordingly.

Fig. 1.8 Turn-on and turn-off control with separate gate resistors

Paper [F4] introduced an active gate control method to limit the gradients. Instead of changing the gate resistors, the gate charging current is limited. For the dv/dt control the collector voltage is sensed and differentiated. The gate current is reduced only when voltage gradient is higher than the desired value. The same basic principle can be used for turn-on di/dt control as well. The derivative of the current is obtained by sensing the voltage across the stray inductance.

Fig. 1.9 Principle of turn-off dv/dt limit control
Instead of purely slowing down the gate resistor, this method actively controls the gate current only when control of $dv/dt$ or $di/dt$ is needed. Thus the extra switching loss could be reduced compared to pure resistive method. The overall switching speed could be increased. Another active control approach\cite{F11} is using current injection and sinking source to control the voltage and current gradient. As shown in Fig. 1.11, Instead of changing resistors dynamically, a controlled current mirror is injected to the switch gate input. By adjusting the current mirror gain value $A$, the effective gate-to-drain capacitance is changed, thus the turn-off $dv/dt$ control could be progressively controlled by gain $A$. Same technique can be applied to electronically adjust the output current $di/dt$ over a wide range with the feedback of $di/dt$ signal by sensing the voltage drop of the switch emitter terminal inductance. Fig. 1.12 gives a conceptual diagram of this turn-on $di/dt$ control. This method controls the gradient rather than limiting the gradient during the switch transactions. The basic concept is still originated from equation (1-1).
With the consideration of the device physics, a more effective active gate driver control would need to control the gate charging current according to the different stages during switch transition [F6][F7][A9]. These methods could be regarded as multi-stage charging current control. The basic principle is illustrated in Fig. 1.13. At the first stage, large current is required to charge up the gate voltage until the collector voltage starts rising. Then gate charging is reduced to limit the di/dt so as to alleviate the diode reverse recovery problem. After device reaches peak current, the gate charging current is again charged rapidly so as to reduce the tail voltage in order to reduce turn-on switching loss. The overall objective is to control the over-voltage at turn-off and over-current at turn-on and maintain minimal switching delay so as to reduce switching power loss. Active turn-off is implemented at the similar control technique. The actual implementation of the multistage could be quite complicated. The fine tune of circuit and control parameters would need lots of field work even though the timing and control logic could be eventually integrated.
The gate controlled di/dt and dv/dt approach looks very attractive since a very compact design could be achieved without adding extra components in the power circuits. However, all the proposed gate based concepts in the literature are based on hard switching design. Thus the limit of di/dt and dv/dt will be largely at the cost of increased switching loss. The safe operating area of the power device is still limited due to the inevitable concurrence of high current and high voltage. Furthermore, most active gate drive circuits will need sensing feedback and complicated control circuits. The active gate driver circuits have to be fine tuned according to each application. This technique is mostly adopted in multilevel converters where voltage balancing is necessary for serial connected devices. In order to fully utilize the device capability and improve overall system efficiency, soft switching techniques are still a better choice. It would be very promising if a new approach can combine both the benefit of soft switching and the compact design of gate drive based circuits.

1.2.3 Soft Switching techniques

Soft switching resonant circuits, however, can achieve both the benefit of switch transition control and switching loss reduction. This gives the potential of achieving higher frequency and reduces harmonic pollution of the converter. The soft switching techniques have evolved from the early traditional series and parallel resonant techniques (RC), quasi-resonant converters (QRC), multi-resonant converters (MRC) to soft switching PWM converters, which includes zero-voltage transition (ZVT) and zero-current-transition (ZCT). The resonant converters employ resonant circuits to achieve soft switching of devices. The converter can be configured to operate under either zero current or zero
voltage switching condition. The conventional resonant converters can be divided into two major categories: series resonant converter and parallel resonant converter. Fig. 1.14 and Fig. 1.15 give typical series and parallel resonant converter circuits.

For series resonant converters, the load is in series with the resonant circuit elements. The resonant current is filtered and used to provide output power. In the parallel resonant converter, the load is in parallel with the resonant circuit, the resonant voltage is rectified and filtered for output power.

Since the energy is transferred from the source to load in the form of resonance, the conventional resonant converter is designed and controlled in frequency domain. The control circuits changes the frequency to move either toward or away from the natural resonant frequency, thus controlling the amount of energy transferred into the resonant circuit so as to control the output power. Clamped-mode resonant converter is reported with the advantage of operation at a fixed frequency. By introducing a phase lag for the two diagonally opposite switches, the voltage $V_{in}$ applied to the tank is quasi-square wave instead of square wave. The converter can thus be regulated by changing the duty of the square wave voltage applied to resonant tank. The main drawback for resonant converter is because the power is delivered by the resonant tank. First, the control would be highly nonlinear and complicated. Second, excess circulation energy will cause increased conduction loss compare to square type PWM.
converters. The load change could also cause the resonant converter lose zero-voltage condition. The technology is less favorable compared to the soft switching methods introduced in the later section.

The introduction of three-terminal PWM switch concept gives power electronics researchers a powerful tool in analyzing a new generation of power converters. The PWM switch model gives the foundations of power converter modeling and control. By analyzing the average behavior of a basic PWM switch cell in DC and small signal manner, the nonlinear switch can be linearized and the converter can be analyzed by replacing the PWM switch with a linear equivalent circuit model. This method significantly simplifies the analysis of the power converter and highlights the intrinsic connections between various circuit topologies. Similar to the PWM switch concept, the introduction of resonant PWM switch is one of the most important concepts in soft switching technologies [C4][C1][C2]. By replacing the PWM hard switching switch with a resonant switch cell in the power converter, a family of quasi-resonant converters could be generated. Fig. 1.16 shows the basic hard switching PWM cell, ZVS QRS switch cell, ZCS QRS switch cell and ZVS MRS cell.

![PWM resonant switch cell](image)

For ZCS quasi-resonant technique, the objective is to use auxiliary LC resonant tank to shape the switching device’s current waveform at on-time in order to create a zero-current condition for the device to turn-off. The ZCS technique does not solve the problem of high switching loss associated
with capacitive turn-on of the switch. On the other hand, the ZVS-QRS technique use auxiliary LC resonant tank to shape the switch voltage waveform to create a ZVS condition before turning on of the switch. The ZVS multi-resonant converter (ZVS-MRC) absorbs both the parasitic output capacitance of the active switch and the parasitic junction capacitance of the rectifying diode, thus provide favorable switching condition for both devices. The only change from a ZVS-QRC to ZVS-MRC is one extra capacitor across rectifying diode, as shown in Fig. 1.16 (d).

For all the resonant converters, the LC tank is always present in the main power path, not only to achieve the soft commutation of the switch but also to store and transfer energy similar to the resonant tank of conventional resonant converters. The regulation of output power will depends on the changing of switching frequency. A wide input voltage and load range will require the resonant converter operate at a very wide frequency range, which makes it difficult to optimally design the resonant converter elements, especially the magnetic parts.

To overcome this problem, a ZVS-PWM switch cell was proposed by adding an extra switch $S_x$ across the ZVS-QRS switch resonant inductor. By turning on $S_x$ before turn-off of $S$, an extra freewheeling period is inserted into the operation stage of ZVS-QRS converter. The output power could thus be regulated by tuning the freewheeling interval with a constant switching frequency. Fig. 1.17 shows a ZVS-PWM buck converter with a ZVS-PWM resonant switch cell. To achieve a constant frequency operation of ZVS-MRC, the passive diode in the switch could be replaced by an active switch $S_x$. The modulation of turn-on time of the added switch allows the control of output power [C9].

However, the achievement of constant frequency operation of resonant converters is at the cost of increased circulation energy. Furthermore, adding extra active switches will need extra gate driver and will increase cost and control complexity. A soft switching circuit that retains control simplicity of hard switching PWM converter without a significant increase in circulation energy is more desired.
Soft-switching PWM techniques combined benefit of the simplicity of PWM control and soft transition of resonant converter. The purpose of soft-switching techniques is to shape the voltage and current waveform during the switching transitions so as to reduce switching losses and device stresses. The converters operate in resonant mode only during switching transition and then resume simple PWM operation during the rest of time. Soft transition is accomplished by the assistance of auxiliary circuits, which consist of resonant components and auxiliary switches that trigger the resonance during the switching transition. After the switch transition accomplished, the auxiliary switch will then disconnect the auxiliary resonant tank from the main power circuits in order to resume the normal PWM operation of the converter. Compared to resonant converter, the extra price to pay is the need of extra auxiliary switches.

According to the soft transition type, the soft-switching PWM technique can be divided into two major categories: zero-voltage transition (ZVT) technique and zero-current transition (ZCT) technique. For the ZVT technique, a resonant capacitor is placed in parallel with the main power switch. The purpose of auxiliary circuit, which is typically an auxiliary switch, a resonant inductor and a diode, is to create a current sinking mechanism to divert the load current from the freewheeling rectifier diode to the anti-parallel diode of the main switch. The voltage across the main switch is brought down to zero by resonance thus creating the zero voltage turn-on condition for the main switch. Fig. 1.18 shows the basic concept of a ZVT PWM cell and switch waveform.

![Fig. 1.18 Conceptual ZVT PWM cell](image)

For the ZCT technique, the resonant circuit is activated to create a current sink so that the current flowing through the outgoing device reduce to zero prior to the turn-off of the main device. Unlike ZVT scheme, the resonant capacitor is in series with the resonant tank. Fig. 1.19 shows the basic
concept of a ZCT PWM cell. In stead of shaping switch voltage pre-turn on for ZVT scheme, the current is shaped before switch turn-off in ZCT schemes.

![Fig. 1.19 Conceptual ZCT PWM cell](image)

In the ZVT PWM case, the resonant tank starts to gather energy, in the form of inductor current, before switch transition. After switch transition, the stored energy is immediately released. However, in the ZCT case, the energy needs to be pre-stored in the resonant capacitor in order to activate the resonant tank. The ZCT resonant capacitor needs to block bi-directional voltage and stand higher stress than that of ZVT. Besides, the ZCT scheme does not solve the diode reverse recovery problem. The load direction dependent is critical for bidirectional load current condition.[D25] [D26] [D27].

![Fig. 1.20 Hua’s ZCT PWM cell](image)
Fig. 1.21 Hua’s ZVT PWM cell

Fig. 1.22 ARCP ZVT PWM cell

Fig. 1.23 An Improved ZVT PWM cell with lossless snubber
1.3 Research motivation

From the last section review, the gate controlled di/dt and dv/dt approach looks very attractive since a very compact design could be achieved without adding extra components in the power circuits. However, all the previously proposed gate based concepts were developed for hard switching circuits. Thus the limit of di/dt and dv/dt will be largely at the cost of increased switching loss. The safe operating area of the power device is still limited due to the concurrence of high current and high voltage. Furthermore, most active gate drive circuits will need complicated control circuit and need sensing feedback. The gate driver circuits have to be further improved.

The soft switching PWM technique, combining the simplicity of PWM technique and soft transition of resonant converter, is the most promising soft commutation method. Many soft switching PWM converter circuits are generated in the past decades. The successful developments of soft switching PWM converters depend not only on particular topology, but also on the optimal control with minimal circulation energy. One major challenge in soft switching PWM technique is to achieve soft switching at all load conditions with minimal circulation energy. This means the resonant energy needs to be adjusted according to the load current level. Using variable timing control that adjusts the advanced trigger time of the auxiliary switch to adjust boost energy can reduce energy circulation in the resonant tank while maintaining the soft switching condition. Such a load current adaptive feature is even more important for high power inverter applications since the load current is always changing over the line cycle. However, to achieve this goal, the variable timing control requires the instantaneous load current feedback to implement the control signals of the auxiliary device. The increased control complexity and tuning efforts eventually increased overall cost significantly. This hampered the further implementation of soft switching PWM technique. Although promising theoretically, the soft switching PWM technique is not widely used in most industry products, especially in inverter application.

One major barrier to further advancements in technology and reduction of cost is the lack of standardization. Individual power converter is designed to offer partial solutions for specific application. This is especially true in soft switching PWM converters. The Power Electronics Building Block (PEBB) concept by the US Office of Naval Research (ONR) is to use intelligent and PEBB with standardized power, thermal and control interfaces to develop multitudes of affordable, reliable and
efficient power processing systems [A16]. The integrated power electronics module, so called IPEM, was widely introduced later by industry for commercial applications. Very few papers are reported in soft switched IPEMs because of its complexity in actual implementation. One major reason is the lack of a simple, robust and effective way to develop soft switching converter.

It would be more promising if a new approach can combine both the benefit of soft switching and the compact design of gate drive based soft commutation circuits. This dissertation presents the first attempt in the literature to systematically explore the possibility of achieving the above goal based on the developments driver based “soft switch” concept. The goal of soft switch is to develop a standard PWM switch with built-in load adaptive soft switching capabilities. Just like a regular switch, only one PWM signal is needed to drive the soft switch under soft switching condition.

A regular Switch \hspace{1cm} “soft Switch” ?

Fig. 1.24 The conceptual diagram of “soft switch”

The soft switch concept originated from the base driver design for current driven device such as SiC BJT. The basic concept of soft switch could be further extended to other current driven device such as GTO, and voltage driven device such as IGBT and MOSFET. A family of novel soft switching cells capable of soft switch development are studied and tested.

The foundation of soft switch design is built-in soft switching technique. The core of soft switch can is still a general PWM soft switching cell. The difference is that the soft switch approach is targeting on “built-in” soft switching capability. This leads to some special requirements for the PWM soft switching cell to be eligible for building a soft switch which will be outlined in Chapter 5.

Overall, with the support of advance packaging techniques, the ultimate goal for the development of soft switch is a high performance, simple, robust, and low cost soft switching solution.
1.4 Outline of the dissertation.

This dissertation is arranged as follows:

**Chapter 2** will explore the soft switching control solutions with minimized circulation energy. The necessity of a load adaptive approach to minimize unnecessary circulation energy loss is analyzed. The approach for variable control timing design for inductor coupled soft switching inverter is proposed. A “piggy-pack” type universal optimal variable timing controller is designed for evaluating three soft switching inverters for electric vehicle application in PNGV (Partnership for the New generation vehicles) program.

**Chapter 3** will explore the methodology of realizing load adaptive soft switching with fixed timing control method. First, a soft switching chopper with near zero voltage switching approach is presented. The key idea is to adjust the ratio of charging time and resonant time in order to get a near zero voltage switching with fixed time control. Second, a load adaptive fixed timing control soft switching chopper is presented utilizing diode reverse recover current. The fixed timing approve method is then generalized by analysis several different approaches of soft switching inverter cell.

**Chapter 4** will explore the soft switching design for SiC bipolar junction transistor. First, a hard switched IGBT and MOSFET based driver scheme is proposed to drive a SiC BJT. The implementation of the world first SiC BJT inverter demonstrated to drive a 7.5HP motor at rated power is presented. By comparing the typical ZVT scheme and the proposed base driver, the driver based soft switching SiC BJT structure is proposed. The new base driver can effectively drive SiC BJT and in the mean time realizing zero-voltage switching of the main device. The concept of the soft switch is presented for current driven devices.

**Chapter 5** will apply the soft switch concept originated from current driven device to voltage driven devices. The key feature and requirement of soft switch is outlined. A coupled inductor based soft switching cell is first proposed by reviewing the existing soft switching cells. An “Equivalent Inductance” conversion based analysis method is used to simply the analysis of coupled inductor based zero-voltage switching scheme. Detailed analysis and design is proposed for a 3kW boost converter. With the proposed soft switch based design, the boost converter can achieve up to 98.9% efficiency over a wide operation range with very simple control. A high power inverter with coupled inductor
scheme is designed will simple control compared to the earlier implementation in Chapter 2. A family of soft switching converter using the proposed “soft switch” cell can be developed.

Chapter 6 gives the conclusion of this dissertation and gives suggestions for future work for the further development of soft switch technique.
Chapter 2  Soft Switching inverter control with minimized circulation energy

The goal of soft switching is to reduce switching loss and thus achieving higher efficiency. To get a higher efficiency gain, the circulation energy must be minimized to reduce conduction loss. Minimizing the unnecessary circulation energy while maintaining the soft switching condition under all load current condition is the key to justifying the benefit of soft switching. This chapter will mainly focus on optimal control of soft switching inverter because the realization of soft switching inverter is most difficult among power converters due to the nature of alternative load current.

The variable timing control adjusts the advanced trigger time of the auxiliary switch according to the load current level in order to reduce the circulating energy, which is critical for the high power inverter application. The variable timing control scheme was first presented as a general concept for ZVT inverter application [D4]. Later, the experimental performance of the variable timing control was reported for both the ARCPi [D16] and the delta-configured resonant snubber inverter (RSI) ZVT inverter [D14]. Recently, the evaluation results were presented for the ZVT inverter using coupled inductors [G13].

2.1 Overview for Soft switching inverter

According to the placement of auxiliary circuitry, soft-switching inverters can be classified into two categories: DC-side topologies and AC-side topologies. In the DC-side topologies, such as resonant DC-link and quasi-resonant DC-link inverters, the DC link voltage is normally brought down to zero during all the switching transitions. The resonant dc link converter (RDCL) [D2] has a simple power stage structure; however it introduces significant voltage stress which is difficult to overcome.

Unlike DC-side soft-switching inverters, the load-side soft-switching inverters usually offer the advantages of pulse width modulation (PWM) control and soft switching without additional voltage or current stress in the main devices. Therefore, the load-side soft-switching inverters promise to achieve high performance for high-power inverter applications. In the AC-side topologies, there are basically two techniques, zero-voltage transition (ZVT) and zero-current transition (ZCT).
The main advantage of the ZCT topology is that it can achieve zero-current turn-off for all of the switches and diodes in both the main power stage and the auxiliary circuits. Thus, the turn-off loss can be significantly reduced. Also, the main switches can turn on under a zero-current condition and the diode reverse recovery problem could be alleviated [D26][D20][D10].

The auxiliary resonant commutated pole converter (ARCP)[D4] provides an independent current commutation control for each main switch thus maintaining the merits of pulse width modulation (PWM) control. However the ARCP requires the middle point of the dc bus voltage, which brings the complexity of power stage and control implementation. The auxiliary resonant snubber zero voltage transition (ZVT) inverter refers to the type of the circuit firstly proposed in [D14]. Different from ARCP circuit, the resonant snubber based inverter (RSI) forms the resonant circuit at load side without the center tap of dc link capacitor. The major advantages of RSI topology is that it can achieve ZVT turn-on for all the switches in the main power stage and zero current switching (ZCS) for the switches in the auxiliary circuits[D22][D23]. RSI is very good for switch reluctant motor applications, but needs modified PWM scheme if applied to inductor motors. There are some other low cost ZVT schemes [D29][D17] but all need to modify the PWM scheme and possibly with hard turn-off auxiliary switches. The ZVT inverter using coupled inductors [D11] maintains the advantages of soft switching and PWM control while eliminating the need of the middle point in compared to the ARCP. The auxiliary switches only carry partial of the resonant current because the diodes in the auxiliary branch

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**Fig. 2.1 Soft Switching inverter family**

- **DC side**
  - Resonant DC link: D. Divan IAS’86 [D2]
  - DC Rail ZCS P. Tomasin, PESC’95 [D6]

- **AC side**
  - Zero voltage Transition: Vlatkovic, PESC’93 [D8]
    - ARCP McMurray, IAS’89[D7]
    - RSI J.S. Lai [D14]
    - Coupled Inductor [D19]
  - Zero current Transition: Hua, PESC’93 [D10]
    - Mao, IAS’96 [D20]
    - Yongli, 6 switch [D25]
    - Yongli, 3 switch [D27]
take over the other parts. The principle of variable timing control will be illustrated by the example of coupled inductor ZVT inverter with unity turns ratio.

### 2.2 Variable timing control for coupled inductor feedback ZVT inverter

This section presents the design example of variable timing control to minimize the unnecessary current boosting according to the load current condition. The three-phase operation is independent thus no modification of the original hard-switching PWM scheme is needed. The previously proposed inverter can actually turn on the main device at half of the dc bus voltage because of wrong improper timing control. It only solves the diode reverse recovery problems. The turn off loss in main switches is not reduced [D11]. Turn off loss of main switches is significantly reduced by adding snubber capacitors across the main PWM switches. With the proposed control scheme and variable timing control, the true zero-voltage-switching for main switches can be achieved by boosting resonant current to a certain amount. Basic circuit operation and design consideration is presented. A design example for a 650V 75KW ZVT inverter for induction motor is given with the verification of simulation and experiment results. There are further improvement with non-unity turns ratio and will be discussed in chapter 3.

#### 2.2.1 Principle of coupled inductor ZVT operation

Fig. 2.2 shows a proposed coupled inductor ZVT cell. The auxiliary circuit structure for each phase is identical. Each phase auxiliary circuit is composed of a coupled resonant inductor, two diode and two auxiliary switches. The only modification of the previously proposed coupled inductor feedback scheme [D19] is adding resonant capacitors across the main switches, which is shown Fig. 2.2 in gray color. Assume the initial load current is positive and is conducted by lower diode Dn.

![Fig. 2.2 ZVT cell of coupled-inductor feedback scheme.](image-url)
The purpose of the auxiliary circuit is to divert the load current from the main diode \( D_n \) to the opposite main diode \( D_p \) and then turn on the main switch \( S_p \) under zero voltage condition. However, for the control method introduced in [D19], no current boosting is used thus the main switch \( S_p \) is actually turned on at half of the dc link voltage at \( t_4 \). There is no control of the resonant period \( t_2-t_3 \). Fig. 2.4 gives a brief operation waveform of an early-proposed control scheme that does not achieve soft switching.

![Fig. 2.3 Key waveforms of the non-soft switched coupled inductor ZVT inverter](image)

Now consider if the auxiliary switch \( S_{xn} \) is turned on before \( S_n \) is turned off. This will initiate a ramp current through the inductor. Once the magnitude of one branch inductor current exceeds half of the load current, the lower diode turns off naturally. The lower switch \( S_n \) is held on for an additional interval of time so that the inductor current will exceed the load current by certain amount. Then when the lower switch \( S_n \) is turned off, the leakage inductors of the coupled inductor will resonant with snubber capacitors across the main switches. As a result of the resonance, the output voltage swings to the upper rail voltage and clamped by the upper diode for a short period of time. By adding resonant capacitors across the main switches, the resonant period \( t_2-t_3 \) can be properly chosen thus the upper switch \( S_p \) can then be turned on under zero voltage condition when diode \( D_p \) is still conducting. The key circuit operation waveforms are given in Fig. 2.4.
The whole ZVT transition can be divided into following stages as shown in Fig. 2.5:

(a) **Initial stage** \([t_0-t_1]\) \(S_n\) switch is on and Load Current flow via diode \(D_n\).

(b) **Pre-charging stage** \([t_1-t_2]\). At \(t_1\), \(S_{xn}\) is turned on. The voltage across the resonant inductor is the DC bus voltage. Inductor current is charged linearly until it reaches half of the load current \(I_{load}\). \(D_n\) current is decreased to zero at \(t_2\) when resonant inductor current \(I_{Lrs}\) reaches half of the load current.

(c) **Boost-charging stage** \([t_2-t_3]\) \(D_n\) is turned off naturally at \(t_2\); \(S_n\) is held on and conduction the boost current. The auxiliary inductor current linearly increases to a certain designed level: \((I_{Load}+I_{boost})/2\).

(d) **Resonant stage** \([t_3-t_4]\). \(S_n\) is turned off at \(t_3\) with a boost current \(I_{boost}/2\). All two main switches and diodes are off at \(t_3\). The leakage inductor resonant with the capacitors paralleled with the main switches. The lower capacitor voltage resonant to dc bus voltage and clamped by diode \(D_p\) at \(t_4\).
(e) **ZVT Clamping stage** \([t_4-t_5]\) Once diode \(D_p\) is conducted at \(t_4\), the resonant inductor is applied by a negative dc bus voltage. The inductor current is thus decreased linearly. Before the inductor current decreased to load current at \(t_5\), \(S_p\) could be turned on under zero voltage condition.

(f) **Discharging stage** \([t_5-t_6]\) \(D_p\) is naturally turned off at \(t_5\) and \(S_p\) take over the load current gradually. After resonant inductor current decreased to zero at \(t_6\), the load current totally flows from \(S_p\).

(g) **Final Stage** \([t_6-t_7]\) After \(t_6\), the auxiliary switch \(S_{xn}\) can be turned off under zero-current condition at \(t_7\).
2.2. Variable Timing Design

2.2.1 Resonant stage analysis

From the previous section, it can be seen that the resonant stage ends when the anti-parallel diode \( D_p \) conducts. The design goal is to choose the optimal gate timing so that \( S_p \) is turned on during the interval of \([t_4-t_5]\) under ZVT condition while \( D_p \) is conducting under all load current condition with minimized circulation energy. The resonant component design and control method can be understood by the following derivation of the resonant stage.

Fig. 2. shows the equivalent circuit of Fig.5.4 during the resonant stage \([t_3-t_4]\). \( V_s \) is dc bus voltage, \( L_{s1} \) and \( L_{s2} \) are the leakage inductor. \( C_p \) and \( C_n \) are snubber caps for upper and lower leg.
Fig. 2.6 Equivalent circuits during the resonant stage.

To simplify the discussion, a turns ratio of 1:1 is used. Chapter 5 will discuss the coupled inductor ZVT cell design under different turns ratio. The initial condition of the resonant stage is: the voltage across $C_n$ equals to zero; the current across the leakage inductor is $i_{Ls1}$ and $i_{Ls2}$. The circuit can be further drawn in Fig. 2.7.

Fig. 2.7 Equivalent circuit during the resonant stage.

\[ V_s - V_{cs} = L_{s2} \frac{di_{Ls2}}{dt} + V_e \]  
\[ V_{cs} = -L_{s1} \frac{di_{Ls1}}{dt} + V_e \]

If define $i_{Ls}$ and $L$ as following:

\[ i_{Ls1} = i_{Ls2} = i_{Ls} \quad L = L_{s1} + L_{s2} \]

subtracts $V_e$ in (2-1) and (2-2) we have:

\[ V_s - 2*V_{cs} = L_{s2} \frac{di_{Ls2}}{dt} + L_{s1} \frac{di_{Ls1}}{dt} = L \frac{di_{Ls}}{dt} \]

Notice that:

\[ i_{en} + i_{cp} + i_{Load} = i_{Ls1} + i_{Ls2} \quad i_{en} = i_{cp} \]
thus:

\[
C_n \frac{dV_{cn}}{dt} = i_{Ls} - \frac{i_{Load}}{2}
\]  
(2-6)

\[
C_n \frac{dV_{cn}}{dt} = i_{cn}
\]  
(2-7)

Now let’s take a closer look of equation (2-4) and (2-7). \(V_{cn}\) is the voltage across the lower leg resonant cap. \(I_{Ls}\) is the resonant current through one branch of the coupled inductor. Equation (2-4) and (2-7) can be represented in a simple circuit shown in Fig. 2.8. Note that the equivalent resonant capacitor \(C\) value is half of the capacitance across the main switch instead of two times of it. the resonant starts when \(S_n\) turned off with a boost current \(I_{boost}\) The resonant stage ends when \(V_{cn}\) reaches \(V_s\) and been clamped at \(V_s\) when diode \(D_p\) is conducting. The initial condition is: \(i_{Lsini} = (I_{boost} + I_{Load})/2\), \(V_{cnini} = 0\).

![Fig. 2.8 Derived equivalent circuit of the resonant stage.](image)

Then the solution of the above circuit can be easily derived as following:

\[
V_{cn}(t) = \frac{1}{2} V_s (1 - \cos \omega t) + \frac{1}{2} \sin \omega t \times Z_e \times I_{boost}
\]  
(2-8)

\[
I_{Ls} = \frac{I_{Load}}{2} + \frac{\sqrt{2}}{2} \frac{V_s}{Z_e} \sin \omega t + \frac{I_{Boost}}{2} \cos \omega t
\]  
(2-9)

where,

\[
\omega = \frac{1}{\sqrt{C \times L}} \quad Z_e = \frac{\sqrt{L}}{\sqrt{C}} \quad C = C_s / 2
\]  
(2-10)

From (8) it can be seen that only if \(I_{boost}\) is positive can the \(V_{cn}\) tends to exceed \(V_s\). This can also be understood by looking the stage plane of the resonant tank [C11].
The initial resonant inductor current level does affect the process of resonance. As shown in Fig. 2.9 (a) and Fig. 2.11 (b), if the auxiliary switch does not have sufficient leading time before turn-off of the main switch, the body diode is conducting current when the main switch $S_n$ is off. The anti-parallel diode of power devices clamp $V_{Cn}$ to zero and the resonant inductor current will linearly increases until it reaches the load current, which is represented by the locus from A to B in the phase plane Fig. 2.10(b). It takes nearly half cycle of resonant period for resonant tank to change from B to C. Only at point C, $V_{ce}$ of $S_p$ is zero. Then $V_{ce}$ of $S_p$ will build up immediately again due to the continuing resonance. It means that practically the precise load adaptive deadtime control is required to get the perfect zero voltage turn-on if no boosting current is introduced.

If the auxiliary switch do have sufficient leading time before turn-off of the main switch, which stands for $I_L(0^-) > I_{load}$, the resonant process is shown in Fig. 2.9 (a) and Fig. 2.11 (a). There is no linear charging of the resonant inductor; the circuit starts the resonance right away when the main switch $S_n$ turns off. The capacitor voltage $V_{Cn}$ will be clamped by diode to DC bus voltage $V_s$ as long as the total resonant inductor current $2*i_{Lr}$ is larger than load current. This period represents the trajectory B to C in Fig. 2.11 (a). During this period, the main switch $S_p$ could be turn-on under zero voltage condition. Such a situation is desired to guarantee the realization of ZVT turn-on. If turn-on signal applies to $S_p$ after C point, the voltage across $V_{ce}$ of $S_p$ will be swing back from zero again and ZVT turn-on will be lost. Based on above analysis, one can see that how to control the pre-charging current of the resonant inductor plays an important role in realizing the ZVT turn-on.
Using an example with a dc bus voltage of 650V, resonant capacitor of 0.22 µF, leakage inductor L=3 µH, fixed charging time $t_3-t_2=1$ µs, the equivalent capacitor voltage as a function of the load current in Fig. 8 is drawn to get a better understanding of the current boosting.
When the capacitor voltage reaches dc bus voltage at \( t_4 \), \( S_p \) can be turned on under zero voltage condition. The boosting current \( I_{\text{boost}} \) actually provided a ZVT zone from \( t_4 \) to \( t_5 \). It can be seen from Fig. 8, for a heavy load condition, the margin of ZVT zone is much smaller than the margin under the light load condition. Thus the concept of variable charging time control is to maintain a constant boosting current by changing the charging time \( t_3-t_2 \). This way, the ZVT condition can still be maintained while minimized unnecessary over-boosting of the resonant current. Fig. 9(a) and (b) shows the same example with a variable charging time control to achieve a fixed boosting current \( I_{\text{boost}}=80\text{A} \). With a fixed \( I_{\text{boost}} \), the time \( t_4 \) are fixed thus make it simple to select a proper turn on time for \( S_p \). \( I_{\text{boost}} \) value is selected so that the ZVT zone \( t_4-t_5 \) is around 500ns.
2.2.2.2 Timing design guideline

The first step is to select the pre-charging timing of the auxiliary gate signal. As stated in the previous section, a proper boost current \( I_{\text{boost}} \) needs to be maintained to ensure ZVT transition. Based on the resonant capacitor voltage during the resonant stage shown in Fig. 2.12(a), the boost current value is chosen such that the ZVT zone can be maintained in the range of 400ns-600ns. Then the overlapping time \( T_{\text{pre}} \) of the auxiliary switches and main switches can be calculated from the following:

\[
T_{\text{pre}}(I_{\text{Load}}) = \frac{I_{\text{boost}} + I_{\text{Load}}}{V_s} \cdot L
\]  

(2-11)

It can be derived from Fig. 2.11 that the resonant period is depends only on the natural resonant period \( T_r \) and total boost current \( I_{\text{boost}} \):

\[
T_{\text{resonant}} = \arctan\left(\frac{V_s}{I_{\text{boost}} \cdot Z_s}\right) \cdot \frac{T_r}{\pi}
\]  

(2-12)

For constant boost variable timing control method, the deadtime soft switching inverter should satisfy the following:

\[
T_{\text{resonant}} \leq T_{\text{deadtime}} \leq T_{\text{resonant}} + T_{\text{discharge}}
\]  

(2-13)
\[ T_{\text{discharge}} = L_r \left( \frac{I_{\text{boost}}}{V_r} \right) \] (2-14)

Thus the deadtime must be selected accordingly. An improper designed deadtime may result in loss of ZVT condition even with high boosting current. The deadtime is chosen based on (2-13). The Turn on duration of auxiliary switch is chosen by:

\[ T_{\text{auxwidth}} \geq 2 \cdot \max(T_{\text{aux}}) + T_d \] (2-15)

Typically the designed auxiliary pulse width should not exceed 6us to reduce duty cycle loss.

![Fig. 2.13 Normalized Boost current with resonant timing](image)

Fig. 2.13 gives the normalized resonant timing via boost current. Typically normalized boost current can be chosen from 0.5-1. Boost current should be as small as possible provided the ZVT zone can be achieved for about 350ns to 600ns. Once \( I_{\text{boost}} \) is chosen, \( T_{\text{deadtime}} \) can be selected based on Fig. 2.13 accordingly. Intuitively, when \( I_{\text{boost}} \) equals to 1, the resonant period is exactly a quarter of resonant cycle.

When the load current goes to negative, it is not necessary to activate the auxiliary switch since \( D_p \) will be freewheeling naturally after turn of \( S_n \). Equation (2-11) also indicates the condition to deactivate the auxiliary switch is when the negative load current equals \( I_{\text{boost}} \)
2.2.2.3 Design Example

Following the design guideline, the coupled inductor ZVT inverter with the proposed variable timing control is designed. The specification of the inverter is \( V_s=650\text{V} \) and \( I_{\text{pkLoad}}=150\ \text{A} \). The detailed design results are presented below:

Snubber capacitor is selected as 0.22\(\mu\text{F} \) based on the device test results.

Limiting the peak resonant current in one branch less than 220 A, the total leakage inductance \( L \) is selected as 6.0 \( \mu\text{H} \).

Calculate \( T_r \) based on \( L \) and \( C \). \( T_r=5.1\ \mu\text{s} \)

Based on Fig. 2.13, \( I_{\text{boost}} \) is chosen to 40A. (about 0.5 in normalized value) The auxiliary pre-charging time is then calculated by equation (2-11) based on load current feedback. Fig. 2.14 shows the required \( T_{\text{pre}} \) according to this example.

![Fig. 2.14 Select pre-charging time \( T_{\text{pre}} \) (us) based on load current](image)

Fig. 2.14 Select pre-charging time \( T_{\text{pre}} \) (us) based on load current

The main switch deadtime is chosen as 2.2\(\mu\text{s} \). The auxiliary pulse width is chosen as 6\(\mu\text{s} \). Then all the design parameters are summarized as follows: \( V_s=650\text{V} \), \( I_{\text{pkLoad}}=150\ \text{A} \), \( L=6\ \mu\text{H} \), \( C=0.22\ \mu\text{F} \), \( T_r=5.1\ \mu\text{s} \), \( T_d=2.2\ \mu\text{s} \), \( I_{\text{boost}}=40\text{A} \), \( T_{\text{auxwidth}}=6\ \mu\text{s} \).

Fig. 2.15 shows the key waveforms by PSPICE simulation with the designed parameter under load current of 150A. Switch \( S_p \) is turned on when diode \( D_p \) is conduction.
Fig. 2.15 ZVT turn on transition by PSPICE simulation.

Fig. 2.14 actually reveals another very important issue. The pre-charging time goes to negative when current changing directions. That means no pre-charging is needed. As shown in Fig. 2.16, at heavy load, the commutation is naturally done when the bottom switch Sn is turned off. So we have the option to disable auxiliary switch Sxn (option 2) or apply a minimum pre-charging time (option 1). At light load, Both auxiliary switch needs to be turned on with a small Tpre. This property is very critical for proper operation since the load current detecting would not needs to be very accurate at light load.

In summary, the basic rules of the ZVT variable timing control are as follows:

1. The load current direction is required to determine the type of commotion. However, the delay timing is symmetrical at light load thus the direction is not critical at zero-crossing;

2. For a commutation from diode to switch, Tpre is adjusted according to the load current amplitude; a constant boost current control is desired;
3. For a commutation from switch to diode, there is no need to turn on $S_x$ when the load current is sufficient. If the load current is small, $T_{pre}$ is used to help establish some current in the auxiliary inductor.

### 2.2.3 Experimental results

Single phase ZVT test for variable timing control with reduced power is performed to verify the concept of constant boost current control with variable timing. Fig. 2.17 shows the resonant peak current changes according to the load current by constant boosting current control. The controller is built by analog circuit. Current feedback is used to control the delay of the auxiliary circuit.

![Fig. 2.17 (a) Option 1: without negative blocking](image1)

![Fig. 2.17 (b) Option 2: with negative blocking](image2)

**Fig. 2.17** Resonant current with load adaptively.

Fig. 2.18 Shows the achievement of ZVT condition with variable timing control. The $S_p$ gate signal is applied when the voltage across $S_p$ drops to zero.

![Fig. 2.18 S_p Gate is turned on when $V_{Sp}$ drops to zero.](image3)

The proposed ZVT scheme offers the advantages of three-phase independent control without any modification of SVM techniques. The inductor coupling provides the reset mechanism for the resonant
inductor current thus the auxiliary switch can be turned off under zero current condition. Auxiliary switches only need to carry half of the load current. Standard six-package module can be used for auxiliary power stage. However, the circuit requires relatively more auxiliary components thus can be more costly in compare to other soft-switching schemes. Magnetic component design is also complicated. There is also magnetizing current reset problem and that be discussed in chapter 5. However, for high power and high performance soft-switching applications, the proposed coupled inductor feedback ZVT scheme is still quite attractive.

It is very difficult to implement in analog circuit because of nonlinear of feedback loop and complicated tuning effort. With the fast development of digital integrated circuit and powerful microprocessor, a DSP+EPLD based solution would be a better solution. The next section will introduce an universal method to implement variable timing control.
2.3 An universal method to achieve variable timing control for soft switching inverters

In the PNGV project, three 55kW soft switching inverters need to be developed: ARCP ZVT [D4], six-switch ZCT [D25] and three-switch ZCT [D27] inverter. The goal is to minimize the effort on control hardware design. A hard switched base line inverter with sophisticated motion control algorithm is already developed in Virginia Power Electronics Center with years of effort. The goal is to develop a “plug in” type of soft switching controller to generate all the control gate signals based on the original hard switched PWM signals. Fig. 2.19 shows the overall soft switching inverter diagram. By adding the auxiliary circuits, the hard switched inverter can be turned into a soft switching inverter with minimal efforts. No motor control programs will be changed except changing the deadtime. This section is to explore a universal method to implement variable timing control by digital microprocessor and EPLD.

Fig. 2.19 A “piggy pack” structure for soft-switching PWM inverter.
2.3.1 Requirement of soft-switching inverter PWM Pulse

In the last chapter, the typical gate signal of a coupled inductor ZVT inverter is proposed. The ARCP gate timing is almost identical to that of coupled inductor. Fig. 2.20 shows the gate timing requirement for six-switch ZCT inverter [D26].

Because the ZCT needs similar resonant path even at light load, the control timing is asymmetrical. Thus the detection of load current becomes critical. Besides, the ZCT have excess circulation energy which doesn’t reduce significantly at light load. This makes it almost impossible to achieve proper ZCT at zero current condition. Thus the solution is to disable the ZCT operation at light load. When the load current falls bellow threshold, the ZCT operation is blocked completely. The typical value is about 1/4-1/5 of the peak load current. This is a significant drawback of existing ZCT inverters. First, the EMI noise reduction could be very much hampered since the inverter is operated at hard switched mode at about 1/5 of the line cycle; second, the energy stored in resonant capacitor right before the cut-off level will be circulation till it’s completely dissipated by parasitic loop resistance. The circulation current will be added on top of the hard switching current. This will make it even worse case than regular hard switching condition at light load.
For digital implementation, it is very simple to disable the gate signal. The approach here is to generate the auxiliary pulses based on the edges of the main PWM signals. The advantage of this approach is that the time constant is only depends on load current and not depend on PWM duty cycles. A much slower update rate for the time constant could be used. This is extremely important for saving processing time with limited I/O capability. The turn-on time and pulse width of the auxiliary pulse can be specified by the time delay data written to the EPLD. Fig. 2.21 shows the universal PWM pattern for any soft switching inverter. The italic time constant is data transferred from the DSP to EPLD via the PIO port. In the event that an auxiliary pulse should be eliminated, the time constant is a zero value so that the logic circuit will not generate a pulse output. However, to generate the auxiliary pulse earlier than a corresponding main PWM pulse, it is necessary to delay the main PWM pulse for a certain amount of time. The main PWM pulse is delayed to an extent so that it can accommodate the maximum charging time needed for the auxiliary circuit.
For different soft switching schemes, the delay time is different even at the same load current level. Besides, the calculation of delay time is time consuming if it needs to implement in real time by DSP. Fig. 2.22 shows the concept of using a lookup table to locate time delay command from the load current feedback. The required delay time is stored in a standard lookup table thus it take only a few lines for the DSP to get the corresponding time delay data. For different soft switching control application, only the lookup table needs to be updated. This saves a lot of coding effort and makes the variable timing controller very flexible. Fig. 2.23 shows the picture of ADMC300 DSP board.

Fig. 2.23 ADMC300 DSP board

Fig. 2.24 shows the interface board for soft-switching operations. The core of the interface board is an EPLD logic chip (EPM9400)). The EPLD chip contains all the necessary control logic schemes in order to generate the gate signals of six main switches and auxiliary switches for any soft-switching topologies. The DSP board transfers information to the interface board to specify time delay constants. Fig. 2.25 shows the assembled interface board with DSP and main driver board.

Fig. 2.24 Interface board for soft-switching operations

Fig. 2.25 Assembled interface board with DSP and main driver board
2.3.2 Transfer Data from DSP to EPLD

Since ADMC300 has no external data bus, its PIO ports are used to provide the necessary data to EPLD. Then, the EPLD generates auxiliary PWM signals as well as main PWM signals using both the downloaded time delay constants and the outputs of ADMC300 PWM generator. The outputs of ADMC300 PWM generator are used as the trigger signals of the EPLD operations. Fig. 2.26 describes the principle function of the interface board.
Among the 12 available digital PIO pins of ADMC300, 10 pins are used for transferring data to EPLD on the interface board. Fig. 2.27 shows the pin assignment. Pins PIO0-PIO7 are used for transferring any necessary information as either data or address bus. Both PIO 8 and 10 are used for data transfer control. PIO8 is used as DATA or ADDRESS selection. Low status of this pin means that the following values on bus are data for timing constants, while high status implies that the values on bus are the address of data. PIO10 is used as I/O enable.

To achieve a more efficient way of data transfer, each data slip consists of an initial data address followed by an array of data. The initial data address is latched in an address counter and automatically refreshed according to data transfer. Multiplexing the eight-line address bus gives 256*8 data spaces which is sufficient for any kind of soft-switching controls.

An address counter is used in order to generate the desired addressing method, as shown in Fig. 2.28 (a). The first action occurs when the address/data line (PIO8) goes high which makes it ready to lock the initial data address from the bus to the address register (an eight-bit counter). At the falling edge of PIO10 (/IOEN), the initial data address is been locked into the address counter. After PIO8
gives to low-status, it is ready to latch data to the register. Each time before changing the bus value, the IOEN signal goes high to avoid possible glitches in the bus. The address counter uses the rising edge of the IOEN signal to accomplish the incrementing of the register address. At the falling edge of the IOEN signal, data is being latched into the data register. The case is the same for the control register and dead-time register except only one level data latch is needed. The starting address of the data registers is decided by EPLD encoding. Generally, 12 time-constant registers are encoded in a consecutive manner, while control register and dead-time register can be in a separate address field. In this manner, we will transfer one address followed by an array of data that will be fitted into corresponding data registers. This can save lots of addressing time and make it more realistic to be used in a high frequency inverter application.

Fig. 2.28 Logic to generate addresses.

Fig. 2.29 shows the control timing of transfer data from DSP to EPLD. As a brief example, suppose we write 20h, 30h, 28h, and 45h to the address start from 10h. The procedure for these data transfer is as follows:

- At t0, set IOEN to high, then one can write initial address information, which is 0Fh
- At t1, set ADDR/DATA to high, prepared to latch the address information the address counter
• At t2, set IOEN to low, at this time ADDR/DATA is high, thus 09h is being latched to address counter

• At t3, set ADDR/DATA back to low, prepared to latch data information to data register

• At t4, set IOEN to high, first it will increase address counter, thus point to first data address of 10h, second it will be prepared to change bus information. After t4, bus PIO0-PIO7 can be changed to the first data of 20h.

2.3.3 Generate PWM signal based on Data transferred to EPLD

After the time delay data is transferred successfully to the EPLD, the next objective is to use these data to generate auxiliary PWM signals. Fig. 2.30 shows block diagrams to generate the PWM pulses
based on the above concepts. There is also a minimum pulse width requirement for PWM generation that is implemented in the EPLD.

Fig. 2.30 Functional diagram for auxiliary PWM pulse generation in EPLD.

Fig. 2.31 PWM generation Mode Block Diagram.

Fig. 2.31 shows a schematic functional block diagram of PWM generation for single phase. The other two phases are independent and identical. Only three upper device PWM input signals are used for three phases. The bottom device PWM pulses are generated within the EPLD.

2.3.4 Experimental results

Fig. 2.32 shows the experimental results for ARCP inverter with variable timing control. Auxiliary switch action is block at heavy load, as shown in option 2 in Fig. 2.16, to reduce unnecessary switch action. Fig. 2.32 (a) and (b) shows the resonant waveforms at high and low load current levels. Fig. 2.33 shows the experimental results for ZCT inverter with optimal variable timing control.
Fig. 2.32 (a) Waveforms on line cycle scale

![Waveforms on line cycle scale](image)

Fig. 2.32 (b) Resonant waveforms at heavy load

![Resonant waveforms at heavy load](image)

Fig. 2.32 © Resonant waveforms at light load

![Resonant waveforms at light load](image)

Fig. 2.32 Experimental waveforms with variable timing control.
Fig. 2.33 ZCT switching waveforms with optimal variable timing control

Fig. 2.34 shows the estimated loss distribution comparison of the variable pre-charging time control in the ARCP and couple inductor ZVT (ZVTCI) in the case of 20 KHz operation. The conditions are specified as follows: $V_{dc}=325\,\text{V}$, $I_{rms}=200\,\text{A}$, $M=0.8$. Fig. 2.35 shows the significant efficiency improvement by optimal variable timing control under various operation conditions.

Fig. 2.34 Loss reduction between fixed and variable timing control in PNGV project.
In summary, the optimal variable timing control is essential for soft switching inverter to achieve higher efficiency than hard switching inverters [A2]. A general design guide line is presented with example of coupled inductor ZVT inverter. A universal flexible controller is proposed to generate variable timing control signal for three soft switching inverters. However, the controller involves complicated EPLD design and will increase the system complexity and overall cost.
Chapter 3 Load adaptive soft switching with fixed timing control

Last chapter explored using variable timing control to adjust the advanced trigger time of the auxiliary switch to minimized energy circulation in the resonant tank [G13]. Such a load current adaptive feature is even more important for high power inverter applications since the load current is always changing over the line cycle. Although the variable timing control achieves zero-voltage-switching (ZVS) operation with reduced circulating energy, it is necessary to acquire the instantaneous load current to synthesize the control signals of the auxiliary devices. The current information will be somehow critical to implement soft switching inverter and the current sensing itself will incur extra cost and complexity. Additional EPLDs (electronic programmable logic devices) are typically required to facilitate the task. This adds to both the complexity and development time of control design implementation. The overall cost on extra parts and labor make soft switching not an attractive solution for commercial PWM inverters. A simple, load current independent, easy to implement soft switching solution will be more attractive.

This chapter will explore the methods of realizing load adaptive soft switching with fixed timing control. First, a soft switching chopper with near zero voltage switching approach is presented. The key idea is to adjust the ratio of charging time and resonant time in order to get a near zero voltage switching with fixed time control. Second, a load adaptive fixed timing control soft switching chopper is presented utilizing diode reverse recover current as extra boost current. A more generalized fixed timing method is then proposed by comparing and analysis a family of soft switching inverter cell. Finally, an inductor coupled fixed timing ZVT scheme is proposed with a 120kW prototype inverter design. All the fixed timing approach is analyzed and presented with both simulation and experimental verification.

3.1 A near-zero-voltage switching ZVT chopper design with fixed control timing

The objective of this section is to emphasize the design method that allows a two-quadrant chopper to have an efficient near-ZVT operation for a wide-range load conditions. Using the proposed design criteria, a 10-kW soft-switched commercial chopper was built and tested for a magnetic levitation (MAGLEV) system. The new design achieves dv/dt and loss reduction, turn-on current spike and noise reduction, and finally the improvement of efficiency and associated heat sink size reduction.
Because the load current of the chopper is only in one direction, only one auxiliary branch is needed and the control is relatively simple. Simulation and experimental results prove that the proposed design method is effective, and the proposed soft-switching circuit is well suited for two-quadrant chopper applications. Although the analysis is based on resonant snubber ZVT cell, the basic design concept applies to other ZVT soft switching tank design as well.

3.1.1 Operation Principle

Fig. 3.1 shows a soft-switching chopper circuit with auxiliary resonant snubber for a two-quadrant chopper. The chopper bridge consists of two synchronously switching pairs, switches $S_1$-$S_2$ and diodes $D_1$-$D_2$. The diodes provide a freewheeling current path and a reverse voltage across the load for two-quadrant operation. The lossless snubber capacitors are added across main devices, and the auxiliary branch is added in between two phase-legs. The auxiliary branch consists of one auxiliary switch, one fast reverse recovery diode, and one resonant inductor. Since the load current flows in uni-direction, only one auxiliary branch is needed to achieve soft switching.

![Fig. 3.1 The proposed soft-switching chopper circuit.](image)

Fig. 2 illustrates the operation modes for the proposed soft-switching scheme. The basic control is to turn on the auxiliary switch, $S_{aux}$, before turning on the main switch, $S_1$ and $S_2$. The auxiliary branch takes over the current from the freewheeling diode and resonates with capacitors in parallel with the main switch. The main switch is turned on while the voltage across the main switch drops nearly to zero after resonance. Although only near-zero-voltage switching can be achieved with the proposed fixed timing control, the diode reverse recovery and $dv/dt$ problems of the chopper circuit are effectively solved.
The circuit operation modes are described in Fig. 3(a) – 3(f).

Initially at time \( t_0 \), all switches are off, and the load current is freewheeling through \( D_1 \) and \( D_2 \) as shown in Fig. 3(a). Operation modes for a complete cycle are described in detail as follows.

Mode a \((t_0 - t_1)\): Assume that load current is positive when \( D_1 \) and \( D_2 \) are conducting the load current, and the main switches \( S_1 \) and \( S_2 \) are off.

Mode b \((t_1 - t_2)\): Following the pulse-width-modulation (PWM) commend, the auxiliary switch \( S_{aux} \) turns on at \( t_1 \), the current in \( L_r \) increases linearly and the current in diodes \( D_1 \) and \( D_2 \) decreases linearly. The auxiliary branch diverts the current from the freewheeling diode gradually.

Mode c \((t_2 - t_3)\): After the auxiliary branch current is larger than the load current at \( t_2 \), diodes \( D_1 \) and \( D_2 \) turn off naturally. Then all four snubber capacitors resonate with the auxiliary inductor. The capacitor across the switch discharges with a finite rate to allow the switch voltage drop to zero.

Mode d \((t_3 - t_4)\): At the end of the resonant stage, the snubber capacitors are discharged to zero voltage at \( t_3 \). At this moment, the main switch can be turned on at zero-voltage condition. In reality, the dissipative components in the resonant branch may prevent the voltage from swinging down to true zero but close enough. However, even if the voltage can swing to true zero, it is difficult to turn on the main switch at the exact moment that the capacitor voltage drops to zero without proper sensing, the main switch can thus be turned on at a near-zero-voltage condition. This near zero-voltage is created by the auxiliary resonant circuit for a short period, which can be considered as “near zero-voltage
transition” or near-ZVT. After the main switches turn on, the inductor current decreases linearly due to reverse voltage polarity.

Fig. 3.3 Operation stages of ZVT chopper.

Mode e (t₄ – t₅): After the resonant current decreases to zero at t₄, the auxiliary switch gate signal can be turned off at t₅. The main switches then conduct the load current, and the auxiliary switch is turned off under zero-current condition.
Mode f \((t_6 - t_7)\): Main switches turn off with lossless snubber capacitors. Once the capacitors \(C_1\) and \(C_4\) are charged to \(V_{dc}\), and \(C_2\) and \(C_3\) are discharged to 0, the load current is transferred to diodes \(D_1\) and \(D_2\), and the circuit operation returns to Mode a.

### 3.1.2 Design criteria

#### 3.1.2.1 Design Analysis

At the end of the resonant stage \((t_2 - t_3)\), the voltage across the main switch should be fully discharged so that the main switches can be turned on under zero voltage. The key design point is how to catch the zero-voltage instant and turn on the main switches exactly at or as close as possible to \(t_3\). The following design analysis will focus on this particular resonant stage to ensure a proper resonant operation. Once the resonant stage is well designed, the component value and control timing can be determined. As long as the resonant inductor current reaches the load current at \(t_2\), \(L_r\) begins to resonate with the capacitors. The equivalent circuit during the resonant period can be shown in Fig. 3.4.

![Fig. 3.4 Equivalent circuit of resonant stage.](image)

To simplify the circuit, \(C_1\) is flipped down, and \(C_4\) is flipped up. The initial condition (IC) of the resonant tank is given in Fig. 3.5. Finally, a very simple circuit can be drawn as shown in Fig. 3.5. In this figure, \(C_r^*\) and \(L_r^*\) are the equivalent resonant capacitor and inductor during the resonant stage, i.e.,

\[
C_r^* = \frac{(C_1 + C_2)(C_3 + C_4)}{C_1 + C_2 + C_3 + C_4}, \quad L_r^* = L_r
\]  

\[(3-1)\]
In the case of $C_1 = C_2 = C_3 = C_4$, we have $C_r^* = C_r = C_1$. The final equivalent circuit is a very simple LC resonant tank with zero initial condition. Here we notice two important points: 1). The resonant stage is independent of load current condition; and 2). The duration of the resonant stage is fixed at half of the natural resonant cycle of resonant tank $T_r$. The resonant capacitor voltage and inductor current can be expressed as

$$
V_{C_r}(t) = V_{dc}(1 - \cos(\omega t)) \tag{3-2}
$$

$$
i_{L_r}(t) = i_L + \frac{V_{dc}}{Z}\sin(\omega t) \tag{3-3}
$$

where

$$
Z = \sqrt{\frac{L_r}{C_r^*}}, \quad \omega = \frac{1}{\sqrt{L_r C_r^*}}, \quad T_r = 2\pi \sqrt{L_r^* C_r^*} \tag{3-4}
$$

The current stress on the auxiliary branch can be obtained as:

$$
I_{Max}(Z) = I_{Load} + \frac{V_{dc}}{Z} \tag{3-5}
$$

The auxiliary switch pre-turn-on time, $T_{pre}$, is the interval from $t_1$ to $t_3$, which is the sum of inductor charging time $T_1$ and the resonant stage duration, $T_2$. A quality factor $Q(Z)$ is defined here as the ratio of $T_2$ to $T_1$, as shown in (7).
If the main switch is turned on precisely with $T_1+T_2$ delay after the auxiliary switch, and the circuit components are lossless, the exact ZVT condition can be achieved. It should be noted that according to (6), $T_1$ is load current dependent, it is necessary to adjust the pre-turn-on time of the auxiliary switch to meet different load current condition if an exact ZVT is desired. To implement this it is necessary to use variable timing control to change $T_{pre}$ according to the load current condition. However, such a variable timing control requires current sensing and additional complicated control circuitry. It is desirable to look for a simple solution with fixed-timing control but not losing ZVT. The proposed approach is described as follows.

Note that if $L_r$ and $C_r$ can be chosen such that $T_2 >> T_1$ or $Q(Z)$ is sufficiently large with a fixed pre-turn-on time, $T_{pre}=T_{1(normal)}+T_2$, where $T_{1(normal)}$ is the charging time under normal load condition, the near-ZVT can then be obtained. Since $T_2$ is much larger than $T_1$, even if the main switch is turned on a little earlier or later due to the load current variation, the voltage will only swing back to a finite amplitude, but close enough to zero-voltage condition.

To reduce the peak resonant current so as to reduce the circulating energy, it is desirable to have large $L_r$ and smaller $C_r$. However, for a wide range of near-ZVT operation, it is desirable to have a large $C_r$ and a small $L_r$ so that $T_2 >> T_1$ condition is satisfied. Since a typical MOS gated device can withstand a high peak over-current in a short period, with a larger $C_r$ and a smaller $L_r$ may cause a high peak current but not cause a problem of finding an economical device to handle it. In other words, a small tank impedance is desirable in the most cases, and thus the tank impedance $Z$ becomes an important design factor. The capacitor value can be selected based on the $dv/dt$ requirement and turn-off loss test. The resonant inductor value can be calculated with the predetermined $Z$, and the pre-turn-on time of the auxiliary switch is optimized at the rated load condition. That is to let $T_{pre}$ equals $T_1+T_2$ under the rated load condition. As a result, the worst case happens under no-load and heavily overload conditions.
3.1.2.2 Design Procedure Example

In a commercial MAGLEV chopper application, the nominal load current $I_{\text{Load}}$ is 25 A, and the dc bus voltage $V_{\text{dc}}$ is 300 V. The design procedure can be described as follows:

**Step 1:** Decide resonant tank impedance so that the quality factor $Q(Z)$ is large enough to satisfy near-ZVT condition with fixed timing control. However, the peak resonant current $I_{\text{max}}$ must be limited to avoid excessive loss in the auxiliary branch. To facilitate the comprehensive of the design under different condition, the tank impedance and resonant peak current is normalized as follows.

$$Z_{\text{base}} = \frac{V_{\text{dc}}}{I_{\text{Load}}} \quad Z = \frac{Z}{Z_{\text{base}}} \quad I_{\text{base}} = I_{\text{Load}} \quad I_{\text{max}} = \frac{I_{\text{max}}}{I_{\text{base}}}$$

(3-8)

Thus equation (5) and (7) can be rewritten as:

$$I_{\text{max}}(Z) = 1 + \frac{1}{Z} \quad (3-9)$$

$$Q(Z) = \frac{T_2}{T_1} = \frac{\pi}{Z} \quad (3-10)$$

As shown in Fig. 3.6, $Z$ is chosen as 0.542 which corresponds to a $Q(Z)$ value of 6.0. In this case, the estimated normalized peak resonant current is 2.845 as indicated in Fig. 3.18. The selection process can also start with limiting the peak current first, and check with $Q(Z)$ to allow a wide range near-ZVT condition.

![Fig. 3.6 Ratio of $T_2$ to $T_1$ with respect to normalized impedance](image)
Fig. 3.7 Normalized resonant branch peak current $I_{\text{max}}$ as a function of $Z$

**Step 2:** Select $C_r$ and $L_r$ so the $dv/dt$ requirement can be satisfied, and the resonant cycle $T_r$ is proper for actual implementation. Since the main switch turn-off loss can only be reduced by snubber capacitors, it is necessary to perform device test to determine a proper value for $C_r$. Fig. 3.8 shows the test results of turn-off energy under different snubber capacitance and load current conditions. Select a $C_r$ value so that further increments of $C_r$ will not significantly further reduce turn-off loss. In the meantime, it is necessary to let resonant cycle, $T_r$, be a reasonable value so that it is not too small for practical implementation and not too large to avoid loss of duty cycles. Fig. 3.20 shows the changes of resonant cycle, $T_r$, under different $C_r$ and $Z$ values. Based on the above criteria, a value of 0.1 $\mu$F was chosen for $C_r$. The resonant inductor value is then calculated by $L_r = Z^2C_r = 4\mu$H, and the tank resonant cycle $T_r$ is around 4 $\mu$s.

![Normalized resonant tank impedance graph](image1)

![Normalized resonant peak current graph](image2)

![Normalized resonant tank impedance graph](image3)

![Normalized resonant peak current graph](image4)

Fig. 3.8 Turn-off energy as a function of $C_r$ under different load conditions.
Fig. 3.9 Variation of $T_r$ as a function of $Cr$ and $(0.25, 0.4, 0.542, 0.8)$.

**Step 3:** Determine the pre-turn-on time of the auxiliary switch, $T_{pre}$, and the turn-on duration of the auxiliary switch, $T_{aux}$. $T_{pre}$ is the sum of the pre-charging time $T_1$ and resonant period $T_2$. $T_1$ is load current dependent and can be chosen under static load current condition. Since $T_2$ is much larger than $T_1$, the variation of $T_1$ will not affect much of the near zero-voltage condition. In this example $T_{pre}$ is chosen as 2.3 µs. $T_{aux}$ is the turn-on duration of the auxiliary switch. $T_{aux}$ is not critical because the auxiliary switch can be turned off after the current reduces to zero. So $T_{aux}$ should be larger than $2T_1 + T_2$, and the selection in this case is $T_{aux} = 3$ µs.

**Step 4:** Summarize the design parameters and select proper auxiliary switch and passive components. Up to this point, the major design has been completed. The remaining jobs such as switch selection and magnetic design can be left to practicing engineers. The complete design summary is listed as follows: $V_{dc} = 300$ V, $I_{load} = 25$ A, $C_r = 0.1$ µF, $L_r = 4$ µH, $T_r = 4$ µs, $T_{pre} = 2.3$ µs, $T_{aux} = 3$ µs, $Z = 6.325$, $Z = 0.542$, $Z = 5.96$, $I_{max} = 72.4$ A, $I_{max} = 2.845$.

### 3.1.3 Simulation and experimental results

The effectiveness of the proposed control scheme can be proved by Pspice simulation with the above design parameters. Actual commercial IGBT SPICE models are used, but parasitic parameters and dissipative components like capacitor ESR and ESL are not included in the simulation.

Fig. 3.10 shows the key waveforms of the chopper operation. Fig. 3.22(a) shows the main switch voltage, $V_{sw}$, and current, $I_{sw}$, waveforms. It can be seen that the main switches operate well in near
zero-voltage turn-on condition. The turn-on dv/dt is controlled by the resonant time constant, $T_r$ and the turn-off dv/dt is proportional to the load current but is limited by the added snubber capacitors. The main switch diode reverse recovery problem is eliminated, and thus there is no current spike during main switch turn-on. Fig. 3.10(b) shows that the auxiliary branch peak current, $I_{Lr}$, is around 70 A, as expected in the previous design section. Fig. 3.10(c) shows the main switch gate drive signal, $G_{\text{main}}$, and auxiliary switch gate signal, $G_{\text{aux}}$.

![Simulated key waveforms of near-ZVT chopper scheme.](image)

It is possible that near zero-voltage turn-on condition may be lost if the timing is not controlled properly. Fig. 3.11 indicates that the main switch is turned on while the switch voltage swings up to a certain value with the situation that the pre-turn-on time $T_{\text{pre}}$ is longer than the designed value.

![Resonant current $I_{Lr}$ (A) and switch voltage $V_{sw}$ (V) waveforms under incorrect timing.](image)

Fig. 3.12 (a) – 12(b) show the simulated waveforms of the voltage across the main switch and the resonant current during turn-on process with designed control timing under different load currents: (a) 7.5 A, (b) 17 A, (c) 28 A, and (d) 37 A. It can be seen that near-ZVT turn-on of the main switch is satisfied for all load current conditions.
Fig. 3.12 Resonant current $I_{LR}(A)$ and switch voltage $V_{SW}(V)$ under different load conditions.

In this simulation, the load current is considered as a constant current source during the switching period with a value corresponding to the actual experimental load current as described in the next section for the comparison purpose.

The above-designed soft-switching chopper has been fully tested with the same parameters that were used in the simulation. Fig. 13 shows experimental key waveforms of load current, $I_{LOAD}$, resonant current, $I_{LR}$, switch voltage, $V_{SW}$, and dc input current, $I_{in}$. The measurement of dc input current is for the purpose of loss calculation. To verify loss of ZVT with inappropriate timing, an experiment was conducted under the condition addressed in Fig. 3.11. Fig. 3.14 shows the corresponding test results of losing ZVT condition. As can be seen from Fig. 14 that an oscillation occurs when the switch turns on after the voltage is been swung back to a relatively high voltage level.
Fig. 3.13 Experimental waveforms of the ZVT chopper scheme.

Fig. 3.14 Switch voltage waveform under incorrect timing.

Fig. 3.15 (a) – 15(d) show experimental waveforms of the load current, $I_{\text{Load}}$, the resonant current, $I_{\text{Lr}}$, and the voltage across the switch, $V_{\text{sw}}$, under different load current conditions that are corresponding to Fig. 3.12 (a) – (d) conditions. The timing design is to ensure that the main switch turns on at near zero voltage under the nominal operation condition (25 A for the example chopper case). Waveforms indicate that even at extreme conditions such as 30% (lightly loaded) in Fig. 3.15 (a) and 150% (overloaded) in Fig. 3.15d), the switching waveform is clean, and the near-ZVT condition is well satisfied. Loss evaluation results indicated that the total loss reduction was 31% at the nominal load condition, as indicated in Fig. 3.16.
Fig. 3.15 Resonant current and switch voltage under different load current condition.

Voltage (V): 100 V/div, Current (A): 10 A/div, Time: 0.5 µs/div
(a) Load current $I_{Load} = 7.5$ A          (b) Load current $I_{Load} = 17$ A

Voltage (V): 100 V/div, Current (A): 20 A/div, Time: 0.5 µs/div
© Load current $I_{Load} = 28$ A               (d) Load current $I_{Load} = 37$ A

Fig. 3.16 Loss comparison between hard- and soft-switching choppers.

![Graph showing loss comparison between hard- and soft-switching choppers.](image)
Tab. 3-1 compares the calculated, simulated and experimental results for resonant branch peak current, $I_{\text{max}}$, and its conduction time, $2T_1 + T_2$, under different load current, $I_{\text{Load}}$, conditions. Although there are some minor differences due to negligence of parasitic and dissipative components, simulation and experimental results match well with the designed value in all different load conditions.

<table>
<thead>
<tr>
<th>Mode</th>
<th>$I_{\text{Load}}$ (A)</th>
<th>$I_{\text{max}}$ (A)</th>
<th>$2T_1 + T_2$ ($\mu$s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Calculation</td>
<td></td>
<td>53</td>
<td>2.3</td>
</tr>
<tr>
<td>Simulation</td>
<td>7.5</td>
<td>52</td>
<td>2.2</td>
</tr>
<tr>
<td>Experiment</td>
<td></td>
<td>50</td>
<td>2.4</td>
</tr>
<tr>
<td>Calculation</td>
<td></td>
<td>63</td>
<td>2.6</td>
</tr>
<tr>
<td>Simulation</td>
<td>17</td>
<td>62</td>
<td>2.5</td>
</tr>
<tr>
<td>Experiment</td>
<td></td>
<td>61</td>
<td>2.7</td>
</tr>
<tr>
<td>Calculation</td>
<td></td>
<td>73</td>
<td>2.9</td>
</tr>
<tr>
<td>Simulation</td>
<td>28</td>
<td>72</td>
<td>2.8</td>
</tr>
<tr>
<td>Experiment</td>
<td></td>
<td>71</td>
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<td>81.5</td>
<td>3.0</td>
</tr>
<tr>
<td>Experiment</td>
<td></td>
<td>81</td>
<td>3.2</td>
</tr>
</tbody>
</table>

3.1.4 Summary

In this section, the design criteria of a novel near-ZVT soft-switching chopper are presented with verification of both simulation and experimental results. The resonant tank impedance was found to be the most critical parameter for ZVT design and should be selected properly. A step-by-step design procedure was described with a practical example. The proposed simple fixed-timing control scheme is proven to be effective to achieve near-ZVT for a wide range of load conditions. The example soft-switching chopper also performs significantly better than its hard-switching counterpart in switching loss and $dv/dt$ reduction.

3.2 Load adaptive ZVT method utilizing diode reverse recovery current

Diode reverse recovery normally increases switching losses and produces noises in power electronics circuits. Over the past few decades, device manufacturers put a lot of effort to improve the
reverse recovery speed and softness by sacrificing the conduction voltage drop. With soft switching, the slowness of diode reverse recovery can turn into an advantage that helps extend the resonance to achieve true zero-voltage switching without initial current boost in resonant inductor. Although soft-switching inverters have been around for more than a decade, such a special feature has never been seriously discussed or implemented. The utilization of the slow diode is specially suited to those zero-voltage transition (ZVT) choppers and inverters because these soft-switching circuits turn on the anti-parallel diode before turning on the main switch thus totally eliminating the diode reverse recovery problem which is often a major headache of the hard switching inverters.

Last section proposed a load adaptive fixed timing control method which can realize near zero-voltage switching over a wide range current condition. Although this fixed timing control performs well with significant switching loss reduction, the device still turns on at a finite low voltage level that is objectionable in high power systems. The design has a restriction of high peak resonant current and can only achieve near-ZVT condition.

This section presents a novel zero voltage transition concepts that utilize diode reverse recovery current as a resonant inductor boosting current to achieve load adaptive zero-voltage operation. Unlike a conventional hard-switching inverter in which the slow diode needs to be avoided since its reverse recovery current adds into the opposite-side switch turn-on current and creates tremendous noises and losses, the utilization of slow diode in a ZVT soft-switching circuit along with the proposed design technique can incorporate the reverse recovery part of the diode current into resonance to achieve true zero-voltage switching and to avoid the switching noises and losses. The boosting current level can be controlled by proper selection of the diode and resonant inductance. The main switch does not need to carry extra boost current. Simulation and experimental results of a two-quadrant full bridge chopper have proven that the proposed method can achieve true zero voltage switching for the main device at all load current conditions.

3.2.1 Operation Principle

It is important to analyze the circuit behavior during the resonant stage to illustrate how the circuit can achieve the feature of load current adaptively. Fig. 3.17 shows a typical single-phase ZVT cell for resonant snubber inverter. To simplify the discussion, the load current direction is assumed in the indicated direction. The initial condition is the current flowing through $D_2$ and $D_3$. The control of the
auxiliary circuit is to help turn on $S_1$ and $S_4$ at zero-voltage condition. Fig. 3.18 shows a corresponding ZVT control waveforms with boosting current control. Main switches $S_2$ and $S_3$ are kept on when the resonant inductor current exceeds the load current. The boosting current level is controlled by the overlapping time of the main switch $S_2$, $S_3$ and auxiliary switches $S_{aux}$, which is the time interval from $t_1$ to $t_3$. To minimize resonant tank energy during the switch transition, it is desired that the boosting current, $I_{boost}$, be kept at a certain constant level. Since the time interval from $t_2$ to $t_1$ is load current dependent, the overlapping time of gate signals for $S_2$ and $S_{aux}$ have to be changed according to the amplitude of load current.

![Fig. 3.17 A typical RSI ZVT cell](image1)

![Fig. 3.18 Key waveforms of typical ZVT with extra current boosting](image2)
The key waveforms of the new proposed ZVT method are shown in Fig. 3.19. Now consider at time \( t_2 \) when inductor current is equal to the load current. If switches \( S_2 \) and \( S_3 \) are not keeping on, and the diode \( D_2 \) and \( D_3 \) are slow recovery diode, such as the body diode of MOSFET, then the reverse recovery current will serve as current booster that adds boost current into the resonant inductor from \( t_2 \) to \( t_3 \). Thus \( S_2 \) and \( S_3 \) are not necessary to conduct extra current for producing the boost current. The turn-off loss of \( S_2 \) and \( S_3 \) could be saved. The boosting current level here is determined by the reverse recovery current level of the slow diode \( D_2 \) and \( D_3 \).

Although the pre-charging time from \( t_1 \) to \( t_2 \) still depends on load current, the new control scheme can still achieve load current adaptively with simple fixed timing. The detailed illustration will be described in the next section.

Initially at time \( t_0 \), all switches are off, and the load current is freewheeling through \( D_2 \) and \( D_3 \) as shown in Fig. 4 (a-f). Operation modes for a complete cycle are described in detail as follows.

Mode a (\( t_0 - t_1 \)): Assume that the load current is positive when diode \( D_2 \) and \( D_3 \) are conducting, and the main switches \( S_1 \) and \( S_4 \) are off.
Mode b ($t_1 - t_2$): The auxiliary switch $S_{aux}$ turns on at $t_1$, the current in $L_r$ increases linearly and the current in diodes $D_2$ and $D_3$ decreases linearly. The auxiliary branch diverts the current from the freewheeling diode gradually.

Mode c ($t_2 - t_3$): After the auxiliary branch current is larger than the load current at $t_2$, slow diodes $D_2$ and $D_3$ keep conducting a reverse recovery current $I_{D2}$. The resonant inductance current keeps increased linearly until at time $t_3$, slow diode $D_2$ and $D_3$ are shut off. The main difference of utilizing a slow and a fast diode is the magnitude of $I_{D2}$. With an ultra fast reverse recovery diode, $I_{D2}$ is nearly zero, and the resonant inductor cannot be automatically boosted.

Mode d ($t_3 - t_4$): After $t_3$, four snubber capacitors resonate with the auxiliary inductor with an inductor over-boosting current equal to diode reverse recovery current level. The initial boosting current condition allows capacitor voltage discharged to zero at the end of the resonant stage at $t_4$.

Mode e ($t_4 - t_5$): When the voltage across the main device drops to zero at $t_4$ at the end of the resonant stage, the resonant inductor current is still larger than the load current at a certain level. Thus, the anti-parallel diode across the main device is forced to conduct the extra current. The resonant inductor current is then discharged linearly by the dc bus voltage. The main switch can be turned on under zero-voltage condition during ($t_4 - t_5$) before the inductor current drops to load current at $t_5$. During this mode, the voltage across the main device is clamped to zero.

Mode f ($t_5 - t_6$): Main devices $S_1$ and $S_4$ start to conduct load current gradually from $t_5$. The resonant inductor current keeps decreasing until time $t_6$, and the load current is then transferred to main devices $S_1$ and $S_4$ completely. There could be also reverse recovery current in $D_4$ and $D_1$ which will show up as an abrupt initial current in $S_1$ and $S_4$, which depends on how fast the main device body diode is. After $t_6$, the load current is completely taken over by the main switches $S_1$ and $S_4$. The auxiliary device $S_{aux}$ can be turned off under zero current condition.
3.2.2 Resonant Circuit Analysis

It is important to analyze the circuit behavior during the resonant stage to illustrate how the circuit can achieve the feature of load current adaptively. Fig. 3.21 shows the equivalent circuits during the resonant stage Fig. 3.20(d). $C_1^*$ can be regarded as $C_1$ flip down to DC negative bus. $C_4^*$ can be equivalent of $C_4$ flipped up to DC positive. $C_r^*$ and $L_r^*$ are the total equivalent resonant inductance and capacitance. In the case all the resonant capacitors have the same value, which is commonly used, we have $C_r^*$ equals to the capacitors across device.
The final equivalent circuit is a simple L-C resonant tank with resonant inductor of initial boosting current. Please note the equivalent resonant inductor current $I_{Lr}^*$ is the actual inductor current minus load current. It is important to emphasize that: 1) the equivalent resonant tank behavior is dependent on peak reverse recovery current $I_{boost}$ instead of the load current; 2) the equivalent resonant inductor $L_{r}^*$ initial current is determined by the negative peak current of the diode reverse recovery. During the resonant period $t_3-t_4$, the equivalent resonant capacitor voltage and inductor current can be derived as:

$$V_c(t) = V_c(1 - \cos \omega t) + \sin \omega t \cdot Z_r \cdot I_{boost}$$  \hspace{1cm} (3-11)

$$I_{Lr} = I_{Load} + \frac{V}{Z_r} \sin \omega t + I_{boost} \cos \omega t = I_{Lr}^* + I_{Load}$$  \hspace{1cm} (3-12)

Where,

$$\omega = 1/\sqrt{C_{r}^* \cdot L_{r}^*} \quad Z_r = \sqrt{L_{r}^* / C_{r}^*} \quad C_{r}^* = C_r / 2$$

Fig. 3.22 shows the state plane diagram of the resonant tank. Notice that the voltage of the equivalent capacitor is twice the voltage across the main switch.
It can be seen from Fig. 3.22 that the voltage of the capacitor across the top device will be clamped at the bus voltage from the end of the resonant stage \( t_4 \) until the inductor current drops to the load current at \( t_5 \). The main devices \( S_1 \) and \( S_4 \) can be turned on under zero-voltage condition at \( t_m \) during time interval from \( t_4 \) to \( t_5 \). This time period can be determined by the resonant tank design. Now if the fixed timing control is used, which means the time interval from \( t_1 \) to \( t_M \) is fixed, then the main switch will be turned on at different points from \( t_4 \) to \( t_5 \) corresponding to load current change. Under heavy load conditions, the main switch gate signal is applied near \( t_4 \), whereas under light load conditions, the main switch gate signal is applied near \( t_5 \). The maximum load current adaptive capability is determined by the time zone between \( t_4 \) to \( t_5 \), which can be determined by resonant tank design and diode reverse characters. This means the load adaptive feature can be achieved with simple fixed timing control by utilizing diode reverse recovery current.

The time interval from \( t_5 \) to \( t_4 \) can be expressed by the following equation:

\[
T_{\text{resonant}} = \arctan \left( \frac{V_s}{I_{\text{resonant}}} \right) \times \frac{T_r}{\pi} \tag{3-13}
\]

The boosting time from \( t_1 \) to \( t_3 \) is:

\[
T_{\text{boost}} = L_r \times \left( \frac{I_{\text{load}} + I_{r}}{V_s} \right) \tag{3-14}
\]

The discharging time from \( t_4 \) to \( t_5 \) can be written as:

\[
T_{\text{discharge}} = L_r \times \left( \frac{I_{r}}{V_s} \right) \tag{3-15}
\]

To ensure ZVT condition, the main switch should be turned on after resonant period but before the resonant inductor current be discharged to the load current level. Thus the criteria to achieve zero
voltage switching are to satisfy the follows equations under the desired load range. $T_{\text{pre}}$ is the leading
time of auxiliary gate from the main device gate signal.

\[ T_{\text{boost}} + T_{\text{resonant}} \leq T_{\text{pre}} \leq T_{\text{boost}} + T_{\text{resonant}} + T_{\text{discharge}} \]  \hspace{1cm} (3-16)

![Equation Image]

Fig. 3.23 Diode reverse recovery current under different load current and driving condition

Fig. 3.24 plots the curves of the above equation with a resonant inductor value of 0.5uH. The reverse recovery current is also changing according to value provided by manufacturer datasheet. The plot also considered the different diode reverse recovery current under different load condition, as shown from manufacturer datasheet in Fig. 3.23. The device used for plot is 1200V IGBT SKM300GB124D.

If fixed timing control is used, the proposed scheme can realize true ZVT at most of load conditions. If using $T_{\text{pre1}}$ as pre-charging time, then the system can achieve ZVT for load current between 25A to 100A. If $T_{\text{pre2}}$ is chosen as leading time, the proposed control can achieve true ZVT up to a load current of 75A. If an even larger region of ZVT is desired, then a variable pre-charging time control should be implemented. Leading of $T_{\text{pre2}}$ should be applied at light load and $T_{\text{pre1}}$ should be applied when the load current is beyond 75A. It can be seen from Fig. 3.24 that the ZVT could always be achieved for load current is under certain level.
3.2.3 Simulation and Experimental Results

Fig. 3.25 shows the key waveforms with PSPICE simulation using the designed parameter under load currents of 5 A, 15 A, and 35 A. The simulation results matches well with the design results and shows that the proposed fixed timing control scheme is very effective. In all load current conditions, the timing of auxiliary switch with respect to the main switches is not changed. However, the resonant current magnitude and the resonant period are automatically adjusted without variable timing control.
From switch voltage and current plots, there is no over-lapping between the switch current, $I_{sw}$, and voltage $V_{sw}$, and the zero-voltage switching is clearly achieved under all load current conditions.

Fig. 3.26 shows experiment waveforms of a full-bridge chopper with the proposed fixed timing ZVT method [G5]. The chopper is using CoolMoS™ device which has slow and snappy body diode. Since the CoolMOS™ have relatively larger reverse recovery current, the test chopper shows true ZVT at full range of load with simple fixed timing control.

![Resonant current $I_{lr}$ and switch voltage $V_{sw}$ under different load current conditions](image)

**Fig. 3.26** Experimental key waveforms of resonant current $I_{lr}$ (A) and switch voltage $V_{sw}$ (V) under different load current condition 5A, 20A, 40A (I: 20A/div, V: 100V/div)

Fig. 3.27 compares the simulation and experimental results with incorporation of parasitic lead inductance between device and power bus. Fig. 3.27 (a) shows the simulated key waveforms of the ZVT circuit. The simulation results with parasitic parameters match very well with the experimental waveforms in Fig. 3.27(b). Diode current $I_{d2}$ is also measured by inserting a resistor in series with the D2. There shows some parasitic ringing when the slow diode is turning off. The ringing amplitude is associated with device characters and lead inductance value. However, it does not affect the proper
operation of the ZVT circuit. There is also a small device voltage drop when the resonance begins, which is due to the forward voltage drop of diodes D2 and D3 and the inductor voltage drop as a result of the resonant current changes.

\[ I_{sw} + I_{d4} \]
\[ V_{sw} \]
\[ I_{load} \]
\[ I_{Lr} \]
\[ I_{d2} \]

Fig. 3.27 Comparison of the simulated and experimental results with parasitic components.

To further explore the application area of the proposed scheme. A two-quadrant chopper using IGBT device SKM300GB124D was also tested. The test results at 50A, 100A, and 125A load current are shown in Fig. 3.29. To measure the device current, a rogowski current probe is inserted. The layout parasitic inductance introduces results in some ringing on the current waveform.

Fig. 3.28 shows the key waveforms with PSPICE simulation using the designed parameter under load currents of 5 A, 30A, and 90 A. From switch voltage and current plots, there is no over-lapping between the switch current, \( I_{sw} \), and voltage \( V_{sw} \), and the zero-voltage switching is achieved under all load current conditions.
It can be seen from Fig. 3.29 that the circuit can achieve zero-voltage switching at a wide range of load current conditions, and the experimental results match the simulation results well except the high frequency ringing occurs in the experiments. The ringing should be minimized by a better circuit layout and the removal of the current sensing leads. The auxiliary switch leading time is optimized at normal current level, which is 100A. More ringing happens at heavy load and light load.

Fig. 3.29 Experimental key waveforms of resonant current $I_{Lr}$ (A) and switch voltage $V_{sw}$ (V) under different load current condition 50A, 100A, 125A (I: 50A/div, V: 100V/div)
Fig. 3.30 Losing ZVT when insufficient boosting current (I: 50A/div, V: 100V/div)

Fig. 3.30 shows a tested waveform which shows the case of losing zero voltage condition. As discussed in the last section, if the main device is turned on with too late, the voltage across the main device will swing back and ZVT condition is not achieved. There could be some current spike and ringing is significant due to large lead inductance. This figure also indicates that using a device with a slower body diode will have advantage of achieving larger load range of ZVT. One way to take advantage of that is to use externally connected diode with very low voltage drop can actually by pass the body diode and can reduce conduction loss. When there is little boosting current, the voltage cannot actually swing down to zero because of resistive loss in the resonant tank.

This section presents the concept of utilizing diode reverse recovery current as the boosting current for soft-switching operation. The analytical and simulation results have proved the viability of the proposed load adaptive schemes for ZVT operation utilizing the diode reverse recovery current. The proposed method can realize soft switching with load adaptive features by a simple fixed-timing approach. The boosting current level can be determined by selection of the diode characteristic and resonant circuit. The experimental results of a two-quadrant chopper prove the feasibility of the proposed approach. Although all the discussion is based on the chopper circuit, the concept can also be applied to other applications such as ARCP, RSI and coupled inductor for inverter operation.

Further work can be directed to justification of the use of the proposed fixed-timing based soft switching with benefits that are not fully discussed here. Potential benefits include the simplification of control, elimination or reduction of the resonant capacitor when using external slow diode as the main switch, reduction of the diode conduction voltage drop and its associated efficiency improvement, reduction of electromagnetic interference, and the overall cost saving.
3.3 A more generalized concept of load adaptive fixed timing control

Aiming to reduce the control complexity related to the variable timing control, one form of fixed timing control is described in [G7] to fix the advanced triggering time of auxiliary switches. However, the excessive current in the auxiliary inductor brings significant conduction loss and switching loss. Another attempt in simplifying soft-switching control was reported for the ARCP [C13]. Control simplification was also introduced for the ZVT inverter using coupled inductors. Although load current amplitude information is not required for auxiliary control signals, the zero voltage detection function of the gate driver is mandatory. This makes the gate drivers more difficult to design and possibly reduces the operation reliability. A new fixed timing control for RSI ZVT converters and ZVT inverters for coupled inductors is presented in [G17] and [G3]. The new timing control does not need any load current feedback. The control signals of the auxiliary devices are pre-defined during the timing design process. The purpose of this section is to find the common parts of the various ZVT inverter scheme and provide a more generalize load adaptive fixed timing control scheme for ZVT inverters. The theoretical analysis and design guidelines are presented in detail. Experimental results of a prototype inductor coupled ZVT inverter scheme with simple fixed timing control shows the proposed scheme.

3.3.1 A General ZVT commutation cell

The commutation circuit in one phase of the ZVT inverters is represented in Fig. 3.31. The voltage source $V_x$ is equivalently obtained by the circuit topology arrangement. The circuit was originally drawn in DC-DC cell based on inductor coupled scheme by Ivo Barbi [C17]. The realization of voltage source $V_x$ various for different ZVT topologies. Usually, $S_x$ is composed of one pair of switches, $S_{x1}$ and $S_{x2}$. $S_{x1}$ only allows the auxiliary current to be injected into the main inverter leg, and $S_{x2}$ enables the auxiliary current to flow out of the inverter leg. $V_x$ will needs to change polarity according to the auxiliary switch pair. The auxiliary switch $S_x$ remains off through most of one switching cycle; only turns on for load current commutation.

For example, in Hua’s original ZVT scheme [C14], $V_x$ is equal to zero; in the ARCP [D4], $V_x$ is half of $V_{dc}$, constructed from the midpoint of the capacitor bank or the power supply. In the ZVT inverter using coupled inductors with unity turns ratio [G13], $V_x$ equals $1/2V_{dc}$. In the $\Delta$-configured RSI [D12], the original control scheme results in $V_x=1/2V_{dc}$. For non-unity coupled inductor scheme
proposed by Ivo Barbi [C17] and improved by J. P. Gegner and C. Q. Lee [C18], $V_x$ is equal to a value less than half of the $V_{dc}$. In this section the focus will be on how fixed timing load adaptive ZVT can be achieved with proper timing and the assistant of $V_x$ as shown in Fig. 3.31.

For the convenience of explaining the control timing during the load current commutation, the load current is considered as constant during one switching cycle. Consider the original condition load current is flowing through diode $D_1$ and the auxiliary circuit is to generate an auxiliary current source to help turn on $S_2$ under zero voltage condition. Fig. 3.32 shows a timing diagram of a fixed timing controlled ZVT converter. Three timing parameters $T_{dly}$, $T_{d,off}$ and $T_x$ are the values needs to be determined by different control scheme. $S_{x1}$ represents the auxiliary switch, which enables the auxiliary current to flow into the inverter leg. $S_{x2}$ is the auxiliary switch, which builds the auxiliary current flowing out of the inverter leg.
As can be seen in Fig. 3.32 [G15], a suitable $T_{\text{dly}}$ can ensure $S_2$ turns on at zero voltage. $T_{\text{d.off}}$ has no impact when commutation is from diode $D_1$ to switch $S_2$. Fig. 3.32 also shows the commutation waveform when the load current flows out of the inverter leg. For the commutation from switch $S_2$ to diode, $T_{\text{d.off}}$ prevents the auxiliary circuit from building unnecessary current when the load is already sufficient to discharge resonant caps, as shown in heavy load case in Fig. 3.32. When the load current is not sufficiently large to charge capacitor voltage, auxiliary circuit will automatically activated at $t_5$ to complete the resonant and create the zero voltage turn on condition for switch $S_1$. If $T_{\text{dly}}$, $T_{\text{d.off}}$ and $T_x$ can be chosen as fixed value to accomplish ZVT condition at all load current, then the control scheme can be a very simple fixed timing control. It does not require any load current feedback and still guarantees ZVS operation. It is also noted that the auxiliary inductor current level is automatically adjusted to be adaptive to the instantaneous load current amplitude.

The key circuit operation could be divided by the following three stage:
The resonant stage is the key part to determine if zero voltage condition will be achieved. Fig. 3.33(b) could be further simplified by flipping $C_2$ to the DC rail similar as the approach in last section. The voltage source $V_x$ is expressed by $kV_{dc}$. The equivalent resonant capacitor value $C_x=C_1+C_2$. 

Fig. 3.33 Three key resonant stage of ZVT cell
Fig. 3.34 Simplified equivalent circuits during resonant stage.

The stage plane representation is a very convenient way to analysis the resonant stage operation. As shown in Fig. 3.35. The base values of the normalized state plane are $V_b=V_{dc}$ and $I_b=V_{dc}/Z$, where the characteristic impedance of the resonant circuit is $Z = \sqrt{L_x/C_x}$. Define $k_1=1-k$ is the normalized value of charging voltage source. The zero voltage condition will be meet only when $V_{Cx}$ reaches $V_{dc}$ and been clamped by diode $D_2$ for a certain amount of time.

As indicated in Fig. 3.35, when $V_x$ equals half of $V_{dc}$, $I_{boost}>0$ is a necessary condition to ensure ZVT condition. However, when $V_x$ is less than half of $V_{dc}$, which means $k<0.5$ or $k_1>0.5$, the $V_{Cx}$ can guaranteed reach to $V_{dc}$ even with $I_{boost}=0$. Therefore, no boost current is required to reach zero voltage turned on of bottom switch. This indicates that there is no need to control the advanced trigger time $T_{pre}$ by variable timing control. As long as a voltage source $V_x$ is introduced in the circuit with less than half of the DC voltage, the zero voltage condition can be achieved with fixed timing control. This is an great advantage for simplified timing control, the ZVT condition could be meet. No boost current and no extra turn-off of main switch is required.
The above analysis is valid for ZVS turn-on of bottom switch $S_2$ when the load current flows into the inverter leg. When load current flows out of the inverter leg, the equivalent circuit is shown in Fig. 3.36. Similarly, it is apparent that $I_{\text{boost}}$ is not needed when $V_x<V_{dc}$.

![Fig. 3.36 Simplified equivalent circuits during resonant stage for turn-on top switch.](image)

In summary, it is necessary that the auxiliary power source $V_x$ should be less than half of $V_{dc}$ and should change polarity when acting different auxiliary switches. In another way to describe, the charging source in the equivalent circuits of resonant stage should be larger than half of $V_{dc}$, the discharging voltage source should be less than half of $V_{dc}$. In this case, ZVT condition can be achieved with fixed timing control strategy.

### 3.3.2 A family of ZVT Inverter design with fixed timing control

The resulting motivation is to modify the existing ZVT circuits so that they satisfy the requirement of $k_1>0.5$ or in other word how to generate the extra voltage source $V_x$. Then the turn-off signal of the main device could be enabled prior to turning on corresponding auxiliary devices. By doing this, the resonance between the inductor and snubber capacitors always starts when the auxiliary current equals the load current. Therefore, the peak inductor current automatically adapts to the load current level.

Since most of three-phase ZVT inverters have individual auxiliary circuit designated for the corresponding leg, the illustration of soft-switching operation is based on one phase leg. The configuration of the ARCPI is shown in Fig. 3.37.
Fig. 3.37 ARCP phase leg and equivalent resonant stage circuit $V_x = 0.5V_{dc}$.

Fig. 3.38 Two internal points of power supply to get proper $V_x$

Since the midpoint of the input DC voltage is used, the auxiliary voltage source is half of $V_{dc}$. By introducing two internal voltage points of power supply or capacitor banks, a proper $V_x$ value can be easily realized, as shown in Fig. 3.39. The practical issue is to use an additional small converter to regulate voltage of the $V_p$ and $V_n$, as explained in [D31].

Fig. 3.39 shows the circuit diagram of the coupled inductor inverter phase leg and equivalent resonant circuit [G3]. It is found that by designing the turns ratio to be larger than one, the required $V_x$ can be obtained. The relationship between $k_1$ and $n$ is expressed in (3-40):

$$k_1 = \frac{n}{1 + n} \quad (3-40)$$
Another ZVT inverter using coupled inductors [D30] is shown in Fig. 3.40. The relationship between $k_1$ and $n$ is given by:

$$k_1 = \frac{n-1}{n}$$

(3-41)

The drawback for this method compare to previous one is the auxiliary switch will getting more current burden. The primary winding is conducting total current instead of partial current.

The single-phase $\Delta$-configured RSI is shown in Fig. 3.41. By synchronizing the switching of the diagonal main devices level under the original control scheme, half of $V_{dc}$ becomes the auxiliary voltage source. It is found that by introducing a time delay among the main device’s gate signals, $k_1=1$ can be equivalently obtained. The commutation waveform is shown in Fig. 3.42. Different from the other ZVT inverters, the resonant stage is divided into two Stages with the equal duration of $1/4T_r$. $T_{\text{discharge}}$ can be infinite because $I_{Lx}$ freewheels in Stage III. Therefore, the control timing can directly determined by the maximum load current condition.
The ZVS turn-on of the main devices is also realized at the light load of 10 A, as seen from Fig. 17(b). The auxiliary switches \( S_{x1} \) and \( S_{x2} \) turn off at zero current. Similarly, the amplitude of \( I_x \) is adjusted according to the load current level.

For simpler control implementation, \( T_{d,off} \) could also be set to zero. The difference would be whether both auxiliary circuits will be activated in each switching cycle. Fig. 3.43 shows the normalized stage plane trajectory of the resonant tank. For convenience, the resonant tank equivalent circuit is given on the left side. Fig. 3.44 gives the corresponding waveforms of resonant inductor current and resonant capacitor voltage. Assuming load current is going into the inverter. At \( t_0 \) current is freewheeling through top diode \( D_1 \). The bottom device \( S_2 \) is turned on under zero voltage condition at \( t_m \).
As shown in Fig. 3.42, with \( k_1 > 0.5 \), the voltage across \( S_1 \) is resonant to \( V_{dc} \), then it stays at \( V_{dc} \). After the current of \( L_x \) reduces to \( I_{load} \), \( V_{s2} \) starts to decrease again if \( S_2 \) is still not turned on. In order to turn on \( S_1 \) at zero voltage under any load current level, the suitable timing relationship between \( S_x \) and \( S_1 \) has to be determined. The detailed commutation waveform with \( k_1 > 0.5 \) is shown in. Referring to, there are four distinctive stages in the development of \( I_{Lx} \) and \( V_{s1} \), as follows. Note that \( V_{s1} = V_{dc} - V_{s2} \).

**[0, \( t_1 \]): Stage I, the inductor current linear charging period.**
The inductor current $I_{Lx}$ is linearly charged by $k_1 V_{dc}$ until it reaches the load current $I_{load}$. Thus, $I_{Lx}$ can be obtained by (3-17) and the duration of Stage I is given by (3-18). Diode reverse recovery current is omitted here for simple analysis.

$$I_{Lx}(t) = \frac{k_1 V_{dc}}{L_x} \cdot (t - t_0) \tag{3-17}$$

$$T_{sin} = t_1 - t_0 = \frac{L_x I_{load}}{k_1 V_{dc}} \tag{3-18}$$

$[t_1, t_2]$: Stage II, the resonance of inductor and capacitors.

Once $I_{Lx}$ equals to $I_{load}$, the snubber capacitors start resonance with the inductor $L_x$. Equations (3-19) and (3-20) gives the expression of $V_{Cx}$ and $I_{Lx}$, where $\omega$ is the angular frequency and $\omega = 1/\sqrt{L_x C_x}$.

$$v_c(t) = k_1 V_{dc} \left(1 - \cos(\omega (t - t_1))\right) \tag{3-19}$$

$$I_{Lx}(t) = \frac{k_1 V_{dc}}{Z} \sin(\omega (t - t_1)) + I_{load} \tag{3-20}$$

At $t_2$, voltage of $V_{Cx}$ reaches $V_{dc}$, which means voltage across $S_2$ drops to zero. Thus the duration of Stage II can be derived from (3-19), and is shown in (3-21).

$$T_{res} = t_2 - t_1 = \frac{\psi}{\omega} \tag{3-21}$$

where:

$$\psi = a r \cos\left(\frac{k_1 - 1}{k_1}\right) \tag{3-22}$$

Then, at the end of resonance, resonant inductor current $I_{Lx \_rend}$ can be easily found in (3-23).

$$I_{Lx \_rend}(t) = I_{Lx}(t_2) = \frac{k_1 V_{dc}}{Z} \sin \psi + I_{load} \tag{3-23}$$

$[t_2, t_3]$: Stage III, discharging period.

During this stage, the voltage of $S_2$ remains at zero due to conduction of $D_2$. $I_{Lx}$ decreases linearly and is obtained in (3-24).
Clearly, the discharging rate of the inductor current is smaller than the charging rate in Stage I. Until \( I_{Lx} \) reaches \( I_{load} \) at \( t_3 \), \( V_{s2} \) stays at zero. Substituting \( I_{Lx\_rend} \), \( \omega \) and \( Z \) into (3-23), the duration of the zero voltage period is derived in (3-24).

\[
T_{\text{discharge}} = t_3 - t_2 = \frac{\sqrt{2k_i - 1}}{1 - k_i} \sqrt{L_s C_x}
\]

(3-25)

Since the natural resonant period of the auxiliary inductor and snubber capacitors is \( T_r = 2\pi \sqrt{L_s C_x} \), (3-25) can be rewritten by:

\[
T_{\text{discharge}} = t_3 - t_2 = \frac{1}{2\pi} \frac{\sqrt{2k_i - 1}}{1 - k_i} T_r
\]

(3-26)

The objective of the desired fixed timing control is to find suitable delay time, \( T_{dly} \), between the turn-on of \( S_x \) and \( S_2 \) so that \( S_2 \) always turns on in Stage III to achieve zero voltage turn on condition. Therefore, the following relationship needs to be satisfied at any load current:

\[
T_{Lin\_any} + T_{res} \leq T_{dly} \leq T_{Lin\_any} + T_{res} + T_{\text{discharge}}
\]

(3-27)

From (3-21) and (3-26), it is known that only \( T_{Lin} \) is dependent on the load current among \( T_{Lin} \), \( T_{res} \) and \( T_{discharge} \). The longest \( T_{Lin} \) happens at the peak load current. If \( T_{\text{discharge}} \) is designed longer than \( T_{Lin} \) at the peak load current, then a fixed \( T_{dly} \) value can be found to satisfy (3-27) for any load current. As a result, \( k_1 \) can be designed according to (3-28) and is rewritten in normalized format by (3-29), where \( I_p \) is the maximum load current and \( I_b \) is the base current which equals to \( V_{dc}/Z_0 \).

\[
T_{\text{discharge}} = \frac{1}{2\pi} \frac{\sqrt{2k_i - 1}}{1 - k_i} T_r \geq T_{Lin\_max} = \frac{L_s I_p}{k_i V_{dc}}
\]

(3-28)

\[
\frac{2k_i \sqrt{2k_i - 1}}{1 - k_i} \geq \frac{I_p}{I_b}, \text{ or } \frac{2k_i \sqrt{2k_i - 1}}{1 - k_i} \geq \frac{I_p}{I_b}
\]

(3-29)
Fig. 3.45 shows the normalized maximum capable current to achieve zero voltage with the change of $k_1$. Increase $k_1$ (which in equivalent to increase turns ratio in coupled inductor scheme) or decrease resonant tank impedance will get a wider load adaptive region. Please note that the current base value is $V_{dc}/Z_r$ where $Z_r = \sqrt{L_s/C_s}$ is the equivalent resonant tank impedance.

![Graph showing normalized maximum load current vs k1](image)

Fig. 3.45 Normalized maximum load current $\bar{T}_p$ to achieve fixed timing ZVT in related to $k_1$

### 3.3.4 Verification of fixed timing control with inductor coupling ZVT scheme

To further verify the proposed control scheme, a 120-kW soft-switching inverter is designed with load adaptive fixed timing coupled inductor ZVT scheme. Fig. 3.46 shows the single-phase coupled magnetic inverter cell and its basic control timing diagram. The coupled magnetic windings have a non-unity turns ratio to increase the zero-voltage range [G3]. A saturable reactor $L_{sr}$ is added to reduce the reverse recovery current, which occurs when the resonant current ($I_{lez}$) swings down to zero condition. Notice in Fig. 3.46 (b), there are only two timing clocks that need to be determined: (1) dead time $T_{dt}$ and (2) delay time $T_{dlv}$. The dead time is needed for all the voltage source inverters to avoid shoot-through. In the proposed design, both main and auxiliary switches use the same dead time to simplify the control circuit. The delay time is the time that main switches turn on and off with a delay following the pulse-width-modulation (PWM) command. The auxiliary switches follow the PWM command without any delay, but the main switches simply delay a fixed $T_{dlv}$ to achieve zero-voltage turn-on. The typical voltage and current waveforms during the resonant period is already given in Fig. 3.32. The simple rule is to have $T_{dt}$ long enough to avoid shoot through and unnecessary conduct of auxiliary
branch when load current is high enough to discharge the cap and $T_{dly}$ long enough to ensure the switch reaches zero-voltage condition before it is gated on. The circuits for $T_{dly}$ could be simple passive delay with few logic gates. Compared to the complicated and costly CPLD variable timing control circuits shown in Fig. 2.26 in Chapter 2, the new approach is much simpler and easier to tune.

Fig. 3.46 Single-phase circuit for inductor coupled ZVT inverter and its control timing

Fig. 3.47 shows the simulation results of the coupled inductor inverter scheme proposed in paper [G3]. The circuit parameters used for simulation: $V_{dc}=640V$, $I_{load}=150A$ (rms), $L_1=1.6\mu H$, $n=1.25$, $k=0.55$, $C_1=C_2=0.14\mu F$, $T_{dly}=1.5\mu s$, $T_{d_{off}}=1\mu s$. By introducing a small dead-time $T_{d_{off}}$, the auxiliary circuit is not acting when natural commutation can be achieved. Around the zero-crossing of the load current, both auxiliary branches are activated and conduction smaller amount of current. The resonant inductor current adapt quite well with load current. $I_{Lr}$ is the total resonant branch current going out of the inverter switch node. $V_{sw}$ and $I_{sw}$ is the bottom switch voltage and current. Fig. 3.47 (b) shows the zoomed in waveforms of the resonant current $I_{Lr}$, switch node voltage and bottom switch current. It is very clear shown that zero voltage condition is achieved at the whole line cycle with minimized circulation current in the auxiliary branch. There is no overshoot in the device current thus the turn-on switching less could be largely eliminated. The resonant peak current is adapted to the load current and all this is achieved with a very simple fixed timing control timing scheme shown in Fig. 3.46.
Fig. 3.48 shows the photograph of a 120-kW soft-switching inverter prototype. The main devices EUPEC FF400R12KE3TM are rated 400A, 1200V, and the auxiliary devices EUPEC FS150R12KE3TM are rated 150A, 1200V. Although the auxiliary devices can be much smaller, their
voltage drop may be too high to trip under de-saturation condition. Because the design is to retrofit a 75-kW hard-switched inverter, the layout needs to be extremely compact, and the heat sink needs to be liquid cooled. A simple delay circuit is built-in in the main gate driver circuit board. The implementation is only a simple RC circuit along with Schmitt trigger logic gates, and thus there is no cost penalty on the control circuitry. The major added bulky components are the coupled magnetic, which sit on top of the entire inverter. With a proper design to minimize the magnetizing current and the use of Litz wire, the coupled magnetic components do not experience any over temperatures.

Fig. 3.39 shows the experimental device voltage, load current and resonant current waveforms at a reduced power condition for one phase leg to prove the concept. The switching frequency in this case is 15-kHz, and the line frequency is 400 Hz. The circuit operates smoothly without any glitches or unusual overshoot. The resonant current increases as a function of the load current, which agrees with the analytical results that the resonance occurs after the auxiliary current exceeds the load current. Because of the layout difficulties, the bottom device gate is monitored instead of switch current. It can be observed from Fig. 3.39 (b), the device voltage $V_{sw}$ comes down to zero first, and the gate voltage $V_g$ arises after $V_{sw}$ is totally dropped to zero. This timing sequence indicates that the device current and voltage do not overlap thus zero voltage turn on condition is achieved under all the load current condition.
Fig. 3.49 Experimental key waveforms of ZVT inverter with simple fixed timing control
Efficiency test is performed to compare the proposed ZVT inverter with a standard hard switching inverter. The load is just an inductor thus the inverter loss can be obtained by subtract the total DC input power by the output active power of the inductive load. The obtained inverter loss will thus count in all the extra magnetic and auxiliary circuit loss. Fig. 3.50 shows the soft switched inverter can achieve up to 50% loss reduction compared to hard switching inverter depends on load condition. Soft switching appears to significantly reduce the switching losses for both turn-on and -off conditions, but the added resonant inductors and auxiliary switches introduce additional losses, which tend to offset the efficiency gain and need to be minimized by tightly selected resonant inductance and delay timing.

![Inverter total loss comparison under hard switching and soft switching condition](image)

Fig. 3.50 Inverter total loss comparison under hard switching and soft switching condition

**Summary:**

The new fixed timing control concept for ZVT inverters is generalized in this chapter. Among the three approach introduced, the coupled inductor based scheme naturally satisfy the requirement of alternative voltage source Vx. The theoretical analysis, simulation results and experimental tests show that the proposed fixed timing control realizes the true ZVS turn-on and snubber assisted turn-off of main devices without any instantaneous load current information. With greatly simplified soft-switching control and improved performance, soft switching inverters with fixed timing control will eventually show promising future compared to hard switching inverter.
Chapter 4 Driver based soft switching technique for SiC BJT

This chapter first presents the base driver design for silicon carbide bipolar junction transistors (SiC BJT). A new MOSFET driven transistor base driver scheme is proposed to successfully drive the first reported 7.5HP SiC BJT inverter [G16]. A new driver based zero-voltage-switching BJT scheme is then proposed based on the fixed timing control concept developed from the previous chapters. The proposed scheme cleared two major obstacles for applications of power SiC BJT: complicated based driver design and potential high stress that causing device breakdown.

4.1 Base driver design of hard-switched SiC BJT inverter

Si materials have been used dominantly in power electronics industry for decades, especially for lower power and low voltage applications. For high-power, high-temperature applications, wide band gap materials will be more favorable. It is widely accepted that SiC would be the most promising materials to replace silicon in the future. Among many polytypes of SiC, 4H-SiC and 6H-SiC is the only commercially available at present time. 4H-SiC is more preferred for power devices with higher carrier mobility and low dopant ionization energy [B2][B3]. The higher break down field will allow SiC device 10 times less thickness of the drifting layer than silicon based device. Moreover, the thermal conductivity is three times higher than Si which will allow much less cooling requirement for SiC devices. The power density of SiC based power converter potentially could be much more higher than Si based converters [B4][B5].

Although all the advantages of silicon carbide materials, the application of SiC based power device is still at immature stage. The difficulties lies in mostly in the material processing, higher crystal defects and very low yield compare to silicon based power devices. However, there are several company already have commercially available SiC diodes and is been reported used successfully in PFC applications [E15]. There has been reported work on SiC IGBT and GTO. More work is focused on the development of VJFET, MOSFET and BJTs. Unlike MOS-based SiC power device, SiC BJT has the advantage of being free of gate oxide. In addition, potentially lower forward voltage drop and higher current density make BJT more attractive over MOSFET for high power high temperature applications. Furthermore, the simple structure makes it more feasible to process a higher power SiC BJT at present time. The reported 4H-SiC BJT have a higher power rating of 600V and 50A [G19].
However, unlike MOSFET and IGBT, BJT is a current driven device. A proper current source should be provided in proportional to the collector current to ensure safety operation and reduce device on-state voltage drop. However, to achieve a faster turn-off speed, the device should not be driven into deep saturation region. Although Si power BJT has been introduced for several decades, an efficient and effective driving method is still remain a big challenge.

To properly switch the BJT device, a sufficient high pulse base current should be provided during turn on to minimizing the delay time and turn on switching losses. Then a base current needs to be maintained in proportional to the collector current to ensure safety operation and reduce device on-state voltage drop. To achieve a faster turn-off speed, the device should avoid getting into deep saturation region and a negative base current is needed.

4.1.1 Basic property of SiC BJT and review of previous work

Fig. 4.1 shows a section of the cross sectional view of the proposed BJT structure. The base-collector junction is terminated by multi-step junction termination extension (MJTE) to improve blocking capability.

![Cross-sectional view of SiC BJT structure by Rutgers](image)

Fig. 4.1 Cross-sectional view of SiC BJT structure by Rutgers

The forward I-V characterization of the packaged 4H-SiC BJTs is tested using Tektronix 370A with 200mA step base current change. The SiC BJT is fabricated by Rutgers University with Cree’s SiC wafer. Fig. 4.2 shows the comparison of forward I-V curves between SiC BJT and a FJL6825 manufactured by Fairchild semiconductor. The BJT is measured up to a collector current of 10A at base current of 1.4 A, corresponding to a common emitter current gain of 7. Poor sidewall passivation
and surface recombination contribute to the first 2V drop even with minimum current gain. An extra base current of about 0.4A is needed to overcome the surface recombination in order to drive the 1st generation SiC BJT. The 2nd generation SiC BJT has almost eliminated the 2V voltage drop. Low carrier diffusion length in base region and low conduction modulation in the drift region may partly contribute to the large voltage drop at high current (Ic=10A with VCE =7V). With improved contact of P+ region and base, the forward voltage drop could be further reduced. Devices with smaller cell pitch sizes will be fabricated and investigated by Rutgers but is not covered by the scope of this work. Fig. 4.3 and Fig. 4.4 shows the third and four generation of SiC BJT have much lower forward voltage drop.

![Graph](image)

(a) Si BJT (Fairchild FJL6825)

![Graph](image)

(b) 1st and 2nd generation SiC BJT (Rutgers)

Fig. 4.2 Si and SiC BJT forward Ic-Vce characters
Fig. 4.3 Third generation SiC BJT measured IV curve (Rutgers)

(a) 4H-SiC I-V characteristics at 25 C    (b) 4H-SiC I-V characteristics at 150 C

Fig. 4.4 Fourth generation SiC BJT measured IV curve (Rutgers)

(a) 4H-SiC I-V characteristics at 25 C    (b) 4H-SiC I-V characteristics at 150 C

Fig. 4.5 shows a detailed vision of an opened SiC BJT package. The SiC BJT device is formed by multiple individual small BJT cells connected in parallel mode. The gold plated case is connected as common collector. The overall blocking capability will be the weakest BJT cell that blocks the lower voltage. The tested device can block at above 600V for multi-cell package.
The optimal point to drive BJT is the place when further increase base current will not help decrease $V_{ce}$ with certain $I_c$. As indicated in Fig. 4.2 at the near saturation point A. For Darlington driven transistor, the actual balanced point will be somewhere in point B because of extra voltage drop.

One of the conventional ways to drive BJT is using totem pole output arrangement. A negative power source is also necessary to get a reverse base current for faster turn off. Although an anti-saturation clamp circuit can be used to limit the excess current, the power loss with this type of circuit is still very significant especially when driving high power SiC BJT with high $V_{be}$ drop and low beta value. Fig. 4.6 shows the switching waveforms of SiC BJT with conventional totem pole variable voltage source.

A small resistor is connected in serial with base to limit base current. It can be seen that for SiC BJT, turn on loss is dominant and turn off delay time of SiC BJT is very short. The turn off negative gate voltage is $-3.5\text{v}$ and turn on voltage is $10\text{V}$. When the load current increases, the turn on gate
voltage needs to be increased accordingly to optimally drive the BJT. This is done manually by device
tester but it’s to implement dynamically. The power dissipation on driver circuit is significant due to
the high $V_{be}$ voltage drop and lower gain for SiC power BJT.

A transformer coupled proportional base drive circuit can provide a better performance but tends
to be saturated at lower operation frequency [B13]. For conventional current source type base drive
methods, a complicated gate drive circuitry with current feedback is essential to proportionally drive
BJT [B11]. Darlington transistor can have the capability of adjusting the base current according to the
change of collector current. With the use of MOSFET to replace the driver transistor, the MOS gated
transistor can be driven with a simple voltage source. Fig. 4.7(a) shows a emitter open transistor with
FET Darlington structure [B24][B22]. Although the MOSFET in series with transistor only need to
block low voltage, the extra conduction loss introduced is a major draw back of this approach. Fig.
4.7(b) shows a typical MOS-Darlington cascade configuration [A10]. With the help of diode, the
device can be turned off faster if the gate drive can provide a large reverse current spike. Paper [B7]
introduced a circuit using MOS-Gated Bipolar Transistor (MGT) structure to drive SiC BJT with two
Si N-MOSFET. A high voltage blocking MOSFET is needed. Two N-FETs need separate gate signals
thus increased complexity of driver circuits.

![Fig. 4.7 MOSFET Gated BJT structure](image)

(a) FGT emitter-open transistor   (b) FET Darlington   (c) Dual FET gated SiC transistor

4.1.2 Proposed Hard-switched IGBT/FET gated transistor

To simplify the FET gated SiC transistor method, a new base drive consists of one Si IGBT and
one Si P-MOSFET in “reversed totem pole” style is proposed to drive SiC BJT transistor. Fig. 4.8
shows the proposed IMGT driver structure with one high voltage IGBT and one low voltage P-channel MOSFET.

Instead of using conventional proportional current driven method for optimal driving bipolar transistor, the proposed base drive method can adaptively drive SiC BJT at a quasi-saturation condition based on voltage balance of $V_{be}$ and $V_{ce}$ as similar in Darlington transistor. Turn off of SiC BJT is realized by turn on the P-FET thus short the base emitter of BJT. The IGBT needs to block full bus voltage. The use of IGBT is to avoid the slow body diode of MOSFET that may cause large diode reverse recovery current for inverter application. By turning on IGBT G1, the base current is feeding into BJT very quickly thus the BJT can be turned on promptly. Noticed the following voltage balance equation should be satisfied:

$$V_{ce_{-BJT}} = V_{ce_{-IGBT}} + V_{be_{-BJT}}$$

(4-1)

From the equation (4-1), it can be seen that the voltage drop between collector and emitter of BJT is actually followed that of the IGBT. The turn-on speed of BJT is then determined by the turn-on speed of IGBT. The BJT turn-on speed can then be adjusted by selecting a proper IGBT device and its gate resistor. In practical, a small saturable core is inserted between collector of IGBT and BJT. The saturable core could reduce the turn-on loss in IGBT and reduce the diode reverse recovery problem for inverter application.
The P-FET is introduced to speed up turn off of BJT. By shorting base to the emitter by turning on the P-FET $G_2$, a low impedance path is formed between base and emitter of the BJT. This will help remove the charge from the base region thus turn off the BJT device quickly.

Consider if there is a sudden increase in the collector current, then the voltage drop of $V_{ce_BJT}$ will increase. This will result in the increase of $V_{ce_IBJT}$ and thus the increase of base current of BJT $I_b$. Thus the proposed driver structure will automatically adjust the base current according to the collector current. The operation point of the device is determined by voltage balance condition presented in equation (4-1).

A new IGBT and MOSFET Gated Transistor (IMGT) base drive structure is proposed for high power SiC BJT. The proposed base drive method can adaptively drive SiC BJT at an optimal condition based on voltage balance control of $V_{be}$ and $V_{ce}$. The whole IGMT structure could be regarded as a new “improved” BJT device, which can be easily driven by a voltage source gate driver. The proposed IMGT driver circuit is much simple in compare to the conventional current source base driver but with much improved switching characters. The SiC BJT is tested with half bridge inverter successfully at 400V 25A condition.

However, the conduction voltage drop on the current-version SiC BJT is still quite high and need further work to be reduced. Compensated voltage source will help alleviate the voltage drop problem but actually implementation of DC voltage source still needs further research.

4.1.3 Demonstration of the first 7.5HP SiC BJT inverter with the proposed base driver

The proposed base drive is tested by pulse testing for both Si and SiC BJT. Fig. 4.9 shows the experimental switching waveforms of the proposed base driver.
Fig. 4.9 Si BJT and SiC BJT pulse testing waveforms with the proposed driver.
The proposed IMGT base drive is used to implement a 7.5HP SiC and Si BJT inverter. Fig. 4.10 shows the overall inverter structure. As shown in Fig. 4.11, the inverter phase leg is constructed with three parts: voltage source gate driver, Si base driver circuitry and SiC BJT power stages. The voltage source gate driver is designed as a regular IGBT driver except the voltage level need to be increased a little to fit the needs for driving SiC BJT. An IGBT can be also put in the place of N-FET for inverter
operations. A saturable inductor is inserted in between the transistor collector and N-FET to limit the rising rate of the base current as well as reduce the turn-on switching loss on the N-FET.

Fig. 4.12 shows the actual board connection of the three-layer structure. The voltage source gate driver board is connected to the base driver board with snap in connectors. This can minimize the unnecessary gate driver parasitic inductance and is easy for assembly. The function of the base driver board is to provide necessary base current to properly drive the transistors. The transistors are surface mounted on an IMS (insulated metal substrate) board. As shown in Fig. 4.13, the power stage board is connected to the base driver board with fifteen brass hex stands. The hex brass stands can also served as a thermal barrier if the SiC inverter needs to be operated at elevated temperature. With the designed three layer structure, the operation of Si and SiC inverter can be easily performed by changed only the BJT power stage boards. If a new type of base driver is needed, the base driver board can be changed to accommodate any special needs without modify the other parts. The overall inverter structure is flexible and easy for reassembly.
Fig. 4.13 SiC BJT and Diode stage on an IMS board with brass stand-off

Fig. 4.14 shows the fully assembled SiC inverter with current sensing resistor. The IMS board with SiC power device can be mounted on a heat sink or a temperature controlled hot plate for high temperature operation test. Three high frequency capacitors is also added to absorb high frequency ripple current thus to reduce voltage spike over the device. The IMS board has Aluminum substrate with 4Oz copper on top. The insulation material is good in heat conduction. The IMS board can handle up to 300 degree C temperature for a short time.

Fig. 4.14 Fully assembled SiC BJT inverter.
A demonstration SiC BJT inverter is built to drive a 7.5HP induction motor at the Future Energy Electronics Center in Virginia Tech. This is by far the first SiC BJT inverter demonstrated to drive an induction motor at this power level. A Si BJT inverter is also built for verification purpose. The Si BJT used is FJL6825 from Fairchild. The power rating for Si and SiC are similar and should be able to handle total power of more than 7.5HP. The base driver power device: NFET and PFET needs to handle large peak current (as high as 40A) for a short period of time. However, the average current is very low. The use of way over rated device is to ensure safer operation of the SiC BJT.

Fig. 4.15 shows the experimental waveforms of the SiC BJT inverter. A modified SVPWM scheme is used so that the phase with maximum current is not taking switching action. The SiC BJT inverter is tested at 20kHz switching frequency. \( I_e \) is the emitter current of the BJT and \( I_{\text{diode}} \) is the anti-parallel discrete SiC diode current.
The efficiency of the SiC BJT inverter and Si BJT inverter is evaluated with a 7.5HP motor running with a dynamometer. The efficiency and heat sink temperature rise for SiC and Si BJT inverter is shown in Fig. 4.16 and Fig. 4.17. The SiC inverter efficiency is about 2% lower than that of the Si
BJT inverter mainly because of higher voltage drop. The inverter efficiency tends to be reduced at higher switching frequencies and higher temperature rise. The temperature effect is significant because higher temperature will cause higher voltage drop and further lowed the efficiency. This could cause significant thermal problem if the power stage is not cooled sufficiently. The SiC BJT needs to further reduce forward voltage drop in order to make it more attractive for inverter operation. Compensated Darlington method could also be used to reduce the conduction voltage drop. The difference is less significant with higher DC bus voltage.

![SiC BJT inverter Test, 20Khz efficiency and Temperature rise](image1)

**Fig. 4.16 SiC BJT inverter efficiency and Temperature rise**

![Si BJT inverter 330V bus, 10KHz switching efficiency and Temperature rise](image2)

**Fig. 4.17 Si BJT inverter efficiency and temperature rise**

### 4.2 Driver based SiC soft switching BJT with load current adaptively

There are two major limitation of using power BJT. The first limitation is high base current requirement due to low current gain. The second limitation of using BJT is the second break down
problem which prevent the device from being used toward its full capability. The devices have to be degraded to get less chance of second break down. In the last section, an IGBT and MOSFET Gated Transistor (IMGt) base driver is proposed. The IGBT and P-FET is complementary turn-on with the same gate signal. This base driver provides base current by MOS-Darlington structure at the expense of increased forward voltage drop. However, the BJT still subject to high voltage and high current at switching transition. In this section, a new scheme is proposed to resolve the second major problem of BJT by turn-on SiC BJT under zero voltage condition and turn-off with lossless snubber. Only a slight modification of the previously proposed hard-switched base driver is needed.

4.2.1 Basic Principle of soft switched base driver design for BJT

Since there are already extra switches in the base driver, it is possible to further utilize the driver switch to serve more function. The basic idea for the new scheme is to use the base driver device (G1 and G2 in Fig. 4.8) as auxiliary switch to realize zero voltage switching. Instead of complimentary turn-on the switch G1 and G2, a certain overlapping period is introduced to produce the resonant current path. As illustrated in Fig. 4.18, by adding one resonant inductor and capacitor to the previously proposed IGBT and MOSFET gated base driver (IMGt), the overall structure is similar to that of a basic ZVT cell in Fig. 1.21.

![Comparison of a typical ZVT cell and the proposed IMGT cell for base driver.](image)

If the P-FET is kept on for a short time when IGBT is on, then a resonant current path is formed to divert current and always turn on the anti parallel diode of BJT. The basic operation of resonance is the same as that the ZVT cell Fig. 1.21. Thus the IGBT and MOSFET driver switches can be utilized to provide soft-transition of BJT besides provide base current during on state. Fig. 4.20 shows the proposed soft switching base driver. For the convenience of later description, the soft switch base driver structure in Fig. 4.19 is named as “Soft Switch Bipolar Junction Transistor”, or SSBJT.
The proposed scheme is particularly good for use with SiC BJT because the turn-on loss is much higher compared to turn-off loss of SiC BJT, as shown in Fig. 4.20. A ZVT scheme will be very appropriate to use since turn-on loss is almost eliminated but turn-off loss is only reduced with snubber capacitors. Besides, SiC BJT demonstrates much shorter charge recombination time in comparing to that of Si BJT. The device can turn-off just by shorting the emitter and base.

The delay circuit could be as simple as a passive delay network such as LCD delay. Fig. 4.21 shows one implementation example and test waveforms for the delay circuit. One small core is used to block voltage for a short time for turn on delay timing.
Fig. 4.21 A simple passive delay circuit for gate delay

Fig. 4.22 soft switching driver operation key waveforms and resonant tank state plane trajectory.

Fig. 4.22 shows the basic operation key waveforms of the proposed soft switching scheme. The basic cell is plug in a simple device testing circuits shown in Fig. 4.23(a).
Initially at time $t_0$, IGBT are off, and the load current is freewheeling through $D_2$. The operation modes for a complete switching cycle are described in details as follow:

Mode a ($t_0 - t_1$): Assume that the load current is positive when diode $D_2$ is conducting, and the main BJT is off with the MOSFET is kept on.

Mode b1 ($t_1 - t_2$): The IGBT gate is applied on at $t_1$, the current in $L_r$ increases linearly and the current in diodes $D_2$ decreases linearly accordingly. MOSFET is still kept on with the present of delay circuits. The auxiliary branch diverts the current from the freewheeling diode $D_2$ gradually. The charging slop is determined by bus voltage and the inductance.

Mode b2 ($t_2 - t_3$): The auxiliary branch current is larger than the load current $I_{load}$ at $t_2$. Diode $D_2$ keeps conducting a reverse recovery current $I_{d2}$. The resonant inductor current increases linearly until at time $t_3$, diode $D_2$ is cut off. The major difference of a slow or a fast freewheeling diode is the magnitude of $I_{d2}$.

Mode c ($t_3 - t_4$): After $t_3$, two snubber capacitors resonate with the auxiliary inductor with an inductor over-boosting current equal to diode reverse recovery current $I_{rr}$. The initial boosting current condition allows capacitor voltage discharged to zero at the end of the resonant stage at $t_4$.

Mode d ($t_4 - t_5$): When the voltage across the main device drops to zero at $t_4$ at the end of the resonant stage, the resonant inductor current is still larger than the load current at a certain level. Thus, the anti-parallel diode across the main BJT device is forced to conduct the extra current. As indicated by current loop $L_2$ on Fig. 8.(d). Similarly, current will have a path through the base-collector PN junction of BJT on loop $L_1$ as in Fig. 8.(d). However, the interconnection inductance between BJT base and emitter of IGBT will be capable of block the current flowing in loop $L_1$. Most current will go through diode $D_1$ in current loop $L_2$. The loop $L_1$ current is build up gradually with the voltage drop on MOSFET applied forward bias the base-collector junction of the BJT. During this mode, the BJT voltage is clamped to negative when diode $D_1$ is conducting.

Mode e ($t_5 - t_6$): MOSFET is turned off at $t_5$. MOSFET current is shifted quickly to BJT base. The BJT emitter current $I_{BJT-E}$ builds up to load current accordingly. The resonant inductor current $I_{Lr}$ keeps decreasing. The excess part of base current $I_B$ over load current will flow through loop $L_1$. $D_1$ current
drops to zero at $t_6$. The resonant inductor current is discharged partially by voltage drop across IGBT and MOSFET voltage during MOSFET turn off.

Fig. 4.23 Operation Stages of the proposed SSBJT scheme
Mode f \((t_5 - t_6)\): The resonant inductor current is further discharged gradually by voltage drop across IGBT and \(V_{bc}\) drop of BJT when base current is still in exceed of the steady state value. The base current is kept reducing until the device is driven into steady state when voltage balance of IGBT and BJT is achieved. At this point, the base-collector junction is reverse biased. The IGBT and BJT is action exactly like a Darlington structure.

Mode g \((t_7 - t_8)\): At \(t_7\), IGBT is turned off and MOSFET is turned on simultaneously. The IGBT needs to cut a small amount of steady state base current. MOSFET is turned on under near zero voltage condition. A low impedance path formed by MOSFET helps cut off the BJT. The turn off loss is reduced with snubber capacitors across the main BJT switch. According to the above analysis, the base driver will always be able to achieve zero voltage condition for the main BJT because the auxiliary power source \(V_x\) source is equals to zero. The main switch BJT can be guaranteed turned on with zero voltage transition with all load current condition because diode \(D_1\) will kept conducting until MOSFET is turned off at \(t_5\). The resonant peak current will be determined resonant tank impedance and diode reverse recovery current [G5]. From Fig. 4.22, the resonant peak current is approximately:

\[
I_{\text{peak}} = I_{\text{boost}} + I_{\text{Load}} + \frac{V_{\text{dc}}}{Z}
\]  

(4-1)

In equation (4-1), \(I_{\text{boost}}\) is equal to peak diode reverse recovery current. \(Z\) is resonant tank impedance.

### 4.2.2 Simulation and experimental results for the proposed soft switching base driver

The basic operation of soft switched base driver is verified by simulation based on Si BJT model FJL6825 provided by Fairchild. Fig. 4.24 shows the proposed scheme can achieve zero voltage switching of BJT under different load current condition. A simple fixed delay circuit can cover the requirement of ZVT under all load current condition.
Experimental test has been done to further validate the soft switching base driver concept. Fig. 4.26 shows the voltage $V_{ce}$, base current $I_b$ and emitter current $I_e$ waveforms with the proposed SS-IMGMT base drive for both Si and SiC BJT. The charge recombination time of SiC BJT, however, is significantly smaller than that of Si BJT.

Fig. 4.25 Si BJT switching waveform: turn on: 0.14mJ turn off: 0.2mJ (2us/div)
Fig. 4.26 SiC switching waveforms loss: turn on : 0.02mJ, turn off : 0.05 mJ (1us/div)

Though the turn-on of BJT shows no overlapping on the switching waveform, there is still loss associated. Fig. 4.27 shows the voltage and current waveforms across IGBT device. The total IGBT loss is about 0.2mJ.

Fig. 4.27 IGBT current and voltage waveforms. (1us/div)

The MOSFET will need to cut off certain amount of current. However, the MOSFET voltage is clamped by base-emitter junction of BJT, thus the switching loss on MOSFET is quite small.

Fig. 4.28 shows the current waveforms of MOSFET, IGBT and BJT base current waveform. Overall, all the three devices are switched under soft commutation condition. The stress on each of the power device is limited. Turn-on di/dt is limited by resonant inductance and turn-off dv/dt is limited by snubber capacitors.
The inherent soft switching property makes the hybrid structure looks very attractive. However, as shown in Fig. 4.29, if there is no other branch for current low, the “two terminal” switch current and switch voltage have to have overlapping. In other words, during the turn-on transition, the switch current has to override the load and diode reverse current before the device voltage increases. However, if we look at the individual switch switching waveform, they have very little overlapping period. The soft transition for each individual switch is achieved from the experimental results, as shown in Fig. 4.26 through Fig. 4.28.

For current driven device, there is an extra need of base driver power consumption. Since the voltage source of gate driver only provides very little amount of static current, the power needed to drive the transistor can only provided from the inductor current. During turn-on transition, the energy is stored in the forms of the energy in the resonant inductor. The base part of the inductor current is
providing source for the base drive, the excess part of the inductor current is freewheeling in loop L₁ in Fig. 4.23 (d) and gradually dissipated by the conduction voltage drop in the L₁ loop.

Fig. 4.30 Reduced conduction drop with excess base current. (2us/div)

However, when the extra part of the base current is in circulation, the conduction voltage drop of the device is reduced which in turn reduces the conduction loss. Fig. 4.30 shows the conduction voltage drop on the SiC device. The energy in the inductor is partially recovered. The conduction loss can partially be point out by looking at power loss on IGBT device. The conduction loss is still one major points that needs further improvement. Fig. 4.31 shows the experimental results of steady state forward voltage drop with the proposed base driver scheme.

Although the driver based soft switching scheme is primarily derived based on SiC BJT diver design, the same concept is valid for Si BJT as well. With the proposed soft switched base driver design, the BJT can achieve built-in soft transition. Similar to PEBB concept, the overall base driver
structure could be treated as a soft switch building block (SSBB). This feature makes it very easy to implement a family of soft switching power converters. Fig. 4.32 shows the conceptual diagram of a soft switching inverter based on the proposed soft switch base driver.

![Conceptual diagram of a soft switching inverter based on Soft Switch Building Block (SSBB) concept](image)

**Fig. 4.32 A soft switching inverter based on Soft Switch Building Block (SSBB) concept**

![Waveforms of phase leg waveform and Si BJT device voltage and current](image)

**Fig. 4.33 Soft switching Si ZVT BJT inverter waveforms**

Fig. 4.33 shows experimental results of a phase-leg Si BJT inverter operation of the proposed scheme, which shows achieved ZVT as well as well controlled spike on the power device. The inverter is operated at 40kHz switching frequency. There is virtually no current spike on the main BJT device current. This means the ZVT condition is achieved under all load condition since a snubber capacitor is connected across the main BJT device. The voltage waveforms are very clean with virtually no overshoots.

In summary, the two major barriers that limit the usage of high power SiC BJT including high loss in base driver and secondary breakdown issue are eliminated by the proposed new soft-switched
IGBT and MOSFET gated bipolar junction transistor (SSBJT) base driver scheme. The zero-voltage turn-on of SiC BJT can be adaptively achieved with wide range of load current. The switch transition can be well controlled with proper resonant tank design thus avoiding the concurrence of high current and high voltage. The proposed “switch” structure can be driven with one simple voltage signal thus minimized the need for gate power. The switch characteristics should be similar to that of an IGBT with “NPN” body instead of “PNP” body. Compare to IGBT, the turn-off tail should be reduced with the existence of the P-FET. The whole SSBJT structure could be regarded as a new voltage driven “soft switch”. The new switch has inherent soft transition property with reduced switching loss. The driver structure is especially good for SiC BJT with fast turn off characters since no negative voltage is applied during turn-off transition.
Chapter 5 Generalized PWM soft switch for power converter

What distinguishes the soft switched base driver from a regular passive snubber is the transformation of the inductor energy. Instead of being dissipated or moved around by lossless snubber network, the inductor energy is utilized for base power for current driven device. For current driven device, the base energy is necessary and the proposed soft switching base driver takes advantage of this. The extra cost over the original hard switched design could be minimal. Now the question is whether this concept can be further implemented on more widely used voltage driven devices such as MOSFET and IGBT. This chapter identifies the more generic characteristics of the soft switching base driver proposed in the previous chapter and proposed a more general “soft switch” idea. The design and analysis of a soft switch based boost ZVT converter shows the validity of the proposed concept. Experimental results show the unperceived 98.9% efficiency of a 3kW boost converter with excellent performance.

5.1 A more generalized PWM soft switch concept

The SSBJT switch structure in the previous chapter can be redrawn as shown in Fig. 5.1. The switch can be divided into three portions: Left part is a turn-on current path, conduction current path in the middle and turn-off current path on the right. During the turn-on transition, the resonant inductor $L_r$ served as a snubber in the turn-on current path. The turn-on energy is stored in the resonant inductor. After the BJT is turned on, it gradually takes over all the load current with low forward voltage drop. The turn-off energy is stored in the snubber capacitors during turn-off transition. The key point is to separate the transition path of the power switch: the turn-on and turn-off paths consist of soft commutation elements and main conduction path provides lower conduction voltage drop.

![Fig. 5.1 Conceptual diagram of a switch with separate path for conduction and commutation](image-url)
The idea of separating the turn-on and turn-off paths is not new. The earlier version of MOS-Transistor pair is aiming to use transistor as conduction device and use MOSFET as switching device [B22]. Fig. 5.2 shows the basic structure of a MOS-BJT pair. The concept to let the fast switching MOSFET handle the switching loss and let the low voltage drop BJT handle the main power during regular conduction. Fig. 5.3 shows a possible improved version of the MOS-bipolar paralleled with turn-on snubber made of a small magnetic bead. The transistor provides lower conduction voltage drop during regular conduction period. The current shifting is relatively quick since only very small inductance is involved. The energy stored in the stray inductance is dissipated in the red loop indicated. The MOSFET is still hard turn-off and extra over-voltage clamp circuits may be necessary. The idea is straight-forward, but this method is not seriously implemented because it is not practical and is soon obsolete when high power MOSFET and IGBT came into business.

![Fig. 5.2 Basic MOS-Bipolar parallel Structure](image1)

![Fig. 5.3 MOS-Bipolar parallel structure with turn-on snubber bead](image2)
Fig. 5.4 Inductor energy served as a source for compensated Darlington

Fig. 5.4(a) shows the structure of the proposed soft switching based driver. When the energy stored in the resonant inductor is shifted gradually to the main transistor, it serves as an equivalent voltage source like a compensated Darlington. This will decrease the forward conduction voltage drop during this period. The energy loss is the conduction loss through the voltage drop on the FET and base-collector junction. Consider an ideal case. If the voltage drop $V_{Lr}$ can be held constant on the driver FET and base-collection junction, which means the inductor current is decreasing at a certain rate, then the $V_{ce}$ drop of the device can always be kept small or even no forward voltage drop! In reality, the inductor current will be shifted gradually in the green loop to the main transistor and energy is partially recovered in the return of reduced forward voltage drop. A wider base region BJT would be more favored for the soft switching base driver application. However, the drawback is the inductance can not be chosen too big. If it takes too long for inductor current to drop to the normal value, the minimum duty cycle will be affected. A typical inverter application will prefer a short pulse as narrow as 3-5us. It would be more attractive to have the inductor energy fully recovered. Although most power applications do not have very narrow pulse requirements, this driver method is still better than other proposed methods in the literature [B7]-[B24].

Fig. 5.5 shows a three terminal soft-switching PWM cell based on the proposed base driver scheme. By replacing the standard hard-switching PWM cell, a family of soft switching power converter could be easily developed, as shown in Fig. 5.6.
The circuits in Fig. 5.3 will have a voltage overshoot problem during turn-off. Thus it’s better to have a separate turn-off path, such as a capacitor. Using saturable core can reduce the total energy stored in the inductor. Fig. 5.7 shows an improved version of it. Any device with lower voltage drop is good. Fig. 5.7 can actually guarantee zero voltage turn-on for the main device if G2 gate is delayed a little while. However, the energy stored in inductor is still gradually dissipated in main switch.
main switch may not necessarily be BJT, now if it is replaced by an IGBT or MOSFET, a more useful circuits could be developed.

![Diagram](image)

Fig. 5.7 Zero-voltage turn-on achieved with gate delay and resonant capacitor.

![Diagram](image)

Fig. 5.8 A further improved voltage driven switch pair with built-in ZVT turn-on.

Note that in order to make circuits in Fig. 5.8 function, the voltage drop in the main current flowing path must be lower than the voltage drop in the auxiliary device. This is the mechanism that brings down the inductor current to near zero. With the discussion in the previous chapters, it would be very natural to think of using a coupled inductor to recover the energy stored in the inductor. This brings about an improved new PWM soft switch structure, as shown in Fig. 5.9.
The coupled inductor introduces an auxiliary voltage source to reset the resonant inductor current. As introduced in the last section in Chapter 3, if the turns ratio $N_s/N_p$ is larger than unity, then the zero-voltage switching of the main switch can be achieved with a simple fixed delay. The resonant tank operation is similar to that shown in Fig. 3.44. In this case, only one single gate driver is needed to drive the proposed PWM soft switch. The detailed analysis of circuit operation will be given by the example of a tested 3kW boost converter in the next section.

It would be straight-forward to apply the voltage-driven PWM soft switch concept back to the previously proposed SSBJT. As shown in Fig. 5.10, the coupled inductor can be used instead of two inductors. The inductor energy can now be fully recovered, which makes the circuit more attractive. Both soft switching structures in Fig. 5.10 are simulated and verified by experimental results. More details will be given in later section. Based on all the previous discussions, both soft switch structures in Fig. 5.10 share some common features and are now be defined a new name which is the focus of this chapter: “Soft Switch”. The definition is given on the next page.
(a) PWM Soft switch for current driven device such as BJT and GTO

(b) PWM Soft switch for voltage driven device such as IGBT and MOSFET

Fig. 5.10 Coupled inductor based PWM soft switch circuits.
**Definition:**

A PWM soft switch is a PWM switch that can achieve built-in adaptive soft switching.

The following features should be accomplished by the switch structure:

- Maintain basic square wave shape of the original hard switched PWM converter thus no modification of original PWM control regulator is needed.
- All the power switches transitions are under soft commutation condition.
- The auxiliary control signal is internally derived from the main PWM control with very simple fixed timing delay. In other words, no current or voltage information, both amplitude and polarity, is needed.
- Single signal to drive the soft switch
- The circulation energy is minimized and recovered while achieving soft switching at all load current condition.
5.2 High efficiency PWM soft switch boost converter

In the previous section, two soft switch solutions are proposed based on the inductor coupling scheme. The concept needs further verification. This section emphasizes on the verification of the proposed PWM soft switch solution based on a ZVT boost converter example. This section starts with the very early boost converter proposed by Hua in early 90’s. The fundamental problems are common for more complicated ZVT converters. But with the simple boost type structure, it is much easier to identify the key issue. This makes it easier to focus on the key improvement of the proposed new soft switch based ZVT boost converter. A simple analytical approach is proposed to conveniently analyze the behavior of inductor coupled ZVT circuits without going through tedious state equations. Finally, the experimental result on a prototype boost converter is presented to show the excellent performance based on the proposed PWM soft switch ZVT solution.

5.2.1 Basic operation and analysis of ZVT boost converter

Fig. 5.11 shows the circuit diagram of a ZVT boost converter proposed in [C15]. Fig. 5.12 shows the simulated waveforms of the boost converter.

![Fig. 5.11 Hua’s ZVT boost converter](image-url)
Fig. 5.12 Simulation waveforms of Hua’s ZVT circuit

The benefit for this circuit is that the zero voltage condition can be achieved with no over boost. In Fig. 5.12, the peak auxiliary current is limited. The first well known problem is that auxiliary device is hard turn-off. The auxiliary voltage is clamped to DC bus voltage to reset the resonant inductor current. The second problem is the reverse recovery of $D_c$ during the end of discharging period of $L_r$. As indicated in Fig. 5.13, the $L_r$ current tends to go negative and will generate a freewheeling loop. The freewheeling will not stop until the energy is all dissipated by loop conduction loss or when the main switch is turned off. Fig. 5.14 shows the freewheeling equivalent circuits. The peak freewheeling current could be expressed as following:

$$I_{pk} = I_{Dc\_rr} + \frac{V_o}{L_r} \sqrt{\frac{C_{out\_lx}}{C_{out\_lx}}}$$

(5-1)

Fig. 5.13 Freewheeling loop associated with $D_c$ turn-off
Fig. 5.14 Equivalent circuit for freewheeling path when resonant inductor fully discharged

C\textsubscript{out,ss} is the output capacitance of the auxiliary device. It can be seen that two portions are counted for this current. The diodes reverse recovery current of D\textsubscript{c} and discharge of S\textsubscript{x} junction capacitor.

The other problem happens when the main switch is turned off. D\textsubscript{x} reverse recovery current as the results of the freewheeling loop mentioned above will generate an extra freewheeling current flowing through L\textsubscript{r}. Assume D\textsubscript{x} has very little reverse recovery current, the junction cap will still resonate with L\textsubscript{r} and create an initial current through L\textsubscript{r}. The peak current can be given by the following equation:

\[ I_{pk\_frewheel} = \frac{V_o}{\sqrt{\frac{L_r}{L_m + C_{out,S_x} + C_j - D_c}}} \]  

(5-2)

Depending on forward voltage drop of D\textsubscript{o} and D\textsubscript{c}, the freewheeling current could be building up or decreasing gradually. Fig. 5.16 gives the equivalent circuits of this part.

Fig. 5.15 A freewheeling path generated when S is turned off.
The circuit initial condition is: $i_{L_t}=I_{r}$ (reverse recovery current of Dx if freewheeling current path shown in Fig. 5.13 is present) and $V_{sx}=0$. $V_{in}$ could be considered ramping up linearly with a constant rate. A slower ramp will induce less initial freewheeling current in $L_t$. Fig. 5.17 shows the voltage and current of the resonant inductor.

Fig. 5.17 Resonant inductor voltage and current waveforms.

Fig. 5.18 shows a practical improvement Hua’s ZVT circuits. A diode $D_b$ is inserted to prevent the MOSFET body diode from conducting, which resolves the freewheeling problem when auxiliary current reverse. A saturable core successfully limits the amplitude of the freewheeling loop.
Using coupled inductor for soft switching was originally introduced by Barbi [C13] and later improved by J. P. Gegner and C. Q. Lee [C18] in DC-DC converter application. Fig. 5.19 shows the circuit diagram introduced in [C18].

The circuit in Fig. 5.19 however, suffers both freewheeling problem when $D_c$ turns off and main switch is turned on. Although diode $D_c$ can clamp the voltage stress on $S_a$ to DC bus, diode $D_s$ will see voltage above the bus voltage when the auxiliary switch is turned off. The voltage stress on $S_x$ is actually shifted to $D_s$. The auxiliary gate pulse needs to be tuned off earlier than the main pulse. Otherwise, the magnetizing current will not be reset within a switching cycle. This makes it difficult to share a same gate driver for $S$ and $S_x$. Furthermore, the use of auxiliary device with power MOSFET will lead to current spike on resonant inductor when the main device $S$ turns off. A patch shown in the
prior arts is to add two to three diodes in series to replace $D_s$. This will prevent the freewheeling current from building up. However, this adds extra components and increases conduction voltage drop.

Fig. 5.20 Proposed boost converter based on soft switch cell.

Fig. 5.20 shows the proposed boost converter by plugging in the three terminal soft PWM switch. Compared to Fig. 5.19, the new circuits get rid of two diodes $D_b$ and $D_c$. From the earlier analysis, $D_b$ is a patch for diode reverse recovery problem of $D_c$. From Hua’s basic ZVT circuit, almost all the later ZVT cells were trying to make $S_x$ unidirectional by inserting a series diode. Since $D_c$ serves similar function in blocking reverse inductor current, blocking diode $D_b$ is not necessary for ZVT operation. By removing $D_c$, the second freewheeling loop, shown in Fig. 5.15, is cut off. However, the reverse recovery of $D_s$ generates over-voltage ringing and the problems addressed by Fig. 5.13 still exist. A saturable core is thus added to damp the reverse recovery current. A “spike killer” type of core would be a good choice. This is almost common to every ZVT scheme since the resonant inductor current always needs to be discharged to zero and then blocked by a fast diode.

5.2.2 Equivalent circuit analysis of the proposed boost converter

The operation of a boost converter is similar to that of the inductor coupled ZVT converter discussed in Chapter 3 except that the load current is unidirectional for boost converter case. Fig. 5.21 shows the operation key waveforms of the proposed ZVT boost converter. $V_S$ and $V_{Sx}$ are the voltage...
across the main and auxiliary switches. $I_{Sx}$ is the auxiliary switch current. The control scheme is to simply delay the rising edge of the main switch by a fixed timing $T_{dy}$.

Fig. 5.21 Operation key waveform of soft switch based boost converter

Fig. 5.22 shows the operation stages of the proposed boost converter. The operation stages could be described as following:

a) **Initial stage**: the load current is flowing through the rectifier diode $D_o$; both switches are off.

b) **Linear charging** ($t_0$-$t_1$): At $t_0$, auxiliary switch is turned on at zero current condition. The output voltage is applied on the primary side of the coupled inductor. The equivalent resonant inductor is the total leakage inductor. The current is built up linearly in auxiliary switch while the current in the rectifier diode is decreased linearly. A more detailed analysis will be given at a later section.
Fig. 5.22 Operation stages of the proposed ZVT boost converter
c) **Resonant stage** (t₁-t₂): At t₁, the total resonant branch current $I_{Lr}=(1+n)I_{Ls}$ is higher than the load current thus the rectifier diode turns off. $L_x$ and $C_x$ begin to resonate at the end of the resonant stage $t_2$, the switch voltage drops to zero. $L_x$ stands for equivalent resonant inductance and $C_x$ is the equivalent resonant capacitance. In this case $C_x=C_r+C_{jDo}$. $C_{jDo}$ is the junction capacitor of the output rectifier $D_o$.

d) **Discharge stage I** (t₂-t₃): At $t_2$, the total resonant current $I_{Lr}$ is still larger than the load current. The body diode of the main switch $S$ is turned on and conducting current. Main switch $S$ can be turned on at zero voltage condition at $t_m$. The output voltage is then applied to the secondary and linearly discharging the resonant inductor current. The current is then shifted linearly from the body diode to the main switch $S$ until at $t_3$, $I_{Lr}$ is equal to load current and the main switch body diode stops conduction.

e) **Discharge stage II** (t₃-t₄): The auxiliary branch current is linearly discharged until $i_{Ls}$ decrease to zero at $t_4$ and diode $D_s$ starts blocking the output voltage.

f) **Conduction stage** (t₄-t₅): At $t_4$, the load current is going through the main switch $S$. However, the auxiliary switch $S_x$ still conducts small amount of the magnetizing current $I_{Lm}$. The magnetizing current is freewheeling in the loop of $S$ and $S_x$.

g) **Turn off reset stage** (t₅-t₇): Both switches are turned off at $t_5$. Load current is charging the resonant cap. The voltage across main switch $V_s$ is then increasing linearly. The magnetizing current is charging up the junction cap of the auxiliary switch $C_j$. The magnetizing energy stored is transformed in the form of $C_j$. Partial of the energy is recovered to the output when diode $D_o$ conducts when $V_{Sx}$ is higher than $V_o$. The voltage across auxiliary switch will be higher than output voltage. Special care must be taken when choosing the resonant tank to make sure the auxiliary switch voltage is under acceptable level. The coupled inductor however, is guaranteed to be reset each and every switching cycle.

The analysis of coupled inductor based ZVT scheme can be done by derivation multi-loop differential equations during every operational stage. This is time consuming and easy to make mistake. The inherent physical merit of the circuit can hardly be grasped when considering the magnetic inductance of the coupled inductor.
This section will introduce an equivalent inductance based method to simplify the analysis of coupled inductor based resonant circuits. First of all, the soft switching cell is redrawn to represent the leakage and magnetizing inductance, as shown in Fig. 5.23. Then an equivalent circuit is given in Fig. 5.24 based on Thevenin equivalent circuit theorem.

By solving several loop equations, the derived equivalent voltage source and inductance are given by:
\[ L_{eq} = \left( \frac{n}{1 + n} \right)^2 (L_{rp} + L_{rseq}) \]  
\[ L_{rseq} = \frac{L_{rs}}{n^2} \]  
\[ V_{eq} = \frac{V_s}{1 + n} \]  

This is a generic conversion that all the analysis for coupled inductor based circuits could be simplified by this approach. The following parts will describe how to utilize this conversion to derive the simplified equivalent circuits. For design simplification, the effects of saturable core are not considered. Fig. 5.25 shows the charging stage equivalent circuit. In order to use the conversion method mentioned earlier, the voltage source \( V_s \) is mirrored to both sides of the circuit. It is now fairly easy to identify the further simplified equivalent circuit as shown in Fig. 5.26.

![Fig. 5.25 Charging stage equivalent circuits](image1)

![Fig. 5.26 Simplified charging stage equivalent circuit](image2)
The linear charging stage ends when current flowing through \( L_{eq} \), \( I_{lr} \), is equals to \( I_{load} \). Without writing a single loop equation, we can get the duration time for the charging stage:

\[
T_{lin} = \frac{L_{eq} \cdot I_{Load}}{n \cdot \left( \frac{n}{n+1} \right) \cdot V_s} \tag{5-6}
\]

Note that only a fraction of \( L_{eq} \) current \( I_{lr} \) is flowing through the auxiliary switch. Equation (5-6) or Fig. 5.26 only reveals the total resonant branch current and behavior. Sometimes it may be necessary to understand the current through the primary side or the auxiliary current \( i_{Lrp} \). When the magnetizing current is neglected, the auxiliary branch current can be given as:

\[
i_{Lrp} = \frac{i_{lr}}{n \cdot \left( \frac{n}{n+1} \right)} \tag{5-7}
\]

\( L_{leakage} \) is defined as the total leakage inductance measured from primary when secondary side is shorted:

\[
L_{Leakage} = \left( L_{rp} + \frac{L_m \cdot L_{req}}{L_m + L_{req}} \right) \tag{5-8}
\]

Then we have the following approximation when \( L_{req} \) is much smaller than \( L_m \):

\[
L_{eq} = \left( \frac{n}{1 + n} \right)^2 \cdot L_{Leakage} \tag{5-9}
\]

With the consideration of (5-7) and (5-9), another equivalent circuit can be drawn to help identify the actual winding current for analysis the actual winding current. Fig. 5.27 gives the equivalent circuit with a “virtual transformer” to help understand the actual physical winding current.
The equivalent circuits of resonant stage in Fig. 5.22 (c) can be redrawn as shown in Fig. 5.28. $C_p$ is the resonant capacitor added in parallel with rectifier diode. $C_p$ represents the junction capacitance if no extra capacitor is added. $C_n$ is the resonant capacitor put across the main switch. With similar transformation approach shown in Fig. 5.24, the further simplified circuit can be derived as shown in Fig. 5.29. $C_r$ is the equivalent resonant capacitor. Resonant period ends when $V_{Ct}$ voltage reaches $V_s$ and the main switch body diodes starts to conduct. The calculation of resonant period will be exactly the same as that shown in Chapter 3.3 and will not be repeated here.

Fig. 5.28 resonant stage equivalent circuits
Fig. 5.29 further simplified resonant stage circuits

Fig. 5.30 shows the discharging stage circuit and Fig. 5.31 shows the simplified equivalent circuits with the same approach above.

Fig. 5.30 discharge stage equivalent circuit

Fig. 5.31 Simplified discharge stage circuit

Comparing the equivalent circuit in Fig. 5.26 and Fig. 3.31, it can be identified that this application falls in the generalized ZVT analysis in Chapter 3.
\( L_{\text{eq}} \) is the equivalent resonant tank inductance. Comparing equation (5-6) to equation (3-17) from chapter 3, we can get:

\[
V' = \frac{V_s}{1 + n} \tag{5-10}
\]

\[
k = \frac{1}{1 + n} \quad k_1 = \frac{n}{1 + n} \tag{5-11}
\]

\[
L_r = L_{\text{eq}} = L_{\text{leakage}} * \left( \frac{n}{1 + n} \right)^2 \tag{5-12}
\]

Fig. 5.32 shows the normalized state plane diagram of the boost converter. Since the boost converter circuits share the same generated fixed ZVT structure discussed in Chapter 3, all the discussions in Chapter 3 are still valid. Thus the calculation results can be directly applied and will not be repeated.

Fig. 5.32 State plane diagram of resonant tank for PWM soft switch boost converter

5.3 Verification of PWM soft switch based boost converter

Fig. 5.33 shows the picture of a 3kW boost converter built to verify the proposed soft switch scheme. To focus on the soft-switching operation, only open-loop fixed duty control is implemented.

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A fixed value power resistor is used as converter load. The turns ratio of \( n_p/n_s \) is about 1:1.25. The total leakage inductance measured from primary side is about 2uH. Both the main switch and diode is in parallel with a 2.2nF resonant cap. The main device is Infenion CoolMOS\textsuperscript{TM} to reduce condition voltage drop. Because of zero-voltage switching operation, a low forward voltage drop instead of fast recovery diode is preferred when select rectifier diode \( D_o \). As described in the previous section, diode \( D_s \) in the auxiliary branch will need to be fast recovery to avoid unwanted ringing and freewheeling current. A saturable core is typically needed to damp the ringing when resonant inductor current reduces to zero at time \( t_4 \) in operation stage as in Fig. 5.21.

![Fig. 5.33 A 3kW soft switch based boost ZVT converter.](image)

Fig. 5.33 A 3kW soft switch based boost ZVT converter.

Fig. 5.34 shows the simulated waveforms of the proposed ZVT boost converter. The main switch gate signal \( G_s \) delays for fixed 0.8us time than the auxiliary gate signal \( G_{sx} \). Fig. 5.34(a) shows the main device voltage \( V_{sw} \) and current \( I_{sw} \) waveforms and resonant current \( I_{Ls} \) flowing through \( D_s \). It can be seen that the zero-voltage condition is achieved under all load current condition. Fig. 5.34(b) also shows the auxiliary device voltage \( V_{sx} \). When both switches are turned off, the voltage across the auxiliary device is higher than the output bus voltage. This over-voltage is needed to resetting the magnetic current. The magnetic inductance energy will be mostly recovered to the output. However, the energy stored in junction capacitor of auxiliary device \( S_x \) will be dissipated as pure loss.
(a) zero voltage condition achieved with different load current condition

(a) typical waveforms of boost converter

Fig. 5.34 Simulated waveforms of ZVT boost converter
Fig. 5.35 Zero voltage switching at different load condition

Fig. 5.35 gives the corresponding experimental waveforms of the boost converter at different output voltages: 200V and 330V. Due to the layout difficulties the device current is not measured. It can be seen, however, that the zero voltage switching condition is achieved because $V_{sw}$ is resonating smoothly to zero after the auxiliary switch is turned on. Otherwise, a switch node waveform similar to Fig. 3.14 would be observed if voltage swings back or drops abruptly due to incorrect timing.

Because the purpose of diode $D_s$ in the secondary branch of the coupled inductor is to block the negative current, it needs to be a very fast recovery diode. As mentioned in 5.2.1, a slower diode could cause unnecessary ringing due to parasitic leakage inductance and extra freewheeling current. Fig. 5.36 shows the comparison of typical waveforms between two different types of diode. In most cases, a saturable inductor or a spike killer will be very helpful to prevent $I_{Ls}$ from going negative.
The original choice of the switch for $S_x$ was to use MOSFET as previously reported [C18][C31]. However, very large ringing is generated and the auxiliary branch will conduct extra freewheeling current as indicated by problem No.3 in Fig. 5.17. A switch with a fast body diode such as IGBT would be more favorable. Fig. 5.37 shows the large ringing when using MOSFET as auxiliary switch when main switch is turned off.

Because the coupled inductor is reset every switching cycle, the core could be selected relatively small. However, the total volt-second during one switching cycle must be satisfied, otherwise the core could be saturated and causing unwanted excess current in the resonant branch. Fig. 5.38 shows the typical waveforms when the coupled inductor is saturated by using a MPP core. A core with lower core loss at the switching frequency would be more desirable. A low-cost selection is to use a ferrite torrid core. Fig. 5.39 shows the volt-second applied across the primary side of the coupled inductor. Because a saturable core is added in serial with the diode $D_s$, the majority of voltage-second is applied during the charging period.

Fig. 5.40 shows the current and voltage across the auxiliary switch and diode $D_s$. It can be seen that both the auxiliary switch and diode $D_s$ are switching under zero current condition. Very little loss is generated in diode $D_s$ that a tiny 1W heat sink would be sufficient to remove the heat as shown in Fig. 5.33.
Fig. 5.38 Typical waveforms when coupled inductor saturates

Fig. 5.39 Volt-second across the coupled inductor primary winding

Fig. 5.40 Auxiliary diode and switch voltage and current waveforms
The boost converter power stage was tested under 26 degree C room temperature driving a constant resistive load. Fig.5.41 shows the efficiency comparison of soft switched and hard switched converters. The input power is measured directly from DC power source, and the output power is measured at the resistive load using Yokogawa power analyzer with 0.1% accuracy. A constant duty of about 0.19 is used as fixed duty open loop control. The power loss of gate driver and control DSP is not counted. Though the efficiency improvement of soft switching boost is not as significant at light load, it is increased to about 1% to 1.5% when output power is above 2kW.

Fig.5.41 Efficiency comparison of hard switched and soft switched boost converter at 100kHz

It might be difficult to tell the difference by only looking at the efficiency curve between hard switching and soft switching converters. Fig.5.42 shows the comparison of temperature of the boost converter with no cooling fan. It can be seen the hard-switched converter has far more temperature rise than the soft-switched converter. The heat sink temperature of the hard-switched converter is too high that it is very difficult to further push the output power to anything beyond 2kW. The soft switched converter however, can easily run at 2.8kW with only little temperature rise on a small heat sink. The loss in the magnetic cores is not counted in the temperature rise since the core is not mounted on the heat sink. Only switches and diodes are mounted on the heat sink. Fig. 5.43 shows the screen shoots of Yokogawa measurement results at 2.8kW and 2.5kW. A very high efficiency of 98.9% is achieved even without much optimized layout. This is an exciting result that the number is better than all the previously reported soft switching boost converters at this power level [C15][C20][C31][C33].
In this section a high efficiency boost converter scheme with the proposed PWM soft switch is verified by both simulation and experimental results. The boost converter shares a single gate driver for both main and auxiliary switches. With very simple control and very limited cost, the converter efficiency can increased significantly and the heat sink requirement can be greatly reduced with high efficiency of 98.9% on the boost converter.
Chapter 6 Conclusion and future work

The soft switching PWM technique proposed in the early 90’s, combining the simplicity of PWM control technique and soft transition of resonant converter, is the most promising soft commutation method. One critical part to demonstrate the advantage of soft switching PWM technique is to achieve soft switching with minimal circulation energy. However, to achieve this goal with conventional approach, the instantaneous load current and voltage information is necessary to implement the timing control of the power switches. The increased control complexity and tuning efforts eventually increased overall cost significantly. This hampered the further implementation of soft switching PWM technique. Although promising theoretically, the soft switching PWM technique is not yet widely used in commercial products, especially for inverter application when load current changes in both direction and amplitude.

The other barrier for further advancements in technology and reduction of cost is the lack of standardization. This is especially true in soft switching PWM converters since individual power converter is designed to offer partial solutions for specific application. It would be more promising if a new approach with standard cell can combine both the benefit of soft switching and the compact design of gate drive based circuits.

The work in this dissertation presents the first attempt in the literature to systematically explore the “soft switch” concept. The goal of soft switch is to develop a standard PWM switch cell with built-in adaptive soft switching capabilities. Just like a regular hard switched PWM switch, only one PWM signals is needed to drive the soft switch to achieve soft switching condition. Two novel coupled inductor based PWM soft switch cell for current and voltage driven devices are proposed to prove the basic soft switch concept. The key feature and requirement of the soft switch is outlined. Over 15 technical papers are published during Ph.D. program in soft switching related area. The major results and contribution of this dissertation is summarized bellow.

6.1 Major results and contribution of this dissertation

The core technique in soft switch development is a built-in load adaptive soft switching circuit with minimized circulation energy. The necessity of minimizing circulation energy is first analyzed. The design and implementation of a universal controller for implementation of variable timing control
to minimize circulation energy is presented. A “piggy-pack” type universal variable timing controller is developed successfully to drive three 55kW soft switching inverters for electric vehicles application in the Partnership for the New Generation Vehicles (PNGV) project. The variable timing control effectively reduced unnecessary circulation energy during switch commutation. However, even with variable timing control, the optimal tuning of timing is very difficult to achieve, and thus the advantage of soft switching inverter is still very limited.

To simplify the control, several methods to achieve soft switching with fixed timing control are proposed. A soft-switching chopper design with near zero voltage switching approach was first presented. The key idea is to adjust the ratio of charging time and resonant time in order to get a near zero voltage switching with fixed timing control. Second, a load adaptive fixed timing control soft switching chopper is presented utilizing diode reverse recover current. The concept of using diode reverse recovery current as boost energy source to achieve zero voltage switching is proposed and verified. A more generalized fixed timing control method is presented by analyzing a family of soft switching inverter cell. A fixed timing inductor coupled ZVT inverter is proposed with load and source adaptivity. With non-unity turns ratio in the coupled inductor, the charging source in resonant tank could be higher than half of the DC bus voltage thus eliminate the needs of extra boosting charging stage. The experimental results of a 120kW inverter phase leg shows the zero voltage condition can be achieved with very simple fixed delay control circuit.

The driver based soft switch concept was originated from development of a base driver circuit for current driven bipolar junction transistor (BJT). A new insulated-gate-bipolar-transistor (IGBT) and power metal-oxide-semiconductor field-effect-transistor (MOSFET) gated transistor (IMGT) base drive structure was initially proposed for a high power SiC BJT. The proposed base drive method drives SiC BJTs in a way similar to a Darlington transistor. The proposed SiC base drive method successfully demonstrated to drive a 7.5HP motor for the first time reported in literature.

By comparing the typical ZVT scheme and the proposed base driver, the driver based soft switching SiC BJT structure is proposed with slight modification. The proposed diver can effectively drive SiC BJT with Darlington type connection and realize zero-voltage switching of the main device with one single gate signal. The proposed gate driver based soft switching method is verified by experimental test with both Si and SiC BJT. The soft switching bipolar junction transistor (SSBJT) structure behaves just like a voltage-driven soft switch module. The new structure has inherent soft
transition property with reduced stress and switching loss. The new base driver design resolved the two major issues for usage of SiC BJT: current driven driver requirement and high stress during switch transition that could potentially causing second breakdown.

The idea of separating turn-on, turn-off and conducting current path gives the hint to extend the SSBJT concept to voltage-driven device such as IGBT and MOSFET. A new coupled inductor based soft switching cell is proposed by reviewing the existing soft switching solutions. The proposed zero-voltage-transition (ZVT) cell serves as a good candidate for the development of soft switch. An “equivalent inductance” and state plane based analysis method are used to significantly simply the analysis of coupled inductor based zero-voltage switching scheme. With the proposed analysis method, the key operation of the ZVT cell could be identified without solving complicated differential equations. Detailed analysis and design is proposed for a 3kW boost converter. With the proposed soft switch design, the boost converter can achieve up to 98.9% efficiency over a wide operation range with a single gate drive. The saving on the thermal management could be significant gain over the cost of extra silicon. A family of soft-switching converter using the proposed “soft switch” cell can be developed by replacing the conventional PWM switch with the proposed soft switch.

6.2 Future works

In summary, A PWM soft switch is a PWM switch that can achieve built-in adaptive soft switching. To make a “soft switch” really a “switch”, integration technique is the key besides circuit topology. For voltage driven device, the most difficult part is the integration of magnetic. The first step could be focused on modulated hybrid “soft switch” development. Then later on, develop integrated magnetic will make the technology more attractive. The idea of separating turn-on, turn-off and conducting current path might be able to give device designers a hint to build a monolithic type soft switch with the help of some external passive components.

The SSBJT technique is among the best choice for driving SiC BJT. New device design could focus on forward voltage drop reduction rather than targeting on creating higher gain. The application for GTO device will be even more attractive because the only major disadvantage for the SSBJT: larger forward voltage drop do not apply to GTO. Once GTO is fully turned on, only a small current will be needed. The driver based soft switch GTO: SSGTO will be working more reliable than hard switched GTO and remove the bulky passive snubber from the power stage. The benefit from soft
switching will allow the switch to operate at a higher frequency which can significantly reduce the overall converter volume. The major modification from current GTO driver, such as ETO, to a SSGTO is only one extra high voltage switch which only needs to handle a fraction of the total power. Replacing the bulky snubber inductor in the main power path by a small air core inductor will have immediate attractive future.

The SSBJT technique green lights the future development of high power SiC BJT. The power level tested in this dissertation: 600V, 50A switch is far beyond other SiC device. SiC BJT would probably be the first SiC power switch suitable for commercial usage. Recently developed SiC VJFET could be a very good candidate for serving the auxiliary device. SiC VJFET is capable of handling high voltage and have relatively low conduction voltage drop.

Simplification for magnetic design still needs further work for inductor coupled ZVT soft switch scheme. It could be more attractive if an integrated magnetic design could be achieved, especially for isolated converters such as forward and flyback converters. More circuit application is yet to be developed based on the soft switch concept. The fundamental cell could be varies but the goal is the same: Built-in adaptive soft switching properties. A PWM soft switch module would not be too far away with new advances in package and device technique, which will eventually make soft switching technique closer to reality than ever before.
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C. DC-DC Soft-Switching Techniques


D. Soft Switching PWM Three Phase Converter Techniques


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E. Passive snubber for soft commutation


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F. Gate drive based di/dt and dv/dt control under hard switching mode


G. Publications during Ph.D. program:


Vita

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