Three Dimensional Passive Integrated Electronic Ballast for Low Wattage HID Lamps

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ABSTRACT

Around 19% of global power consumption and around 3% of global oil demand is attributable to lighting. After the first incandescent lamp was invented in 1879, more and more energy efficient lighting devices, such as gas discharge lamps, and light-emitting diodes (LED), have been developed during the last century. It is estimated that over 38% of future global lighting energy demand could be avoided by the use of more efficient lamps and ballasts [1].

High intensity discharge (HID) lamps, one category of gas discharge lamp, have been widely used in both commercial and residential lighting applications due to their merits of high efficacy, long life, compact size and good color rendition [2-4]. However, HID lamps require a well-designed ballast to stabilize the negative VI characteristics. A so-called ignitor is also needed to provide high voltage to initiate the gas discharge. Stringent input harmonic current limits, such as the IEC 61000-3-2 Class C standard, are set for lighting applications. It is well-known that high-frequency electronic ballasts can greatly save energy, improve lamp performance, and reduce the ballast size and weight compared with the conventional magnetic ballast. However, a unique phenomenon called acoustic resonance could occur in HID lamps under high-frequency operation. A low-frequency square wave current driving scheme has proved to be the only effective method to avoid acoustic resonance in HID lamps. A typical electronic HID ballast consist of three stages: power factor correction (PFC), DC/DC power regulation and low-frequency DC/AC inverter. The ignitor is usually integrated in the inverter stage. The three-stage structure results in a large size and high cost, which unfortunately offsets the merit of the HID lamp, especially in low-wattage applications. In order to make HID lamps more attractive in low-wattage and indoor applications, it is critical to reduce the size, weight and cost of HID ballasts.

This dissertation is aimed at developing a compact HID with an ultra-compact ballast installed inside the lamp fixture. It is a similar concept to the compact fluorescent lamp (CFL), but it is much more challenging than the CFL. Two steps are explored to achieve high power density of the HID ballast.
The first step is to improve the system structure and circuit topology. Instead of a three-stage structure, a two-stage structure is proposed, which consists of a single-stage power factor correction (SSPFC) AC/DC front-end and an unregulated DC/AC inverter/ignitor stage. An SSPFC AC/DC converter is proposed as the front-end. A DCM non-isolated flyback PFC semi-stage and a DCM buck-boost DC/DC semi-stage share the semiconductor switch, driver and PWM controller, so that the component count and cost can be reduced. The proposed SSPFC AC/DC front-end converter can achieve a high power factor, low THD, low bulk capacitor voltage, and the desired power regulation with a simple control circuit. Because the number of high-frequency switches is reduced compared to that of state-of-the-art two-stage HID ballast topologies, the switching frequency can be increased without sacrificing high efficiency, so the passive component size can be reduced. The power density of the whole ballast is increased using this two-stage structure. It results in a 2.5 times power density (6 W/in\(^3\)) improvement compared to the commercial product (2.4 W/in\(^3\)).

The power density of the converter in discrete fashion usually suffers as a result of poor three-dimensional (3D) volume utilization due to a large component count and the different form factor of different components. In the second step, integration and packaging technologies are explored to further increase the power density. A 3D passive integrated HID ballast is proposed in this dissertation. All power passive components are designed in planar shape with a uniform form factor to fully utilize the three-dimensional space. In addition, electromagnetic integration technologies are applied to achieve structural, functional and processing integration to reduce component volume and labor cost. System partitioning, integration and packaging strategies, and implementation of major power passive integration, including an integrated EMI filter, and an integrated ignitor, will be discussed in the dissertation. The proposed integrated ballast is projected to double the power density of the discrete implementation.

By installing the HID ballast inside the lamp fixture, the ambient temperature for the ballast will be much higher than the conventional separately installed ballast, and combined with a reduced size, the thermal condition for the integrated ballast will be much more severe. A thermal simulation model of the integrated ballast is built in the IDEAS simulation tool, and appropriate thermal management methods are investigated using the IDEAS simulation model. Experimental verification of various thermal management methods is provided. Based on the thermal management study, a new integrated ballast with improved thermal design is proposed.
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Chapter 1. Introduction

1.1. Background

It is well-known that lighting represents a major component of energy consumption worldwide. Around 19% of global power consumption and 3% of global oil demand is attributable to lighting [1]. In 1879, Thomas Edison invented the "practical" electric light bulb. Since then, many significant energy-saving lighting products have been invented. Today there are nearly 6,000 different kinds of lamps being manufactured, most of which can be placed in the following three categories: incandescent lamp, gas discharge lamp, and light-emitting diode (LED).

Incandescent lamps, gas discharge lamps and LEDs generate light through different physical mechanisms of electrical energy conversion [5].

Incandescent lamps use the Joule-heating process by electrically heating high-resistance tungsten filaments to intense brightness. The lamp current is determined by the applied voltage and the resistance of the tungsten filament, which is close to the v-i characteristic of a linear resistor. The spectrum of energy radiated from incandescent lamps is continuous with good color rendition. However, incandescent lamps usually have low efficiency and only around 10% of the electrical energy flowing through incandescent lamps is converted to light.

Gas-discharge lamps generate light by sending an electrical discharge through an ionized gas, i.e. plasma. Typically, such lamps are filled with both noble gases and metals, such as mercury, sodium, and/or metal halides. Then, the metals produce the light once they are heated to a point
of evaporation, forming a plasma. During operation the gas is ionized, and free electrons, accelerated by the electrical field in the tube, collide with gas and metal atoms. Some electrons circling around the gas and metal atoms are excited by these collisions, bringing them to a higher energy state. When the electron falls back to its original state, it emits a photon, resulting in visible light or ultraviolet radiation. Ultraviolet radiation is converted to visible light by a fluorescent coating on the inside of the lamp's glass surface for some lamp types.

An LED is a semiconductor diode that emits light when an electric current is applied in the forward direction of the device. The effect is a form of electroluminescence where incoherent and narrow-spectrum light is emitted from the p-n junction. An LED is usually a small-area light source of less than 1 mm², often with optics added to the chip to shape its radiation pattern and assist in reflection [6, 7]. The color of the emitted light depends on the composition and condition of the semiconducting material used, and can be infrared, visible, or ultraviolet. LEDs are widely used as indicator lights on electronic devices and increasingly in higher-power applications like flashlights and area lighting. Because individual LEDs are low-voltage DC devices, operating from AC mains requires well-designed circuitry and a thermal case to dissipate the heat.

Common characteristics used to evaluate lamp quality include luminous efficacy, typical lamp life, and color rendering index [8].

Luminous efficacy is the most important property of light sources, which indicates the fraction of electromagnetic power which is useful for illumination. It is the ratio of emitted luminous flux to radiant flux, and is measured by lumens per watt (lm/W). Light with wavelengths outside the visible spectrum reduces luminous efficacy, because the light with non-visible wavelengths contributes to the radiant flux, while the luminous flux of this light is zero.
Wavelengths near the peak of the eye's response contribute more strongly to radiant flux than those wavelengths near the edges of the eye’s response.

Typical lamp life is the number of hours it takes for approximately 50% of a large group of lamps of the same kind to fail. Failure means that the lamp will no longer light or that light output has dropped to a specific percentage value.

The color rendering index (CRI) is a quantitative measure of the ability of a light source to reproduce the colors of various objects faithfully in comparison with an ideal or natural light source. A reference source, such as black-body radiation, is defined as having a CRI of 100. This is why incandescent lamps have that rating; they are, in effect, almost black-body radiators. CRI is expressed in a scale of 0 to 100. The best possible faithfulness to a reference is specified by a CRI of 100, while the very poorest is specified by a CRI of zero.

1.2. **HID Lamp and Ballast**

1.2.1. **HID lamp**

Gas discharge lamps consist of low-pressure discharge lamp and high-pressure discharge lamp. Fluorescent and low-pressure sodium (LPS) lamps operate on low-pressure gaseous discharge, and the mercury vapor, metal halide (MH) and high-pressure sodium (HPS) lamps operate on high-pressure gaseous discharge. The mercury vapor, metal halide and HPS lamps are commonly known as high-intensity discharge (HID) lamps.

The fluorescent lamp (FL) is the most common lamp in office lighting and many other applications. FLs can produce up to 100 lumens/watt.
Low-pressure sodium lamps are the most efficient gas-discharge lamp type, producing up to 200 lumens/watt, but at the expense of very poor color rendering. The almost monochromatic yellow light is only acceptable for street lighting and similar applications.

Mercury vapor (MV) lamps were the first commercially available HID lamps. Originally they produced a bluish-green light, but more recent versions can produce light with a less pronounced color tint. However, mercury vapor lamps are falling out of favor and being replaced by sodium vapor and metal halide lamps.

Metal halide (MH) and ceramic metal halide (CMH) lamps can be made to give off neutral white light useful for applications where normal color appearance is critical, such as TV and movie production, indoor or nighttime sports games, automotive headlamps, and aquarium lighting. MH lamps can attain 100 lumen/watt light output.

High-pressure sodium (HPS) lamps produce up to 150 lumens/watt. HPS lamps tend to produce a much whiter light than the LPS lamps, but still with a characteristic orange-pink cast. New color-corrected versions producing a whiter light are now available, but some efficiency is sacrificed for the improved color. HPS lamps are mainly used for street lighting.

HID lamps have been widely used in both commercial and residential lighting applications, such as track lighting for offices and retail environment (20W-39W), automotive headlights (35W-70W), LCD projectors (100W-150W), supermarket lighting (175W-400W), stadium, parking area and roadway/tunnel lighting (400W-2000W), and so on.

Compared with incandescent lamps, gas discharge lamps have three great virtues as light sources: They are efficient energy converters with four times higher efficacy than incandescent lamps (75-80 lumen/watt for MH); they last a long time, 18 times longer than incandescent
lamps if fluorescent lamps are taken as an example (rated life up to 20,000 hours); they have excellent lumen depreciation, typically delivering 60% to 80% of the initial level of light at the end of life. [1-3]; due to the compact tube structure, HID lamps especially MH lamps have good focusing capability; MH lamps also have versatility in color.

1.2.2. HID ballast

Although gas-discharge lamps have tremendous advantages over incandescent lamps, they require an auxiliary apparatus called a ballast to run with them. It is a well-known fact that gas discharge lamps have negative incremental impedance [9], as shown in Figure 1-1. If an HID lamp is directly connected to a voltage source, a small variation of the current may lead to the extinguishment or bursting of the lamp. As a result, a ballast with a positive impedance is needed to compensate the negative incremental impedance, and stabilize the lamp current. This is the first requirement for the HID lamp ballast.

![Figure 1-1. Negative incremental impedance of gas discharge lamp.](image)

Obviously, the resistive ballast incurs large power loss and significantly reduces the system efficiency. Fortunately, most discharge lamps are operated in alternating-current (AC) circuits, so inductive or capacitive impedance can be used to provide current limitation. The inductor
and the inductor-capacitor (lead) ballast represent the conventional ballasting approaches, and are known as magnetic ballasts.

Magnetic ballasts are operated at 50/60Hz line frequency. Every half line cycle, they reignite the lamp and limit the lamp current. Although magnetic ballasts have the advantages of low cost and high reliability, they have several fundamental performance limitations due to their low-frequency operation. First of all, the ballast is bulky and heavy. Second, the arc is reignited twice each line cycle, which causes two big problems: significant lamp electrode wear and annoying audible line frequency flickering [10]. Finally, there is no efficient and cost-effective way to regulate the lamp power.

These drawbacks led to studying the use of high-frequency AC current to drive the discharge lamps. High-frequency operation not only results in significant ballast volume and weight reduction, but also improves the properties of the gas discharge lamp, such as improved circuit efficiency, improved luminous efficacy of lamps, improved lamp lifetime, absence of flickering, and the elimination of audible noise.

1.2.3. Ignitor

Most types of HID lamps, including metal halide and high-pressure sodium lamps, require an external ignition device, a so-called ignitor, either as an integral part of the ballast, or as a separate item of the control gear. Basically the function for an ignitor is to deliver a proper ignition voltage for starting the discharge in the HID lamp. Different HID lamps require different ignition voltages. The shape of voltage peak, the number of voltage pulses within a certain period, the instant of application of the voltage itself, the amount of energy available and the amplitude, all play a part in creating an optimum situation for establishing a discharge. After
ignition, the ignitor has to stop producing ignition peaks. This can be controlled by sensing the lamp voltage or lamp current.

For cold lamps, the required voltage pulses are of the order of 1kV to 5kV, while the maximum permitted amplitude of the pulse is limited by the lamp construction and the type of lamp holder.

Apart from the amplitude of the pulse, the width, the number and the position of pulses are also important to provide a high enough voltage to take over the lamp current after ionization.

1.2.4. Acoustic resonance

In principle, the use of high-frequency electronic ballast can reduce the size and the weight of the ballast and improve the system efficacy. This feature is especially attractive for low-wattage HID lamps, because the overall lighting system is expected to have a small size. Moreover, as the operating frequency increases, the re-ignition and extinction peaks disappear, resulting in a longer lamp lifetime. The load characteristics of an HID lamp can be represented as a pure resistor and the lamp power factor approaches unity. There is no flickering effect and the stroboscopic effect in the light output can be improved, as can the light lumens. However, the operation of high-pressure HID lamps with high-frequency current waveforms is hampered by the occurrence of acoustic resonances (AR), which was first reported by Campbell [11].

The common explanation of acoustic resonance is that the periodic power input causes pressure fluctuation in the gas volume of the HID lamp. If the power frequency is at or close to the eigenfrequency of the lamp, traveling pressure waves will appear. These waves travel towards and reflect on the tube wall, resulting in standing waves with large amplitudes. This phenomenon may lead to visible arc distortions, as shown in Figure 1-2, resulting in fluctuation
of the light, variation of the color temperature, decreased lamp life time and, in some cases, cracking of the discharge tubes.

![Image of lamp arc distortion due to AR: (a) normal arc (b) distorted arc under AR.]

Lamp eigenfrequencies depend on arc vessel geometry, gas filling and gas thermodynamic state variables, such as temperature, pressure and gas density, and so on [12-14]. Acoustic resonance is more likely to occur in lamps with a spherical shape or aspherical tube end than in lamps with flat ends or narrow and cylindrical arc tubes. Small spherical-shape lamps usually have broad bands of acoustic resonance frequencies. Moreover, since the thermodynamic state variables change with lamp age, the acoustic resonance bands will change with the lamp age as well.

The existence of acoustic resonance during high-frequency operation is a major challenge to the ballast circuit designers.

In terms of energy, acoustic resonance is actually caused by the following two factors: 1) the lamp frequency is within acoustic resonance frequency band; 2) the high-frequency energy applied to the lamp is larger than the threshold energy required to excite acoustic resonance.

Besides the lamp-related method, a lot of ballast circuit topologies and control methods have been proposed to avoid acoustic resonance, which can be classified as the following categories:
1. HID lamp is operated in non-AR frequency range.

   Acoustic resonance usually occurs from several kilohertz to several hundred kilohertz, and there are several scattered AR-free frequency bands within the range, as shown in Figure 1-3.

   ![Figure 1-3. Typical acoustic resonance frequency band.](image)

   S. Wada proposed a DC-type ballast [15] to avoid alternating energy and thus avoid acoustic resonance, however; however, DC operation causes etching and asymmetrical eroding of electrode due to the cataphoretic effect, which reduces lamp life.

   Other than DC operation, the lamp can be operated in predetermined AR-free frequency zones [16], as shown in Figure 1-3. However, since the AR-free zone is strongly dependent on lamp tube geometry and thermodynamic state variables, which vary from lamp to lamp, it is very difficult to select an appropriate operation frequency for a lamp.

   R. Redl proposed ultra-high-frequency ballast [17] to avoid AR, which refers to the operation above the maximum acoustic resonance frequency. When the time constant of the plasma parameter is much longer than the time constant of the supply power, the discharge path will behave like a dc-driven arc due to thermal hysteresis. However, the lowest frequency above which AR can be prevented needs to be pre-determined, and high-frequency lamp operation causes high EMI noise and high power losses.

2. Reduce high frequency input energy to below the threshold of acoustic resonance.
Modulation of the switching frequency or phase angle [18-21] will expand the spectrum of lamp power and lower the magnitude of the input energy in a certain frequency range. Sufficiently low amplitude of the power spectrum is required to eliminate acoustic resonance. This requires a wider bandwidth, which will cause uneven light spectral distribution and excite acoustic resonance in other acoustic resonant frequency zones. Additionally, since the AR frequency and threshold energy varies with the lamp parameters, it is quite difficult to determine the resonance frequency windows. How to adjust the frequency over a broad resonance frequency range without causing serious arc fluctuation is still unclear.

3. Square-wave current driving.

Ideally, square-wave operation can distribute lamp power spectrum in a theoretically infinite number of harmonics. It can also be explain in another way. Since the lamp voltage and lamp current are both square wave and in phase, the power supplied to the lamp remains constant; thus the plasma temperature remains constant.

The low-frequency square wave (LFSW) current-driving method [22] can effectively eliminate acoustic resonance, and has been widely used in commercial HID ballast products. However, an extra-low-frequency square wave inverter is required, which results in relatively complicated system structure and extra size, weight and cost.

![Figure 1-4. Low-frequency square wave current-driving method to avoid acoustic resonance.](image)
Ideally, the high-frequency square wave (HFSW) current-driving method [23-26] also provides a flat instantaneous lamp power to avoid AR, as shown in Figure 1-5. However, due to parasitic effects, there is still high-frequency energy provided to the lamp, as shown in Figure 1-5, which still could cause acoustic resonance.

Figure 1-5. High-frequency square wave current-driving to avoid AR [23 M. Ponce, et al, “Electronic ballast for HID lamps with high frequency square waveform to avoid acoustic resonances”, IEEE APEC 2001, pp. 658-663.]: (a) circuit topology, (b) voltage, current and instantaneous power in ideal case, (c) voltage, current and instantaneous power in real case.

Among all the above methods, the low-frequency square wave current-driving method has been proved to be the most effective method to eliminate AR, and it has been successively adopted in commercial products.

1.2.5. Other requirements for HID ballast

Other than the basic current-stabilizing, ignition, and AR-free requirements, there are many other challenges for HID ballasts.

Lighting equipment is usually in a high demand. At homes and offices, from 20% to 50% of the total energy consumed is due to lighting. In order to meet energy saving and “green energy” trends to save electricity costs and prevent harmonic currents from polluting the public supply
system, the HID ballast must have power factor correction (PFC) function to comply with international input harmonic current standards, such as the IEC 61000-3-2 standard [27]. The IEC 6100-3-2 standard specifies limits of harmonic current emissions applicable for electrical and electronic equipments that have an input current up to 16A per phase, and are intended to be connected to public low-voltage distribution systems. Originally this standard does not set the limit for power system with 120V line-to-neutral voltage in United States. Many offline converters need to deal with universal line input voltage from 95V to 265V. Even for products with a narrow input voltage range, a high power factor and low input harmonic current are still important specifications that make the product more competitive and have the potential to expand the market worldwide.

For electrical and electronic equipment other than lighting devices, the IEC 61000-3-2 standard is only applicable for equipment with a rated power of more than 75W. For lighting equipment, there are more stringent requirements.

For lighting equipment having an input power greater than 25W, the harmonic currents cannot exceed the relative limits given in Table 1-1. For lighting equipments having an input power smaller than or equal to 25W, one of the following two sets of requirements should be considered:

1) The harmonic currents shall not exceed the power related limits for Class D equipment, as shown in Table 1-2. (Column 2: Maximum permissible harmonic current per watt)

2) The third harmonic current, expressed as a percentage of the fundamental current, shall not exceed 86%, and the fifth shall not exceed 61%; moreover, the waveform of the input current shall be such that it begins to flow before or at 60°, has its last peak before or at
65°, and does not stop flowing before 90°, where the zero-crossing of the fundamental supply voltage is assumed to be at 0°.

### Table 1-1 IEC 61000-3-2 limits for Class C equipment: lighting equipments.

<table>
<thead>
<tr>
<th>Harmonic order (n)</th>
<th>Maximum permissible harmonic current expressed as a percentage of input current at the fundamental frequency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>30 · (\lambda) ((\lambda) is the circuit power factor)</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>9</td>
<td>5</td>
</tr>
<tr>
<td>11 ≤ n ≤ 39</td>
<td>3</td>
</tr>
</tbody>
</table>

### Table 1-2 IEC 61000-3-2 limits for Class D equipments.

<table>
<thead>
<tr>
<th>Harmonic order (n)</th>
<th>Maximum permissible harmonic current per watt (mA/W)</th>
<th>Maximum permissible harmonic current (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>3.4</td>
<td>2.30</td>
</tr>
<tr>
<td>5</td>
<td>1.9</td>
<td>1.14</td>
</tr>
<tr>
<td>7</td>
<td>1.0</td>
<td>0.77</td>
</tr>
<tr>
<td>9</td>
<td>0.5</td>
<td>0.40</td>
</tr>
<tr>
<td>11</td>
<td>0.35</td>
<td>0.33</td>
</tr>
<tr>
<td>13</td>
<td>0.296</td>
<td>0.21</td>
</tr>
<tr>
<td>13 ≤ n ≤ 39</td>
<td>3.85/n</td>
<td>2.25/n</td>
</tr>
</tbody>
</table>

(odd harmonics only)

Other than the input line regulation, the electronic ballast of an HID lamp usually requires a constant lamp power control during the lamp’s lifetime to maximize the lamp life. Since the HID lamp has very high efficacy and a compact size, the ballast also needs to have high efficiency and a small size.
1.3. Motivations and Challenges for Compact HID Ballast

1.3.1. Motivations for developing compact HID (CHID) lamp

Regardless of the advantages of HID lamps as high-quality lighting sources, the utilization of HID lamps in low-power application is limited by the high initial cost of both lamps and ballasts. HID lamps are rarely used in residential applications.

To take track lighting as an example, the major two competitors in this application are halogen lamps and HID lamps. HID lamps have much higher luminous efficacy (one 20W HID lamp can provide the same lumens as one 70W halogen lamp), and much longer lamp lifetime (up to 12000 Hours) than a halogen lamp (up to 4000 Hours). However, HID lamps make up less than 20% of the total market for track lighting, while halogen lamps make up around 70% of the market. The major reason for this is that halogen lamps are basically incandescent lamps, so they don’t need ballasts, while HID lamps need expensive ballasts, and additional space is needed for the ballast. It takes around four years for the energy savings and lower maintenance costs of an HID lamp to offset the high initial cost.

Therefore, developing cost-effective, high density electronic ballasts with high performance by using advanced high-frequency electronic ballasting techniques is the key to promoting the utilization of HID lamps.

In electrical lighting history, there have been several successive inventions which have changed people’s lives. The compact fluorescent lamp (CFL) is one of them. Figure 1-6 shows a picture of a CFL, where the electronic ballast is built inside the lamp fixture and can be directly plugged in the socket used for an incandescent lamp. CFLs have been widely used and are going to replace the incandescent lamps in residential applications.
Figure 1-6. Compact fluorescent lamp with built-in ballast.

Figure 1-7 shows an example of the circuit topology widely used in CFL commercial products. A self-oscillating half-bridge series resonant circuit is used to drive the fluorescent lamp. To maintain low cost, only one capacitor is used for power factor correction.

The objective of this work is to adopt the same concept as the CFL, and build the HID ballast inside the lamp fixture, as shown in Figure 1-8; making a compact HID (CHID) lamp possible.
1.3.2. Challenges for CHID ballast

Why can’t the simple and low cost CFL topology be used for HID lamps? The major reason is the acoustic resonance and higher ignition voltage requirement. Figure 1-9 [46] and Figure 1-10 [50] shows examples of start-up profiles of an FL and an HID lamp, respectively.

![FL Start-up profile](image)

**Figure 1-9.** FL Start-up profile [46 J. Qian, “Advanced Single-Stage Power Factor Correction Techniques”, Ph.D Dissertation, Virginia Polytechnic Institute and State University, September 1997].
Since the fluorescent lamp doesn’t have acoustic resonance, the FL ballast can use high-frequency ac current to drive the lamp. However, for the HID lamp, an additional low-frequency inverter stage is needed to avoid acoustic resonance, which adds to the circuit complexity, the component count, size and cost. As for the ignition voltage requirement, a fluorescent lamp usually requires 400V-600V ignition voltage, so a series-resonant parallel-loaded circuit is usually used for the ignitor. Before the lamp is ignited, the lamp impedance is very large, so the high-Q series-resonance will generate a high resonant voltage across the resonant capacitor and the lamp. After the lamp is ignited, the lamp impedance drops dramatically, the Q factor reduces accordingly, and the voltage across the lamp is reduced as well. However, the HID lamp requires a much higher ignition voltage, i.e., 1kV to 5kV for a cold strike, and around 20KV for a hot

Figure 1-10. HID lamp start-up profile [50 Y. Hu, “Analysis and Design of High-Intensity-Discharge Lamp Ballast for Automotive Headlamp,” Master thesis, Virginia Polytechnic Institute and State University, November 2001].
strike. To achieve such a high voltage, an additional transformer or other circuitry is needed to further boost the voltage.

Other challenges for the implementation of the CHID lamp come from the stringent power factor and input current harmonic requirements, which require a specific high-frequency converter to implement the power factor correction function, which also adds to the system size and cost.

1.4. Dissertation Outlines

This dissertation consists of six chapters. The first chapter serves as an introduction to the scope of the project. The rest of this dissertation is organized as follows.

In Chapter 2, the system structure and topology of the ballast for low-wattage HID ballasts is investigated with the goals of achieving high power density and high performance. A two-stage structure is proposed, which includes a single-stage PFC AC/DC front-end with constant power regulation, and a non-regulated DC/AC square-wave inverter integrated with the ignitor function. This chapter includes detailed analysis, detailed design of the circuit, and experimental results.

In order to further increase the power density, integration and packaging strategies are investigated in Chapter 3. System partitioning and appropriate integration technologies are discussed. Passive integration and a three-dimensional package strategy are two key points of the integrated HID ballast. Design and implementation of major integrated passive components, such as the integrated ignitor and integrated EMI filter, are explored. Experimental verification of the integrated ballast is provided.

Chapter 4 is focused on thermal analysis and management of the integrated ballast. By installing the ultra-compact HID ballast inside the lamp fixture, the ambient temperature for the
ballast will be much higher than the conventional separately installed ballast; combined with a reduced size; the thermal condition for the integrated ballast will be much more severe. A thermal simulation model of the integrated ballast is built in the IDEAS simulation tool, and appropriate thermal management methods are proposed and investigated in the IDEAS simulation model. Experimental verification of various thermal management methods is provided. Based on the thermal management study, a new integrated ballast with an improved thermal design is proposed.

Chapter 5 summarizes the work done in the dissertation and suggests topics for future work.
Chapter 2. High Density HID Ballast Topology Study, Design and Implementation

2.1. System Structure of the HID Ballast

The basic function of the HID ballast is to provide a high voltage to initiate the lamp arc and provide appropriate power regulation to stabilize the HID lamp operation. From the lamp performance point of view, a low-frequency square-wave current/voltage driving method is preferred to avoid acoustic resonance. A HID ballast structure with four function blocks is shown in Figure 2-1. The AC/DC power factor correction (PFC) stage changes the AC line voltage into a constant DC bus, and provides a high input power factor (PF) and small input harmonic currents in order to meet the IEC 61000-3-2 Class C requirement for lighting equipments. The DC/DC stage is a high-frequency converter that steps down the DC bus voltage and provides power regulation for the lamp. The DC/AC inverter provides a low-frequency AC square-wave lamp current, which is essential for avoiding acoustic resonance in HID lamps. The ignitor delivers a proper ignition voltage for starting the discharge in the HID lamp. After ignition, the ignitor has to stop producing high voltage ignition peaks.

Figure 2-1. HID ballast with four function blocks.
In order to simplify the ballast circuit, the ignitor is combined with the inverter and results in a three-stage HID ballast as shown in Figure 2-2. A typical three-stage HID ballast circuit diagram is shown in Figure 2-3. The PFC stage is a conventional boost converter that operates at the boundary (BCM) between the continuous-current mode (CCM) and the discontinuous-current mode (DCM). The switch’s on-time is controlled to achieve a constant DC bus voltage and high PF. A Buck DC/DC converter steps down the PFC output voltage and provides constant output power control, and voltage and current limiting during the start and warm-up period. A full-bridge square-wave inverter switches the lamp voltage/current polarity alternatively at a frequency of 200~400Hz to avoid acoustic resonance. During the igniton mode, inductor $L_r$, capacitor $C_r$ and the lamp form a parallel-loaded series-resonant tank. Four switches in the inverter stage operate at high frequency, sweeping from 100kHz to 200kHz. The 3rd order harmonic of the 100kHz~200kHz square wave voltage is very close to the resonance frequency between $L_r$ and $C_r$, which is around 450kHz, so high voltage will be generated across the capacitor and the lamp. After the lamp is ignited, the switches will operate at 400Hz. Inductor $L_r$ is saturated and is considered short-circuited, but the current going through it is controlled by the DC/DC stage. Capacitor $C_r$ can be considered open-circuit under such low frequency condition.

![Figure 2-2. A three-stage HID ballast.](image-url)
As discussed in Chapter 1, compact size and low cost are two major targets for the HID lamp ballast, especially in low power applications. However, the three-stage approach usually has a large component count and complicated control circuitry, resulting in a potentially large size and high cost. In order to increase the power density and reduce the cost, a two-stage approach, which combines the DC/DC power-regulation stage and the inverter into one stage, is proposed in other works [28-31].

Figure 2-4 shows a typical circuit configuration for this two-stage approach [28]. It consists of a BCM boost PFC AC/DC stage followed by a full-bridge buck converter. The full-bridge buck converter combines the buck power-regulation stage with the full-bridge inverter stage. Two switches (S₂ and S₃) operate at high frequencies to regulate the lamp power, and the other two switches (S₄ and S₅) operate at low frequencies to provide the lamp voltage/current polarity change.
Figure 2-4. A two-stage HID ballast: combining DC/DC and DC/AC inverter: (a) system block diagram, (b) circuit configuration, (c) gate signal and lamp voltage waveform.

Other circuit implementations are also proposed in [29, 30, 31] as shown in Figure 2-5, which basically explore the same concept of combining the DC/DC stage with the inverter stage to save components. Compared with the three-stage structure, one MOSFET and its controller are saved; however, there are still three MOSFETs operating at high frequencies, and two of them (S₂ and S₃) are hard-switching devices, which impedes the pursuit of a higher frequency to reduce the passive component size. Because the boost converter cannot control the inrush current at start-up, an additional MOSFET and a power resistor are needed for soft starting. For the full-bridge buck converter stage, the lamp power regulation requires that the lamp voltage and current be sensed. Because the lamp voltage and current are low-frequency AC signals,
sensing and power-computing circuit is complicated. The PWM control of the four switches also adds the complexity of the pulse-distributing circuit.

![Diagram of Boost PFC stage and two-stage HID ballast](image)

(a)

![Diagram of another two-stage structur e](image)

(b)


To overcome the limitations mentioned before, another two-stage structure is considered, as shown in Figure 2-6, which combines the PFC AC/DC stage and DC/DC stage into a single-stage PFC (SSPFC) AC/DC front end. The DC/AC stage is just an unregulated inverter used to transfer the DC-link current/voltage to a low-frequency square wave current/voltage, both PFC and lamp power regulation are accomplished in the SSPFC AC/DC front end.
The single-stage single-switch PFC (S$^4$PFC) converters [32-45] are widely used in low-power applications because of their low component count, low cost and simply control. Usually a DCM boost or flyback converter is used as the PFC semi-stage to share the switch with the DC/DC semi-stage, to simultaneously achieve inherent PFC and output regulation. Only one switch in the S$^2$PFC front end operates at a high frequency; thus the potential exists to operate at a higher frequency in order to reduce the passive component size. Additionally, since the DC/AC stage is unregulated, the lamp power signal can be sensed at the DC output of the SSPFC front end, which simplifies the control circuit. Therefore, this structure can be a high-power-density, low-cost solution for the low-power lamp ballast. First of all, a suitable high-frequency SSPFC AC/DC topology is needed to implement this front end.

As for a 20-watt HID ballast, the input RMS current is small. The DCM operation is preferred to simplify the control circuit. The S$^4$PFC converter is also preferred. According to the different load characteristics of HID lamp ballasts with traditional AC/DC converters, the following aspects need to be considered in this SSPFC AC/DC front end:

1) The HID lamp ballast does not need a fast output-voltage regulation, but needs a constant output-power regulation at the steady state, a constant voltage regulation before ignition, and a constant current regulation during the start-up time.
2) Because lamp impedance changes dynamically from open circuit to almost short circuit and then increases until it reaches a steady state, a high bulky capacitor voltage stress should be avoided for all operation modes.

3) High Power Factor and small input-current harmonics are required. In this dissertation, input PF should be higher than 90%, and the input current harmonics should meet IEC 61000-3-2 Class C standards, and input current THD should be lower than 10% with an input line voltage within 120V±10%.

According to the requirements mentioned above, an investigation of the different topologies of S\textsuperscript{4}PFC converters is provided in the following part to find a suitable SSPFC AC/DC converter for this particular application.

### 2.2. Investigation of SSPFC AC/DC Front-End Topology

A number of SSPFC AC/DC converters have been introduced recently [32-45]. In a typical single-stage approach, the PFC and the high-bandwidth output control are performed in a single control chip, and an internal energy-storage capacitor is employed to handle the difference between the instantaneous input power and output power. Among these SSPFC converters, single-stage single-switch PFC (S\textsuperscript{4}PFC) converters are particularly attractive from the cost point of view, because only one semiconductor switch and one simple control circuit are used. The main stream of the S\textsuperscript{4}PFC converter is based on the two-cascade-stage PFC converter. It integrates the PFC stage and the DC/DC stage with a shared switch and its controller, as shown in Figure 2-7. Because the PFC semi-stage and the DC/DC semi-stage share a common switch, only one control variable can be controlled, since the output voltage is required to be regulated. It is required that the PFC semi-stage has an inherent PFC function. It is well known that a DCM
boost or Flyback converter can draw a near sinusoidal input current with a constant on-time control during a half line period. Therefore, a DCM boost or flyback integrated with a DC/DC converter is able to achieve PFC and output regulation simultaneously with a simple control.

![Conceptual diagram of Single stage PFC converter.](image)

Based on the position of the energy-storage capacitor in the path of energy flow, there are two types of topology. One approach is to place the capacitor in the series path of energy flow, such as BIFRED and BIBRED [32-36]. The other is to place the capacitor in the parallel path of energy flow [37-45]. Both approaches will be discussed with representative topologies respectively.

### 2.2.1. Comparison of two types of SSPFC topologies

#### A. Capacitor in the series path of energy flow

BIFRED and BIBRED are initiated in reference [32], where a family of SSPFC converters is proposed using a cascade method. These converters are derived by the integration of a DCM boost rectifier, energy storage capacitor and a cascaded DC/DC converter. BIFRED/BIBRED is resulted from integrating a DCM boost rectifier with a flyback/buck DC/DC converter as shown in Figure 2-8.
Figure 2-8. S$^4$PFC converters with capacitor in the series path of energy flow [32 M. Madigan, et al, “Integrated high quality rectifier-regulators”, IEEE PESC 1992, pp.1043-1051]: (a) BIFRED, (b) BIBRED.

In order to achieve low harmonic distortions in the input current, $L_1$ must operate in DCM. The flyback semi-stage operates in CCM to reduce the current stresses.

The output voltage is proportional to the duty cycle as expressed in Eq. (2-1).

\[
\frac{V_{2c}}{V_{g,rms}} = \frac{\sqrt{2}}{2} \frac{D_{10}}{n} \left( 1 + \sqrt{4A_0 \frac{n^2}{K_1}} \right), \quad A_0 = 0.426, \quad K_1 = \frac{2L_1}{RT_s}
\]  

(2-1)

The line input current is also a function of the duty cycle as shown in Eq. (2-2).

\[
i_l = \frac{1}{R_c} \left( V_g + \frac{V_g^2}{V_1 + nV_2 - V_g} \right), \quad R_c = \frac{2L_i}{D_1^2 T_s}
\]  

(2-2)

Thus duty cycle can be used to control output voltage/power or line input current. Since DCM boost can automatically draw a near sinusoidal input current if its switch on-time is held relatively constant during a half line period, a simple duty cycle controller can be used to regulate the output voltage/power, without active control of the line input current.

There are two drawbacks of this type of SSPFC converter.

1) Relatively high input current THD
When a simple duty cycle control is employed to regulate the output, with no active control of the input current, the shape of the peak input current is nearly proportional to the line input voltage, but the average of the input current may have a certain distortion, so the total harmonic distortion is relatively high compared to the two-stage approach. What’s more, during the switch off-time, the load absorbs energy not only from the magnetizing inductor of the transformer but also from the line input until the input current decreases to zero. Therefore, part of the input power is directly transferred to the load. As a result, with constant frequency and constant duty cycle in a half line period, this part of power is proportional to the square of the line input voltage, adding to the output ripple of the output voltage. With tight output regulation requirements, PFC function will be sacrificed and the input current THD will increase. The input current THD in a BIRFED converter reaches 21.4% [32].

A more sophisticated control scheme using both duty cycle and switching frequency control can further reduce the line current harmonics [32]. However an analog multiplier and a voltage controlled oscillator is added and hence the complexity of the controller and the cost increases.

2) High bulky capacitor voltage stress

In both BIFRED and BIBRED converters, the energy-storage capacitor should handle the difference between the instantaneous varying input power and output power. If the DC/DC stage operates in CCM and PFC stage operates in DCM to achieve PFC, then there will be a high DC bus voltage stress at light load. This is the major issue of the BIFRED and BIBRED converter. Figure 2-9 shows the relationship between the input power and the duty cycle of PFC stage, and between the output power and the duty cycle of DC/DC stage [36].
Figure 2-9. Relationship between the input/output power and the duty cycle [36 J. Qian, et al, “Single-stage single-switch power factor correction AC-DC converters with DC bus voltage feedback for universal line applications”, in IEEE Trans. Power Electronics, vol 13, pp.1079-1088, Nov.1998]: (a) DCM PFC + CCM DC/DC, (b) DCM PFC + DCM DC/DC.

If DC/DC stage operates in CCM, when the load becomes light, which means output power decreases, the duty cycle doesn’t change immediately because of the CCM operation of the DC/DC stage. From Figure 2-9 (a), the input power stays the same as that of the heavy load. The unbalanced power between the input and output should be stored in the energy storage capacitor, resulting in an increase of the bulky capacitor voltage. To keep the same output voltage, the voltage feedback works to decrease the duty cycle. As a result, the input power decreases correspondingly. This dynamic process will not stop until the new power equilibrium is built. It is obvious that the power balance at light load and high line is reached at the penalty of a significant bulky capacitor voltage stress. It could reach 1000V for universal line input application. It is impractical for the converter with such a high bulky capacitor voltage.
If both the PFC stage and the DC/DC stage operate in DCM, the duty cycle decreases when
the load becomes light, and the input power decreases accordingly. Therefore, there is no
unbalanced power between input and output, that is, the bulky capacitor voltage is independent
on the load. However, the DCM operation of the DC/DC stage will increase the current stress,
thus conduction loss will increase, and consequently decrease the efficiency. Approaches to
reduce bulky capacitor voltage stress are summarized as follows.

1) DCM operation of the DC/DC stage

   As discussed before, when both PFC and DC/DC stage operate in DCM, the bulky capacitor
   voltage is independent on the load [32][33][36]. Generally, for high-power applications, the
   CCM operation of the DC/DC stage is preferred in order to reduce the current stress. For low-
   power applications, the RMS current is relatively small, and conduction loss is not significant.
   DCM operation of the DC/DC stage is preferred to simplify the control circuit.

2) Variable frequency control

   Milan proposed a variable frequency control to reduce the bulky capacitor voltage stress as
   shown in Figure 2-10 [34]. Since the gain of the CCM DC/DC stage depends only on the duty
   cycle, and the gain of DCM boost depends on the frequency, it is possible to regulate the bulky
   capacitor voltage by a variable frequency control, without affecting the output. Figure 2-11 shows
   the frequency range required to regulate the capacitor voltage to a desired regulation voltage. A
   very wide range frequency is required to achieve a reasonable bulky capacitor voltage, which is
   undesirable for the magnetic component design. Efficiency will also suffer.
Figure 2-10. Circuit diagram of a variable-frequency control [34 M. M. Jovanovic, et al, “Reduction of voltage stress in integrated high-quality rectifier-regulators by variable frequency control”, IEEE APEC 1994, pp.569-575].

Figure 2-11. Switching frequency as function of output current for different bus voltage [34 M. M. Jovanovic, et al, “Reduction of voltage stress in integrated high-quality rectifier-regulators by variable frequency control”, IEEE APEC 1994, pp.569-575].

3) Bulky capacitor voltage feedback control

Another way to suppress the bulky capacitor voltage is to use a negative feedback scheme in the power stage instead of in the control loop [36]. If the PFC stage is inherently able to reduce the input power automatically when the load becomes light, then the bulky capacitor voltage can be suppressed. Since the input power is controlled by the duty cycle, Li, and the
voltage across $L_i$, we can reduce the voltage across $L_i$ during the switch on-time at light load in order to reduce the input power. One implementation is to insert a voltage source $v_f$ in series with the inductor $L_i$, as shown in Figure 2-12. The amplitude of $v_f$ should be proportional to the DC bus voltage. Thus the voltage across $L_i$ is the rectified line input voltage minus the feedback DC bus voltage during the switch on time. This negative feedback signal can be easily obtained by employing a feedback winding coupled with the transformer as shown in Figure 2-12. By properly designing the turn’s ratio between the primary winding $N_1$ and the feedback winding $N_2$, a suitable bulky capacitor voltage can be obtained.

Figure 2-12. Integrated PFC converter with power stage negative feedback [36 J. Qian, et al, “Single-stage single-switch power factor correction AC-DC converters with DC bus voltage feedback for universal line applications”, in IEEE Trans. Power Electronics, vol 13, pp.1079-1088, Nov.1998]: (a) conceptual diagram, (b) implementation by adding coupled winding.
However, the feedback winding also produces a dead time in the input current, as shown in Figure 2-13. There is no input current near the zero crossing of the line input voltage because the feedback voltage is higher than the rectified line input voltage. As a result, input current THD is increased. The higher the feedback voltage is, the higher the input current distortion. If $N_2=N_1$, there is no PFC function, and there is no bus voltage stress at any load condition. Besides, the main switch deals only with the current of the DC/DC stage, thus has minimal current stress. If $N_2=0$, the converter becomes the BIFRED converter and a relatively low THD can be achieved. However, the converter suffers from high DC bus voltage stress at light load. The main switch has to handle the currents of both stages, and has a maximum current stress. Therefore there is a trade-off among the bulky capacitor voltage, switch current stress, input current distortion (THD) and output voltage ripple.

![Figure 2-13. Input current waveform and the input current THD as a function of $N_2$](image)


B. Capacitor in the parallel path of energy flow

SSPFC converters can also be implemented by the integration of a PFC stage and a DC/DC stage with an energy storage capacitor in the parallel path of energy flow [37-46]. Figure 2-14
shows some representative $S^4$PFC topologies of this type. Figure 2-14 (a), (b) are the integration of a boost PFC cell with a flyback and forward DC/DC converter respectively, and Figure 2-14(c) is the integration of a flyback PFC cell and a flyback DC/DC converter.

![Diagram](image)

Figure 2-14. Some representative $S^4$PFC topologies with capacitor in the parallel path of energy flow
(a) boost + flyback [37 R. Redl, et al, “A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage”, in Proc. IEEE PESC 1994, pp.1137-1144], (b) boost + forward [37], (c) flyback + flyback [46 J. Qian, “Advanced Single-Stage Power Factor Correction Techniques”, Ph.D Dissertation, Virginia Polytechnic Institute and State University, September 1997].

Based on the analysis, when the PFC stage operates in DCM, while the DC/DC stage can operates in either CCM or DCM, the PFC function and fast output regulation can be achieved simultaneously no matter whether the energy storage capacitor is in the series or the parallel path.
of the energy flow. The second family of topology also suffers from the high DC bus voltage stress at high line and light load, when the DC/DC stage operates in CCM. The difference between the two groups is: when the energy storage capacitor is in the series path of energy flow, there is a part of the input power being directly transferred to the load during the switch off-time without being processed by the switch. This part of directly transferred power will increase the low frequency ripple of the output voltage or increase the input current harmonics distortion or increase the control complexity according to different control schemes. When the capacitor is in the parallel path of the energy flow, there is no input power being transferred directly to the load. Lower output voltage ripple or lower input current THD can be achieved. Therefore the second group of SSPFC topologies represents the main stream. And most of the literature focuses on how to reduce the high DC bus voltage at high line and light load when the DC/DC stage operates in CCM. Similar to the first group of the circuit, three approaches can be utilized to reduce the DC bus voltage: a) DCM PFC + DCM DC/DC; b) DCM PFC + CCM DC/DC with a variable frequency control; c) Bulky capacitor voltage feedback control.

These approaches can be implemented similarly to the first group of $S^4$PFC converters, and same issues apply. Figure 2-15 shows some topologies using DC bus feedback control [36][38][39]. In Figure 2-15 (a) [38], the bus voltage feedback control is implemented by the winding $N_2$ during the switch on-time. In Figure 2-15 (b) [39], the voltage feedback control is achieved by the winding $N_2$ during switch on-time, and by the winding $N_4$ during the switch off-time, respectively.

2.2.2. Summary

Table 2-1 summarizes the comparison between different types of the SSPFC converters discussed above, in terms of input current THD, bulky capacitor voltage stress, switch current stress, and control complexity. From Table 2-1, it is obviously a better choice to place the energy storage capacitor in the parallel path of the energy flow to reduce the input current harmonics. In a low-wattage HID ballast application, DCM PFC + DCM DC/DC is the best choice to guarantee a low DC bus voltage with an acceptable current stress.

Considering the boost or flyback converter as the PFC stage, and the flyback or forward converter as the DC/DC stage, four topologies can be generated as the candidates for the AC/DC front-end of the HID ballast. Comparison among these four topologies is provided in Table 2-2 in terms of component count, input current THD, DC bus voltage, output voltage range, and soft start circuit.
As a PFC stage, the flyback topology is better than the boost topology because the flyback PFC can achieve unity PF and very low input current THD; soft-start function can be achieved by PWM control in the flyback PFC circuit with no need of additional soft-start circuit; the bulky capacitor voltage is controlled by the duty cycle and turn’s ratio of flyback transformer. So it can be lower than the line peak voltage.

As a DC/DC stage, the flyback topology is better than the forward topology because flyback converter has less component count, and can both step-down and step-out at different load condition, which is very important in the HID ballast. During ignition mode, high ignition voltage (several kV) is required to ignite the lamp, therefore high voltage and enough energy is needed to feed the ignitor circuit.

As a result, DCM flyback PFC + DCM flyback DC/DC is selected for the AC/DC front-end of low wattage electronic ballast for HID lamps. Further simplification and modification of the circuit topology according to the application is discussed in the following part.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Operating mode (PFC + DC/DC)</th>
<th>THD</th>
<th>V_B</th>
<th>I_{sw}</th>
<th>Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>CB in the series path of energy flow</td>
<td>DCM + DCM</td>
<td>High</td>
<td>Low</td>
<td>High</td>
<td>Duty cycle &amp; frequency control</td>
</tr>
<tr>
<td></td>
<td>DCM + CCM</td>
<td>High</td>
<td>High</td>
<td>Low</td>
<td>Duty cycle &amp; frequency control</td>
</tr>
<tr>
<td>CB in the parallel path of energy flow</td>
<td>DCM + DCM</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>Duty cycle control at constant frequency</td>
</tr>
<tr>
<td></td>
<td>DCM + CCM</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
<td>Duty cycle control at constant frequency</td>
</tr>
</tbody>
</table>
Table 2-2. Comparison of different SSPFC topologies

<table>
<thead>
<tr>
<th>Topology</th>
<th>Comp. count</th>
<th>I_{THD}</th>
<th>Soft Start</th>
<th>Bulky cap voltage</th>
<th>Output voltage range</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>#S</td>
<td>#D</td>
<td>#L/T</td>
<td>#C</td>
<td></td>
</tr>
<tr>
<td>Boost + Flyback</td>
<td>1</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>High</td>
</tr>
<tr>
<td>Boost + Forward</td>
<td>1</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>High</td>
</tr>
<tr>
<td>Flyback + Flyback</td>
<td>1</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>Low</td>
</tr>
<tr>
<td>Flyback + Forward</td>
<td>1</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>Low</td>
</tr>
</tbody>
</table>

2.3. Proposed SSPFC Front-End for Low-Wattage HID Ballast

2.3.1. Proposed SSPFC front-end: topology simplification

Based on the above analysis, a DCM flyback PFC combined with a DCM flyback DC/DC [41] has been selected as the single-stage PFC front-end. Since there is no isolation requirement
in the electronic ballast application, the flyback DC/DC stage is replaced by its non-isolated equivalent circuit, buck-boost converter. The circuit is then modified to a DCM flyback PFC stage integrated with a DCM buck-boost DC/DC stage as the single-stage PFC front-end for the HID ballast. Figure 2-16 shows the power stage of the proposed single-stage PFC AC/DC front-end. The flyback PFC semi-stage and the buck-boost DC/DC semi-stage share the same switch, and both stages operate at DCM.

Figure 2-16. Proposed SSPFC AC/DC front end: DCM flyback + DCM buck-boost.

2.3.2. Operating principle and design of proposed SSPFC AC/DC front-end

2.3.2.1. Operating principle of the proposed SSPFC AC/DC front-end

Assuming the turn’s ratio of the coupled inductor L1 is 1: 1. Figure 2-17 shows equivalent circuits under different operation modes over one switching cycle in a steady state, and key waveforms are shown in Figure 2-18.
Figure 2-17. Operation modes of proposed SSPFC AC/DC stage: (a) M1 \([t_0, t_1]\), (b) M2 \([t_1, t_2]\) and (c) M3 \([t_2, t_3]\).
M1 \([t_0, t_1] \): Before \(t_0\), all the inductor currents are zero because of the DCM operation. At \(t_0\), switch \(S\) turns on. Switch current consists of the current through \(L_{1a}\) and the current through \(L_2\). Both of them are charged linearly.

M2 \([t_1, t_2] \): At \(t_1\), switch \(S\) turns off. Due to the coupled-inductor effect, the energy stored in \(L_{1a}\) is transferred to \(L_{1b}\), which charges the bulk capacitor \(C_b\). Meanwhile, the energy stored in \(L_2\) is transferred to the load during this time interval. The currents through \(L_{1b}\) and \(L_2\) decrease linearly. Figure 2-17 shows a special case in which the currents through \(L_{1b}\) and \(L_2\) simultaneously decrease to zero. More typically, when the line-input and output voltages are different, one of them will go to zero before the other.

M3 \([t_2, t_3] \): At \(t_2\), the currents through \(L_{1b}\) and \(L_2\) decrease to zero, and the output power is only provided by the output capacitor.

Figure 2-18. Key waveforms within one switching cycle.
Therefore, the input power is transferred through $L_{1a}$-$L_{1b}$-$C_b$-$L_2$ to the load. If both $L_1$ and $L_2$ operate in DCM, then the output energy equals the energy stored in $L_{1a}$ during the switch on-time. The output power can be expressed as:

$$P_o = \frac{1}{T} \int_0^T \frac{1}{2} L_{1a} \left( \frac{V_p \sin(\omega t)}{L_{1a}} \right)^2 DT_s = \frac{V_p^2 D^2}{4L_{1a} f_s} \tag{2-3}$$

where $V_p = \sqrt{2V_{in}}$, $T$ is the AC line period, $D$ is the duty cycle, and $f_s$ is the switching frequency. Eq. (2-3) shows that a constant switching frequency and a constant duty cycle allow a constant output power to be achieved, which is the desired characteristic for HID ballast. For the DCM flyback semi-stage, a constant switching frequency and constant duty cycle results in unity PF and very low THD in the input current.

Based on the energy balance on bulk capacitor $C_b$ and the volt-second balance of $L_1$, the bulk capacitor voltage can be expressed as:

$$V_b = \sqrt{\frac{L_2}{L_{1a}}} V_{in} = \sqrt{\frac{L_2}{2L_{1a}}} V_p \tag{2-4}$$

Therefore, if both $L_1$ and $L_2$ operate in DCM, the bulk capacitor voltage is only dependent upon the ratio of the two inductances and the line-input voltage, and it can be designed to be lower than the input peak voltage.

There are several advantages of this topology for the low wattage HID ballast:

For SSPFC stage:

(1) No soft start switch and resistor.

(2) Constant frequency operation.
(3) Designable bulk cap voltage, can be lower than input peak voltage (<100V).

(4) Unity PF and very low THD.

For full-bridge inverter:

(1) Easy to sense lamp current and voltage.

(2) Mosfet voltage stress is low (<100V).

(3) No regulation is needed.

In general, compared with the previous two-stage ballast, only one active switch needs to be controlled. It will greatly simplify the control circuit. Since one switch operates at a high switching frequency, the circuit potentially can be pushed to a higher switching frequency to improve the power density.

2.3.2.2. Inductor design for DCM operation condition

The design procedure of the inductors $L_1$ and $L_2$ is provided to ensure the DCM operation for both inductors.

From Eq. (2-3), $L_1$ can be calculated as:

$$ L_{1a} = \frac{V_p^2 D^2}{4P_o f_s}. \quad (2-5) $$

In order to keep the DCM operation of $L_1$, based on the volt-second on the $L_1$, we have:

$$ V_p D = V_p D_1 \leq V_b (1 - D). \quad (2-6) $$

Combining Eqs. (2-5) and (2-6) yields that the minimum value for $L_2$ is:
\[ L_{2,\text{min}} = \left( \frac{D}{1 - D} \right)^2 \cdot 2L_{1a} = \left( \frac{D}{1 - D} \right)^2 \frac{V_p^2 D^2}{2P_o f_s} . \] (2-7)

In order to keep the DCM operation of \( L_2 \) at the minimum output voltage, based on the volt-second on the \( L_2 \), we have:

\[ V_{b} D = V_{o,\text{min}} D_2 \leq V_{o,\text{min}} (1 - D) . \] (2-8)

Combining Eqs. (2-5) and (2-8) yields that the maximum value for \( L_2 \) is:

\[ L_{2,\text{max}} = \frac{V_{o,\text{min}}}{V_p^2 D} \left( \frac{1}{D} - D_2 \right)^2 \cdot 2L_{1a} = \frac{V_{o,\text{min}}}{V_p^2 D} (1 - D)^2 \frac{V_p^2}{2P_o f_s} . \] (2-9)

From Eqs. (2-7) and (2-9), the critical duty cycle can be calculated as:

\[ D_{\text{crit}} = \frac{1}{1 + \sqrt{\frac{V_p}{V_{o,\text{min}}}}} . \] (2-10)

Given the input and output voltage, the critical duty cycle is then determined. In order to ensure DCM operation, the steady-state duty cycle should be smaller than the critical duty cycle. Given the duty cycle, output power and switching frequency, the inductance of \( L_{1a} \) can be calculated from Eq. (2-5), and inductance value of \( L_2 \) can be selected according to the range set by Eqs. (2-7) and (2-9). Figure 2-19 shows the inductor value curve as a function of duty cycle at 250 kHz switching frequency.
2.3.2.3. **Switching frequency selection: Loss analysis**

A higher switching frequency leads to a smaller size of magnetic components, but it also produces more switching loss. Therefore, careful loss analysis should be done to determine a proper switching frequency.

Basically the total losses in a converter include semiconductor conduction losses, inductor/transformer losses, switching losses and other frequency-independent fixed losses, such as control circuit losses. The semiconductor conduction losses here include MOSFET conduction loss and diode conduction loss. The inductor losses include the copper loss due to the resistance of the winding, and the core loss due to the hysteretic and eddy current loss in the magnetic core. The switching losses include MOSFET turn-on loss, turn-off loss, and other switching losses caused by device capacitance or leakage, package and stray inductances.
1) Conduction Loss $P_{\text{cond}} (P_{\text{cond}} = P_{\text{cond}_{\text{MOS}}} + P_{\text{cond}_{\text{Diode}}} + P_{\text{cond}_{\text{copp}}})$

During the conduction period, a MOSFET can be modeled as an on-resistance $R_{d\text{s(on)}}$ and a diode can be modeled as a voltage source $V_D$ plus an on-resistance $R_D$. A suitable model describing the inductor copper loss consists of an ideal inductor in series with a resistor $R_L$.

The conduction loss can be calculated as:

$$P_{\text{cond}} = P_{\text{cond}_{\text{MOS}}} + P_{\text{cond}_{\text{Diode}}} + P_{\text{cond}_{\text{copp}}}$$  \hspace{1cm} (2-11)

where:

$$P_{\text{cond}_{\text{MOS}}} = I_{S,\text{rms}}^2 R_{d\text{s(on)}}$$  \hspace{1cm} (2-12)

$$P_{\text{cond}_{\text{Diode}}} = I_{D,\text{ave}} V_D + I_{D,\text{rms}}^2 R_D$$  \hspace{1cm} (2-13)

$$P_{\text{cond}_{\text{copp}}} = I_{L,\text{rms}}^2 R_L$$  \hspace{1cm} (2-14)

From the waveforms shown in Figure 2-18, inductor and switch current peak can be calculated as follows.

$$I_{L1,\text{pk}}(t) = \frac{|V_{in}(t)|}{L_1} \frac{D}{f_s}, \quad V_{in}(t) = V_p \sin(\omega t)$$  \hspace{1cm} (2-15)

$$I_{L2,\text{pk}} = \frac{V_B}{L_2} \frac{D}{f_s}$$  \hspace{1cm} (2-16)

$$I_{S,\text{pk}}(t) = I_{L1,\text{pk}}(t) + I_{L2,\text{pk}}$$  \hspace{1cm} (2-17)

Because $|V_{in}(t)|$ is a rectified sinusoidal waveform, $I_{L1,\text{pk}}(t)$ is also a rectified sin wave, and $I_{S,\text{pk}}(t)$ is a dc value plus a rectified sinusoidal waveform. We should calculate the average and RMS value of these waveforms during the half line cycle.
\[ I_{s,\text{rms}} = \sqrt{\sum_{k=1}^{n(f_s)} \frac{1}{120} \cdot \left[ \frac{V_p}{L_1} \cdot \frac{D}{f_s} \cdot \sin(2\pi \cdot 60 \cdot \frac{k-1}{f_s}) + I_{L_2, \text{pk}} \right]^2}, \quad n(f_s) = \frac{f_s}{120} \]  
(2-18)

\[ I_{L_1,\text{rms}} = \sqrt{\sum_{k=1}^{n(f_s)} \frac{1}{120} \cdot \left[ \frac{V_p}{L_1} \cdot \frac{D}{f_s} \cdot \sin(2\pi \cdot 60 \cdot \frac{k-1}{f_s}) \right]^2} \]  
(2-19)

\[ I_{L_2,\text{rms}} = \sqrt{\sum_{k=1}^{n(f_s)} \frac{1}{120} \cdot \left[ \frac{V_p}{L_1} \cdot \frac{D}{f_s} \cdot \sin(2\pi \cdot 60 \cdot \frac{k-1}{f_s}) \right]^2}, \quad D_1 = \frac{V_p \cdot \sin(2\pi \cdot 60 \cdot \frac{k-1}{f_s})}{V_B} \]  
(2-20)

\[ I_{L_1,\text{ave}} = \frac{1}{2} \frac{V_p}{L_1} \cdot \frac{D}{f_s} \cdot \sum_{k=1}^{n(f_s)} \sin(2\pi \cdot 60 \cdot \frac{k-1}{f_s}) \]  
(2-21)

\[ I_{L_2,\text{ave}} = \frac{1}{2} \frac{V_p}{L_1} \cdot \frac{D}{f_s} \cdot \sum_{k=1}^{n(f_s)} \sin(2\pi \cdot 60 \cdot \frac{k-1}{f_s}) \]  
(2-22)

2) Switching loss \( P_{\text{sw}} \) (\( P_{\text{sw}} = P_{\text{sw,on}} + P_{\text{sw,off}} + P_{\text{sw.cap}} \))

Because both inductors operate in DCM, the MOSFET is turned on at zero current, the switching loss can be ignored during turn-on interval, and there is no reverse recovery during the switching turn-on time. However, since the energy stored in the output capacitor will be dissipated when the MOSFET turns on, turn-off loss and output capacitor loss needs to be considered.

a) Turn-off Loss

The turn-off time includes drain-source voltage rise time \( t_{rv} \) and the current fall time \( t_{fi} \). The voltage rise time \( t_{rv} \) is defined by the time it takes to remove the gate charge \( Q_{gd} \) by a fixed gate current, given as:
\[ t_{rv} = \frac{Q_{gd}}{V_{gs1} / R_g} \] (2-23)

The current fall time \( t_{fi} \) can be estimated by:

\[ t_{fi} = \frac{Q_{gs1} - Q_{th}}{V_{gs1} - V_{th}} \cdot R_g \cdot \ln\left(\frac{V_{gs1}}{V_{th}}\right) \] (2-24)

where \( R_g \) is the total gate resistance, including the driver resistance, external resistance and internal MOSFET resistance. \( Q_{gd}, Q_{gs1}, V_{gs1} \) and \( V_{th} \) are shown in Figure 2-20, and they all can be obtained from the device datasheet.

![Typical gate charge curve.](image)

Therefore, the turn-off loss can be estimated as:

\[ P_{sw\_off} = \frac{1}{2} I_{s\_pk} \cdot V_{DS} \cdot (t_{rv} + t_{fi}) \cdot f_s \] (2-25)

b) **Output Capacitor** \( C_{DS} \) **Loss**

The drain-to-source capacitance \( C_{DS} \) is charged up to \( V_{DS} \) during the switch-off time, and \( \frac{1}{2} C_{DS} V_{DS}^2 \) is dissipated through the charge loop. When the switch is turned on, the energy stored
in $C_{DS}$ is discharged as an extra drain current and is dissipated through $R_{ds(on)}$. The power dissipated is equal to the energy stored in this capacitance each switching cycle, that is $\frac{1}{2}C_{DS}V_{DS}^2$. Because during the charge time of $C_{DS}$, there is also the same energy dissipated through the charge loop, the total loss caused by $C_{DS}$ is:

$$P_{sw\_cap} = C_{DS,V_{DS}} \cdot V_{DS}^2 \cdot f_s$$  \hspace{1cm} (2-26)

Where $C_{DS,V_{DS}}$ can be derived from the datasheet values of $C_{oss}$ and $C_{rss}$ at the given value of $V_{DS}$.

Since the inductor copper losses and core losses depend on the detailed inductor design, including core material, core size, winding design, inductor losses are not included in this preliminary losses analysis. Detailed winding loss and core loss estimation will be discussed in Chapter 3. From the calculated losses, and assuming 1W fixed loss for inductors, the efficiency curve with respect to switching frequency is shown in Figure 2-21. Appropriate switching frequency can be selected according to the efficiency target.

![Figure 2-21. Efficiency versus frequency.](image-url)
Figure 2-22 shows the loss breakdown of the proposed circuit at 250kHz. Since $P_{\text{con\_diodes}}$ is the total diodes conduction losses, including the rectifier bridge, the loss of each diode is less than 0.3W. Since only half of the $C_{DS}$ loss (discharge loss) dissipates in the MOSFET, therefore the total loss on MOSFET is:

$$P_{\text{MOS}} = P_{\text{con\_mos}} + P_{\text{sw\_off}} + 1/2 P_{\text{sw\_cap}} = 1.305W \tag{2-27}$$

The temperature rise in the MOSFET is estimated as:

$$\Delta T = R_{\text{ja}} \cdot P_{\text{MOS}} = 62.5 \times 1.305 \approx 81.5^\circ C \tag{2-28}$$

### 2.3.3. Simulation results of $S^2$PFC AC/DC front-end

Parameters used in simulation are: $f_s = 250kHz$, $L_{1a} = L_{1b} = 170uH$, $L_2 = 167uH$, $C_b = 66uF$, $C_o = 0.22uF$, $D = 0.37$ at full load (90V/20W) and nominal input voltage (120Vac).

The ripple of bulk capacitor voltage $V_b$ can be estimated as:
\[
\Delta V_{b,\text{pk}} = \frac{V_{\text{in}} \cdot I_{\text{in}}}{2V_b \cdot \omega_b \cdot C_b} = \frac{20}{2 \cdot 120 \cdot 2\pi \cdot 60 \cdot 66 \mu} \approx 3.35V = 2.79\%V_b
\]

(2-29)

Low frequency ripple of the output voltage is

\[
\Delta V_{\text{out, pk}(f)} \approx \Delta V_{b,\text{pk}} \frac{D}{D_2} \approx 1.97V
\]

(2-30)

The high frequency ripple of output voltage can be estimated as:

\[
\Delta V_{\text{out, pk}(hf)} \approx \frac{1}{2} I_{L2,\text{pk}}(D + D_2)T \left( \frac{I_{L2,\text{pk}} - I_o}{I_{L2,\text{pk}}} \right)^2
\]

\[
\frac{2C_o}{2.85V \approx 3.16\%V_{\text{out}}}
\]

(2-31)

Figure 2-23 shows the simulation results. In the simulation, we change the line frequency to 600Hz to reduce the simulation time, therefore the ripple of \(V_b\) will be 1/10 of that at 60Hz line frequency. Figure 2-23(a) shows the output voltage, bulk capacitor voltage, and the input current (without filter). The average value of the output voltage is about 90V, and the average value of the bulk capacitor voltage is about 120V. Figure 2-23 (b) shows the drain-source voltage of the MOSFET.
Figure 2-23. Simulation results: (a) Output voltage, bulk capacitor voltage and input current, (b) Drain-Source voltage of MOSFET.
2.3.4. Improved SSPFC AC/DC front-end

2.3.4.1. Issues of the proposed SSPFC AC/DC front-end

Since the inductor $L_2$ operates in DCM, when the current through $D_3$ reduced to zero, $L_2$ will resonate with the junction capacitor of $D_3$. If there was no damping, the voltage across $L_2$, $V_L$ would reduce to $-V_o$, and the voltage across $D_3$ will be $2V_o$. When the load is open circuit, the output voltage is 300V, therefore 600V diode is not enough for the voltage rating. Therefore, an additional diode $D_4$ is used to clamp inductor voltage $V_L$ as shown in Figure 2-24. When $V_L$ decreases to $-V_b$, $D_4$ turns on, and the $V_L$ is clamped to $-V_b$, therefore the maximum voltage across $D_3$ will be limited under $V_b + V_o \approx 450V$.

This clamping diode $D_4$ can also reduce the voltage stress of $D_1$ and $S_1$. In this design, the output voltage $V_o$ at nominal load condition is lower than the bulky capacitor voltage $V_b$, clamping diode $D_4$ won’t turn on at nominal operation mode. Therefore, adding this diode will not sacrifice the efficiency.

![Figure 2-24. Single switch SSPFC front-end with clamping diode.](image-url)
Figure 2-25 show the currents through D1, D2 and D3 at different line input voltages (instantaneous value), respectively. Diode reverse recovery current is observed in the current waveforms.

During the interval between S1’s turning off and D2’s turning on, if \( v_{in} > V_{out} \) (at line input peak), a voltage of \( v_{in} - V_{out} \) is added to the leakage inductance and the stray inductance of the loop of input-B1-L1-D1-D2-D3-load, which produces a large \( \frac{di}{dt} = \frac{v_{in} - V_{out}}{L_{stray}} \). At the peak of line input, the current through D1 at the interval of S1 turning off is relatively high. This large di/dt will introduce a large reverse recovery current through D1, as shown in Figure 2-25. The reverse recovery current flows through the loop of input-B1-L1-D1-D2-D3-load. For D2, this reverse recovery current is cancelled by the positive current through it; while for D3, this reverse recovery current adds a large peak to the current through it, as shown in Figure 2-25 (c).

Similarly, if \( v_{in} < V_{out} \) (at line input valley), D1 keeps on. The reverse recovery will occur on the diode bridge. Since the current through the rectifier bridge before the switch turn off is relatively small at line input valley, the reverse recovery current will be much smaller than that at high line.

Fortunately, the reverse recovery currents occur when the switch turns off, therefore the currents will not flow through the switch, and won’t produce more turn-on loss as the conventional reverse recovery related cases. But the reverse recovery currents flow through the load, which results in a larger low frequency ripple in the output voltage.
\[
di/dt = (V_{in} - V_{out})/L_{stray}
\]

Figure 2-25. Reverse recovery current in SSPFC stage: (a) Current through D1, (b) Current through D2, (c) Current through D3.
2.3.4.2. Proposed two-switch SSPFC AC/DC Front-End

In order to solve the above issue, an alternative implementation of this SSPFC AC/DC converter is proposed as shown in Figure 2-26. An additional MOSFET $S_2$ is used to separate the PFC semi-stage and DC/DC semi-stage, therefore the blocking diode $D_1$ can be eliminated. The body diode of $S_2$ can also be used as the clamping diode when $L_2$ operates on DCM, therefore, the clamping diode $D_4$ can also be eliminated.

![Figure 2-26. Proposed two-switch SSPFC front-end.](image_url)

Although one Mosfet is added, two diodes can be eliminated. Since MOSFETs $S_1$ and $S_2$ are in common-gate common-source connection, no additional PWM controllers and gate drivers are needed to drive the 2nd switch. Compared with the single-switch version, because the total current is conducted by two switches, the conduction loss will be greatly reduced. Therefore we can use the smaller current capability Mosfet with the smaller package (IPAK or DPAK), larger $R_{ds(on)}$, and smaller $C_{ds}$, to keep the conduction loss the same, but reduce the $C_{ds}$ loss, and the total footprint of the two switches (IPAK/DPAK) is almost the same as that of the single switch (TO-220).

The benefits of the two-switch version can be summarized as follows:
1. Due to the elimination of Diode D1, the reverse recovery related problems, such as reverse recovery losses and large output ripple, are solved. The body diode of MOFET S2 also serves as the clamping diode, so the original clamping diode D4 can be saved.

2. Each MOSFET only deals with the current of one semi-stage, which is around half of the total current in the single-switch version. Total losses can be smaller than that of the single-switch with the same footprint by selecting suitable devices. The loss of each switch is much smaller than the previous case, and the heat sink can be saved.

2.3.5. Constant power control scheme

Since the inverter stage is unregulated, the lamp power regulation needs to be implemented in the SSPFC AC/DC front end. Unity PF and low THD can be inherently achieved by maintaining constant levels of switching frequency and duty cycle in each half line cycle. Therefore, the control bandwidth should be lower than 120Hz to achieve the unity power factor.

![Figure 2-27. Control scheme of SSPFC front-end.](image)

![Figure 2-28. Ideal ballast curve](image)
Figure 2-27 shows the control scheme for the SSPFC front-end. Instead of the output voltage, the lamp power signal is controlled so it is constant during the steady state. The equivalent lamp power signal can be obtained from the DC output of the SSPFC stage. The drain current through the MOSFET $S_2$ is sensed for comparison with the error signal from the error amplifier. The power control law can be expressed as:

$$K \cdot \text{Max}(K_p V_o, V_{CL}) \cdot \text{Max}(K_I I_o, V_{YL}) = P_{ref}$$

(2-32)

Where $K$ is the gain of the multiplier, $K_p$ is the voltage-sensing gain, $K_I$ is the current-sensing gain, $V_{CL}$ is the reference voltage for current limiting, and $V_{YL}$ is the reference voltage for voltage limiting. Thus different power regulations can be realized under different load conditions.

1) Before ignition:

$$K_p V_o > V_{CL}, \quad K_I I_o < V_{YL} \quad \Rightarrow V_o = \frac{P_{ref}}{K \cdot K_p \cdot V_{YL}} = \text{cons} \tan t$$

(2-33)

2) During start-up time:

$$K_p V_o < V_{CL}, \quad K_I I_o > V_{YL} \quad \Rightarrow I_o = \frac{P_{ref}}{K \cdot K_I \cdot V_{CL}} = \text{cons} \tan t$$

(2-34)

3) During steady state:

$$K_p V_o > V_{CL}, \quad K_I I_o > V_{YL} \quad \Rightarrow P_o = V_o I_o = \frac{P_{ref}}{K \cdot K_p K_I} = \text{cons} \tan t$$

(2-35)

Therefore, the SSPFC AC/DC front-end can achieve a constant voltage regulation before ignition, constant current regulation during the start-up interval, and constant output power regulation at steady state. The ideal ballast curve is shown in Figure 2-28.
2.4. Implementation and Experimental Verification of HID Ballast

2.4.1. Implementation of a 20W HID ballast

2.4.1.1. Whole system structure

Figure 2-29 shows the system structure of the 20W HID ballast, which consist of two stages: the proposed SSPFC AC/DC front-end with constant power regulation cascaded with an unregulated low frequency full bridge square wave inverter. The ignitor is integrated with the inverter. Detailed circuit implementation is discussed in the following part.

![System structure of a 20W HID ballast.](image)

2.4.1.2. Low frequency inverter and ignitor

Figure 2-30 shows the low-frequency inverter with the ignitor. In the steady state, switches $S_2$~$S_5$ operate at low frequencies (each at 400Hz). Before the lamp is ignited, the full bridge
operates at a high frequency near the resonant frequency of $L_r$ and $C_r$, and the LC resonant tank will produce several thousand volts of voltage to ignite the HID lamp.

Based on the Farad law, the size of the resonant inductor is determined by the resonant frequency and the voltage across the inductor, which can be expresses as:

$$V = \frac{d\phi}{dt} = N \cdot A_e \cdot dB \cdot dt \Rightarrow \lambda = V \cdot \Delta t = 2N \cdot A_e \cdot \dot{B}$$  \hspace{1cm} (2-36)

Where: $V$ is the amplitude of the ac voltage across the inductor, $N$ is the number of the turns of the winding, $A_e$ is the effective area of the magnetic core, $B$ is the flux density, and $\lambda$ is the volt-second.

Higher resonant frequency leads to a smaller inductor size. In order to reduce the switching loss that occurs during ignition mode, third- (or even higher-order) harmonic resonance can be used to reduce the switching frequency. In this design, the resonant frequency of LC is set at 450kHz, while the switching frequency sweeping from 100kHz to 200kHz for $3^{rd}$ harmonic resonance.

![Figure 2-30. Low frequency inverter with LC resonant ignitor](image)

For Figure 2-30 (a), before the lamp is ignited, there is no current through the lamp. Therefore, the exciting voltage of the resonant tank is a square wave voltage (the amplitude is $\frac{V_{Bus}}{2}$) with a DC value of $\frac{V_{Bus}}{2}$. In Figure 2-30 (b), by changing the position of the resonant
capacitor, the exciting voltage of the resonant tank is a square wave voltage with the amplitude of $V_{Bus}$, therefore, with the same voltage gain of the resonant circuit, the ignition voltage will be twice of that of the previous one.

A low power microcontroller (87LPC764) is used to produce the gate signal for the full bridge inverter. The lamp voltage at the DC side (output voltage of SSPFC stage) is monitored to determine the appropriate operation mode. Before the lamp is ignited, the lamp voltage is 300V. After the lamp is ignited, the lamp voltage drops to a value lower than 90V.

Figure 2-31 shows the flowcharts of the main program, comparator interruption subprogram and ignition mode program. One set of ignition mode operation is applied after the initialization, then the MCU detects the lamp voltage and decides to continue ignition mode or go to the normal mode. The comparator interruption is set for lamp restart after distinguish. A 5-second delay is applied before the restart.

The detailed timing control during the ignition period is shown in Figure 2-31(c). One set of switching operations for resonant ignition is applied every 800ms until the lamp is ignited. Two diagonal Mosfets turn on and off at the same time, and two pairs of Mosfets turn on and off alternatively. In each cycle of the ignition mode, there are three different parts. In part A, the switching frequency is sweeping from 100kHz to 200kHz, and duration of this part is 50ms. In part B, the switching frequency is fixed at 100kHz, and part B will last for 20ms. In part C, the switching frequency is fixed at 400Hz. The period of the part C is 730ms. Part C is set to avoid the overheating of the ignitor transformer.
Figure 2-31. Inverter/ignitor stage timing control: (a) Main program (b) Comparator interruption sub-program, (c) Ignition mode program.
2.4.2. Experimental verification of a 20W HID ballast

An HID lamp ballast prototype, as shown in Figure 2-32, is built to verify the operation principles of the proposed circuit and to demonstrate the improvement in power density. The key component parameters of the prototype are: $L_{1a} = L_{1b} = 170 \mu H$, $L_2 = 170 \mu H$, $C_b = 68 \mu F$, $C_o = 0.22 \mu F$. The SSPFC front-end operates at 250kHz, and the inverter stage operates at 400Hz at steady state. The measured total efficiency at nominal input (120Vac) is 84.2%. The power density of the whole ballast is about 4.68W/inch$^3$, which is twice the density of state-of-the-art commercial products operating at the same power level.

The key switching waveforms of the S$^2$PFC AC/DC front end are shown in Figure 2-33 and Figure 2-34. Figure 2-33 shows the drain-source voltage and the switch current. Figure 2-34 shows the currents through inductors $L_1$ and $L_2$.

Figure 2-35 shows the input voltage and current waveforms. At nominal input (120Vac), the measured input PF is 0.996, and the THDs of the input voltage and current are: $V_{THD} = 1.153\%$ and $I_{THD} = 8.077\%$, respectively. Figure 2-36 shows that the input-current harmonics
are well below the IEC 61000-3-2 Class C standard. Figure 2-37 shows the PF and input current at different input voltage levels; a high PF (>99%) and low THD (<10%) can be achieved within the input-voltage range of 120Vrms±10%.

Figure 2-38 shows the lamp voltage and current at the steady state. Figure 2-39 shows the curve of a normalized output power vs. output voltage. It shows that the output current stays constant when the output voltage is less than about 50V, a constant output power can be achieved near the nominal operating point, and the output voltage is limited at about 290V.

Figure 2-40 shows the bulk capacitor voltage at different output voltage levels: The bulk capacitor voltage is less than 150V at all load conditions.
Figure 2-34. Currents through inductors.

Figure 2-35. Input voltage and input current.
Figure 2-36. Input-current harmonics.

Figure 2-37. Input PF and I_{THD} vs. v_{in}.
Figure 2-38. Lamp voltage and current at steady state.

Figure 2-39. Normalized output power vs. output voltage
2.5. Summary

In this chapter, a two-stage HID ballast is proposed, which includes a SSPFC AC/DC front-end and an non-regulated low frequency square wave inverter. How to select the SSPFC topology for low-wattage HID ballast and how to design the proposed SSPFC frond-end are discussed in this chapter. The proposed topology can take advantage of the DCM operation of both the PFC stage and DC/DC semi-stage to achieve near-unity PF, low THD, low bulk capacitor voltage, and constant output power by using a simple PWM control scheme. The power density of the entire ballast is increased as a result of the passive components’ size reduction, achieved through higher-frequency operation. Therefore, this topology is very suitable for the low-power, low-cost ballast application. A prototype is built; its input PF is 0.996 and its input-current THD is 8.077%. The efficiency for the whole ballast at nominal input is 84.2%. The power density of the entire ballast is 4.68W/inch³, which is twice the density of commercial products.
The proposed two-stage HID ballast has been commercialized and was launched in the US market starting in June 2007. The new product features an even higher power density of 6 W/in$^3$, which counts for 2.5 times the power density of the previous commercial product (2.4 W/in$^3$), as shown in Figure 2-41.

![Diagram showing power density comparison](image)

**Figure 2-41. Power density comparison.**
Chapter 3. High Density 3D Passive Integrated Ballast

3.1. Background on Integration Technologies

With the aim of increasing the power density and improving converter performance, a current trend in converter manufacturing is the integration of power converters into various integrated power electronic modules. According to different electrical functions and processing technologies, the integrated power electronics modules (IPEMs) can be chiefly classified into two categories, active IPEMs and passive IPEMs. Active power electronics modules have been well explored and successfully developed as standardized commercial products [51].

However, in most power electronics converters, the largest part of the converter volume usually consists of electromagnetic passives. As a result, electromagnetic integration technology has been a topic of research in the past few decades. By integrating the electromagnetic functions of the inductor, capacitor and transformer into a functional module, the number of the passive components is reduced and the overall passives volume decreases.

Passives integration is aimed at achieving the following advantages over discrete passive components:

- Functional integration for better performance
- Reduction in volume, profile and mass for higher power density
- Modularization for better manufacturability for mass production and low cost
- Improvement in ruggedness and reliability.
In cooperation with active and passive integration technologies, a fully integrated power converter could be constructed to consist of only a number of integrated active modules and integrated passive components, as shown in Figure 3-1. Studies have already been published on this kind of integration of reactive components in resonant and soft-switching power electronic converters [52-58].

**Figure 3-1. Converter integration.**

### 3.1.1. Principle of passive integration technologies

Electromagnetic integration can be best described by first considering a simple bifilar spiral winding like that shown in Figure 3-2. This structure consists of two windings (A-C and B-D), separated by a dielectric material. The resultant structure has distributed inductance and capacitance, and is an electromagnetically integrated LC-resonant structure. With different terminal conditions, the structure performs different functions as a combination of inductors and capacitors. More complex integrated structures can be realized by adding more winding layers so that the integrated structure can perform complicated functions with the combination of inductors, capacitors and transformers; for instance, the integrated LLCT module [80] for a resonant converter, as shown in Figure 3-3.
The design of these integrated structures requires a deliberate increase or modification of naturally existing structural impedances to realize a particular equivalent circuit function. For example, the intra-winding capacitance is purposely increased to form the LC resonant structure. The classical term “parasitics” therefore no longer applies, and all the higher-order impedances are rather referred to as “structural impedances” [59].

**Figure 3-2.** General integrated L-C structure and equivalent circuits [59 J. D. van Wyk, et al, “A Future Approach to Integration in Power Electronics Systems”, IEEE IECON 2003].

**Figure 3-3.** Integrated LLCT component and equivalent circuit [59 J. D. van Wyk, et al, “A Future Approach to Integration in Power Electronics Systems”, IEEE IECON 2003].
3.1.2. Previous work on passive integration in power electronics

In previous work, integrated passives have been theoretically and experimentally investigated in relation to aspects of electromagnetic modeling, structure, processing technologies, loss modeling, and design algorithms based on the planar spiral winding structure.

Several structures have been proposed to implement passive integration, such as the original bifilar structure [60-62], the cascaded transmission lines structure [63], and the planar spiral winding integrated LC structure [64-69], as well as the more advanced multi-cell [70-72] and stacking structures [73-74]. In a bifilar structure, the achievable capacitance is limited by the flexible dielectric material which has lower permittivity. In a planar spiral winding structure, high-permittivity dielectric materials can be used to achieve higher capacitance. The spiral winding structure has been successfully applied in power electronics. To increase the volume utilization ratio, design flexibility and mechanical reliability, the multi-cell structure and stacking structure were developed.

These structures have been applied in several areas in power electronics, such as the LC resonator [75-76], or the LCT or LLCT module [77-79] in resonant converters. With the spiral winding structure, a developed LLCT module [78] reaches the power density of 480W/in$^3$. With the stacked structure and heat extraction technology, a power density of 1147 W/in$^3$ is achieved in a LLCT module, with an efficiency of 97.8% at 1000W output [74].

Other than the application in power conversion for storing and processing electromagnetic energy at the switching frequency, passive integration technology can also be used in an integrated EMI filter [95-98], which attenuates electromagnetic energy at the switching frequency and above.
3.2. System Partitioning and Integration Strategy for HID Ballast

In Chapter 2, a two-stage structure with a regulated SSPFC AC/DC front-end and an unregulated low frequency DC/AC inverter was developed for low-wattage HID lamp ballasts. Figure 3-4 shows the circuit configuration of the HID ballast. The prototype implemented with discrete components is shown in Figure 3-5. By simplifying the system structure and circuit topology, and by pushing the switching frequency to 250 kHz, the size of the passive components is reduced dramatically, and the power density of the whole ballast is about 4.68W/inch³, which was twice the benchmark commercial product.

Figure 3-4. Circuit configuration of the HID ballast.
Figure 3-5. Discrete implementation of HID ballast.

However, it can be observed from Figure 3-5 that the volume utilization of this prototype is very poor due to the large component count and different form factor. A large component count also results in a higher labor cost. A volume breakdown of the ballast prototype is shown in Figure 3-6. Around 55% of the space is not utilized, which allows the possibility to further improve the power density by improving the volume utilization. Figure 3-6 also shows that more than 90% of the component volume is occupied by large passive components, such as inductors, bulky capacitors, and EMI filters. Therefore the passive integration is the major task to further reduce the ballast size.

Figure 3-6. Volume breakdown of discrete HID ballast
The main purposes of applying the integration and packaging technologies are to increase the volume utilization to reduce the ballast size; to achieve functional, structural and processing integration to reduce the component count, reduce component size and reduce labour costs for mass production; and to achieve better thermal conditions.

At first, the whole system is partitioned into two parts: the active part, including semiconductors like diodes and MOSFETs with their controller and drivers; and the power passive part, which includes inductors and capacitors, as shown in Figure 3-7.

Based on circuit functions, power passive components are further partitioned into several functional modules: the EMI filter, the ignitor (which is an LC series resonator), and the LC output filter, as shown in Figure 3-8. Those passive components, that are not suitable for integration with other components due to material and processing limitations, such as the energy storage electrolytic capacitor \( C_b \) and the coupled flyback inductor \( L_1 \), are optimized into a planar structure for better space usage and thermal performance. The technology of stacked foil large-sized aluminum electrolytic capacitors proposed in [100] can be applied for the large energy storage capacitor \( C_b \).

Figure 3-7. System partitioning of the HID ballast.
All active components, including the MOSFETs, diodes and control circuitry, are divided into two parts according to the circuit function, i.e., the SSPFC stage and the inverter stage; and implemented in two small PCBs, which are vertically mounted on the mother-board. Chip-on-board (COB) technology can be used for further size reduction. In the comprehensive design of the integrated ballast, active integrated function blocks have a shape and dimensions consistent with the integrated passive modules, and occupy about 15% of the total volume.

In this integrated ballast, all the components are designed to have the same form factor, which enables the maximum usage of the 3D space. Figure 3-9 shows the structure of the proposed integrated ballast. The volume utilization is expected to be increased to 80%. Detailed design and specifications of three main integrated passive components are summarized below.
3.3. Integrated Power Passives in HID Ballast

3.3.1. Functional integration, structural integration and hybrid integration

The benefits of functional integration of the passive integration technology may be limited by material characteristics and processing technologies. For the integrated LC module shown in Figure 3-2, the copper length and width is subject to the inductor design, while the total copper area is related to the capacitor design. Since practical values of material characteristics, such as permeability and permittivity, are fixed by physical properties and may not meet the desired value, the design freedom is limited. For given material characteristics, it is difficult to reach the minimum volume for the inductor and the capacitor at the same time. When there is a mismatch between the required copper area for the inductor and that for the capacitor, hybrid integration or structural integration can be alternative solutions.

For example, if the designed inductance is large and requires a long copper length, there is a large copper area for a certain copper width, while the designed capacitance is small and requires a small total copper area. To solve this problem, the inductor winding consists of two parts: one is functionally integrated with the capacitor and the other is the pure copper winding. This forms the hybrid integration. Obviously, hybrid integration covers functional integration. In some cases, the inductor winding has too many turns and too small a copper width for integrating the capacitor. For these cases, the inductor and capacitor are designed separately but assembled together as one module. This forms the structural integration.

All three types of passive integration, functional integration, structural integration and hybrid integration are covered in the proposed integrated ballast. The EMI filter and the ignitor ($L_I$ and $C_I$) are implemented with a hybrid structure; the LC output filter ($L_2$ and $C_o$) is
implemented by structural integration. The coupled inductor ($L_1$) is designed with the planar structure to have a better form factor. Stacked-foil aluminum electrolytic capacitor technology [100] is used for the bulk capacitor ($C_b$). The design of each of the integrated passive components is discussed in this chapter.

### 3.3.2. Integrated ignitor: LC series resonator

In this chapter, the ignitor refers to the series resonant inductor $L_r$ (the auto-transformer version is used to boost the ignition voltage) and the resonant capacitor $C_r$, as shown in Figure 3-10. To achieve high ignition voltage, high voltage gain is needed, and high voltage of several thousand volts across the resonant inductor and capacitor is the main design concern.

![Figure 3-10. LC series resonator with auto-transformer configuration as the ignitor.](image)

The basic concept for integrating the ignitor is to integrate the primary winding of $L_1$ and $C_r$ by using the planar spiral winding LC structure terminated as a series resonator, and adding the secondary winding of $L_r$ in the same core to realize magnetic coupling. The structure of the integrated ignitor is shown in Figure 3-11.

In this design, the resonant capacitance is several hundred pico-farads, while the resonant inductance is several hundred micro-henrys. The conductor area required by the inductor is much more than that required by the capacitor. The integrated resonator is implemented with the
hybrid structure. The integrated LC resonator is made of Pyralux with double-sided copper layers on a Kapton substrate. The Kapton layer between the two copper layers works as the dielectric material and provides the resonant capacitance. Terminals a’ and d are connected to the switching nodes, and terminals d and e are connected to the lamp.

As shown in Figure 3-12, the integrated resonator is implemented by four layers of Pyralux windings and four layers of pure copper windings. The additional winding $L_{r2}$ is made of PCB winding.

![Figure 3-11. Integrated ignitor - Structure I.](image)

![Figure 3-12. Composition of the integrated ignitor - Structure I.](image)

For the integrated ignitor shown in Figure 3-11, if the turn’s ratio of the single-side winding ($W_1'$) to the double-side winding ($W_1$) and secondary winding ($W_3$) is $1 : n_1 : n_2$, then the ignition voltage applied to the lamp, $V_{des}$, can be expressed as
\[ V_{dc} \approx V_{dc} + V_{ce} \approx (1 + \frac{n_2}{1 + n_1})V_{Cr} \]  \hspace{1cm} (3-1) 

where \( V_{Cr} \) is the voltage across the capacitor, which is determined by the voltage gain of the series resonator.

In Structure I, the additional winding \( W_2 \) is added only to generate the resonant capacitor \( C_r \) in Structure I. It is noticed that the voltage across winding \( W_2 \), \( V_{bd} \), is in phase with the ignition voltage \( V_{de} \). Based on this observation, Structure I can be improved by simply changing the output termination. Instead of terminals d and e, terminals b and e are connected to the lamp, as shown in Figure 3-13. As a result, the voltage across winding \( W_2 \) is added to the ignition voltage, which can be expressed by the following equation:

\[ V_{be} \approx V_{bd} + V_{dc} + V_{ce} \approx (1 + \frac{n_1}{1 + n_1} + \frac{n_2}{1 + n_1})V_{Cr} \]  \hspace{1cm} (3-2) 

Due to the additional voltage across winding \( W_2 \), to achieve the same ignition voltage across the lamp, the number of turns' of secondary winding \( W_3 \) can be greatly reduced. Therefore the component size can be reduced, as shown in Figure 3-14.

![Figure 3-13. Integrated ignitor - Structure II.](image-url)
Prototypes of the two structures of the integrated ignitor are built and compared in Table 3-1. The dimensions of the magnetic core is shown in Figure 3-14. For the same cross-section of the core, the winding thickness of Structure II is reduced from 5mm to 2.3mm, and the total thickness and volume of the integrated ignitor is reduced by 32.6%.

Table 3-1. Comparison of the integrated ignitors.

<table>
<thead>
<tr>
<th></th>
<th>Structure I</th>
<th>Structure II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of turns/layer</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Number of layers for each winding</td>
<td>4/4/4/12</td>
<td>2/4/4/6</td>
</tr>
<tr>
<td>Number of turns for each winding</td>
<td>20/20/20/60</td>
<td>10/20/20/30</td>
</tr>
<tr>
<td>Copper winding thickness (µm)</td>
<td>70</td>
<td>70</td>
</tr>
<tr>
<td>Kapton thickness in pyralux (µm)</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Total winding thickness (mm)</td>
<td>5</td>
<td>2.3</td>
</tr>
<tr>
<td>Total component thickness (mm)</td>
<td>9.2</td>
<td>6.2</td>
</tr>
<tr>
<td>Total Volume (mm³)</td>
<td>20<em>30</em>9.2 =5520</td>
<td>20<em>30</em>6.2 =3720</td>
</tr>
<tr>
<td>Lr</td>
<td>403µH</td>
<td>384µH</td>
</tr>
<tr>
<td>Cr</td>
<td>336 pF</td>
<td>401pF</td>
</tr>
</tbody>
</table>
Figure 3-15. Dimensions of the magnetic core for the integrated ignitor.

Figure 3-16 shows the measured impedance $Z_{\text{a'd}}$ of the new integrated ignitors. Since the two structures have the same primary winding design, the first resonant frequency is almost the same. Structure II has fewer winding turns in the secondary winding, which results in less inductance and less parasitic capacitance between the primary and secondary windings; therefore the higher order resonant frequencies are higher than those of Structure I. The picture of the integrated ignitor is shown in Figure 3-17.

Figure 3-16. Measured $Z_{\text{a'd}}$ of the integrated ignitors (blue: Structure I, red: Structure II).
3.3.3. **Integrated LC output filter**

The LC output filter consists of inductor $L_2$ and capacitor $C_o$, as shown in Figure 3-18. Since there is no electromagnetic coupling between the two components, functional integration is not necessary. To reduce the overall volume and enhance mechanical stability, $L_2$ and $C_o$ are implemented using structural integration technology. The inductor $L_2$ is made of the PCB winding. Capacitor $C_o$ has the form of a parallel-plate capacitor. Two copper layers are deposited on a dielectric substrate to form the capacitor. The inductor and capacitor are designed to have the same footprint and are stacked together to implement the structural integration.

![LC output filter configuration](image)

Figure 3-18. LC output filter configuration.

To assemble the integrated module, the capacitor can be put inside the core or outside the core, as shown in Figure 3-19. The position of the capacitor is related to parasitic parameters, which influence the performance of the output filter. Figure 3-20 shows the equivalent circuits for two different capacitor positions. Typical parasitic parameters are extracted using Maxwell Q3D simulator, and the simulated impedance is shown in Figure 3-21. The results show that the
larger parasitic capacitance, $C_c$, in Structure A will influence the high-frequency performance of the LC filter, while the influence of the lead inductance can be avoided by proper interconnection to insure the lead inductance is in series with the main inductor. Therefore Structure B has better high-frequency performance.

Other aspects, such as losses, mechanical stability and thermal performance are also considered for these two structures, as shown in Table 3-2. When the planar capacitor is put inside the core, there will be eddy current going through the capacitor winding conductor, which will increase the loss. Since the capacitor is closely attached to the inductor winding, the dielectric property of the capacitor material will be influenced by the heat generated from the inductor winding. As for the mechanical stability, each structure has its own benefits and drawbacks. When the capacitor is inside the core, the metallization area is reduced, and the heat is more balanced on the two sides of the capacitor conductor, which is better than the case when the capacitor is outside the core; however, there needs to be a hole in the inside capacitor, and the additional laser cutting process needed for this will add more mechanical stress to the capacitor.

![Figure 3-19. Integrated LC structures: (a) Structure A: Capacitor inside the core, (b) Structure B: Capacitor outside the core.](image)
Figure 3-20. Equivalent circuit of different structural integrated LCs: (a) Structure A: Capacitor inside the core, (b) Structure B: Capacitor outside the core.

Figure 3-21. Simulated impedance of integrated LC: (a) Impedance between b & c, (b) Impedance between a & c.
Table 3-2 Comparison between different capacitor positions

<table>
<thead>
<tr>
<th></th>
<th>Structure A: Cap inside the core</th>
<th>Structure B: Cap outside the core</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Losses</strong></td>
<td>More loss due to the eddy current on cap metal</td>
<td>No eddy current on cap metal</td>
</tr>
<tr>
<td><strong>Parasitic effect</strong></td>
<td>EPC of the inductor is increased by the capacitance between winding and cap</td>
<td>The influence of lead inductance can be avoided</td>
</tr>
<tr>
<td><strong>Mechanical Stability</strong></td>
<td>More stable</td>
<td>Larger mechanical stress</td>
</tr>
<tr>
<td><strong>Thermal performance</strong></td>
<td>Dielectric property is influenced by temperature</td>
<td>Dielectric property is less influenced by temperature</td>
</tr>
</tbody>
</table>

According to the comparison in Table 3-2, Structure B with the capacitor outside the core is selected in this design. The dimensions of the magnetic core for the planar inductor are shown in Figure 3-22, and the detailed specifications of the planar inductor are summarized in Table 3-3.

![Figure 3-22. The dimensions of the magnetic core for planar output inductor.](image)
Table 3-3. Specifications of the planar inductor prototype.

<table>
<thead>
<tr>
<th>Specifications</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn’s number</td>
<td>20</td>
</tr>
<tr>
<td>Layer’s number</td>
<td>4</td>
</tr>
<tr>
<td>Copper thickness</td>
<td>140µm</td>
</tr>
<tr>
<td>Insulation layer thickness</td>
<td>1mil Kapton + 1mil adhesive layer</td>
</tr>
<tr>
<td>Winding width</td>
<td>500µm - 700µm</td>
</tr>
<tr>
<td>Winding space</td>
<td>250µm - 400µm</td>
</tr>
</tbody>
</table>

To achieve sufficient capacitance with the same footprint, high-permittivity dielectric material Y5V is used to implement the capacitance. The material property of Y5V is the main design concern. The permittivity of the Y5V material is sensitive to temperature and electrical field [101]. Figure 3-23 shows that the effective permittivity of Y5V is reduced with the increase in temperature and electrical field. The design value of the effective permittivity is selected based on the temperature at the thermal steady state and the rated output voltage. Detailed design parameters of the planar capacitor are listed in Table 3-4.

![Figure 3-23. Relative permittivity vs. DC bias voltage & temperature for Y5V.](image)

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Table 3-4. Design parameters of the planar capacitor.

<table>
<thead>
<tr>
<th>Dielectric Material</th>
<th>Ceramic Y5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Effective Permittivity at 80°C, 90V</td>
<td>3200</td>
</tr>
<tr>
<td>Thickness</td>
<td>0.15 mm</td>
</tr>
<tr>
<td>Number of capacitors in parallel</td>
<td>2</td>
</tr>
<tr>
<td>Dimensions of single capacitor (width X length)</td>
<td>20 mm X 22 mm</td>
</tr>
<tr>
<td>Designed capacitance</td>
<td>166nF</td>
</tr>
<tr>
<td>Measured capacitance at 80°C, 90V</td>
<td>167nF</td>
</tr>
</tbody>
</table>

Attaching the planar capacitor to the planar inductor results in the structural integrated LC module. Pictures of both discrete and integrated LC filters are shown in Figure 3-24. Sizes of the two different implementations are compared in Table 3-5. Although the total volume of the integrated module is slightly increased, the footprint occupied on the motherboard is greatly reduced due to the better form factor, and the component count is reduced as well.

Figure 3-24. Pictures of output filters: (a) discrete LC filter, (b) integrated LC filter.
Table 3-5. Size comparison between the discrete LC and the integrated LC module.

<table>
<thead>
<tr>
<th></th>
<th>Discrete LC filter</th>
<th>Integrated LC module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>20mm x 30mm x 5.5mm</td>
<td></td>
</tr>
<tr>
<td>Total volume</td>
<td>2640mm³</td>
<td>3300mm³</td>
</tr>
<tr>
<td>Profile</td>
<td>10mm/8mm</td>
<td>20mm</td>
</tr>
<tr>
<td>Total footprint</td>
<td>281mm²</td>
<td>165mm²</td>
</tr>
</tbody>
</table>

3.3.4. Integrated EMI filter

3.3.4.1. Integrated EMI filter design

Figure 3-25 shows the schematic of a typical one-stage EMI filter for power converters, which is used in the HID ballast. An integrated EMI filter was proposed in [95-98] for the front-end converter in a distributed power system. All the filter components are integrated into one module, constructed by standard semiconductor processing and packaging techniques. Figure 3-26 shows the composition of the integrated EMI filter. The CM inductor and CM capacitor are functionally integrated with a low-pass filter termination configuration. The leakage inductance between the two CM windings serves as the DM inductance. DM capacitors are also implemented by integrated LC winding connected as capacitors, and a four-terminal transmission line connection method is used to minimize the equivalent series inductance (ESL) of the DM capacitors.
The above integrated EMI filter structure is applied in this dissertation with some modifications in the implementation, which are described below.

(a) CM filter design

Since a large CM inductance (several mH) requires a larger number of turns for the winding, and the CM capacitance (several thousand pF) requires a relatively small copper area, a hybrid structure is used for this winding design. An N1250 ceramic substrate with copper layers on both sides is needed to realize the required CM capacitance and part of the CM inductance. The rest of the layers are pure copper foil to realize the rest of the CM inductance.
Given the required inductance value and given core design, the required number of turns for the CM inductance can be calculated by the following equation:

$$N = \left[ \frac{L_{CM} \cdot \left( \frac{I_{eff}}{\mu_c \cdot \mu_0 \cdot A_c} + \frac{I_{gap}}{\mu_0 \cdot A_c} \right)}{c_{gap}} \right]$$

(3-3)

In this design, the required CM inductance is $L_{CM} = 4.3mH$.

A 3E5 ferrite core with a relative initial permeability of 100,000 is used in this design. Figure 3-27 shows the dimensions of the magnetic core for the integrated EMI filter. The cross-sectional area of the core $A_c$ is 80mm$^2$, and the effective magnetic path $L_{eff}$ is 30mm. It is assumed that the air gap between the E core and I core $l_{gap}$ is 5$\mu$m. The required number of turns for CM inductance is around 16.

A shield layer is inserted in the middle of each CM winding to cancel the equivalent parallel capacitance (EPC) of the CM winding. If the capacitance between the shield and one side of the
winding is \( C_g \), then the total added capacitance between the winding and ground is \( 2C_g \). To fully cancel the winding capacitance, we need \( 2C_g = 4C_e \), thus \( C_g = 2C_e \). After inserting the shield layer, the EPC of the CM choke winding is also changed, since part of the winding has been shielded.

Assuming the width of the shield is the same as the width of the winding window and its length is \( X \) mm, the capacitances \( C_e \) and \( C_g \) can be calculated from the following equations.

\[
C_e = \frac{n}{n^2} \left( \frac{1}{m} - \sum_{i=1}^{m} \frac{\varepsilon_0 \varepsilon_r W_w \cdot (l_i - X) \cdot (2i - 1)^2}{h_i} \right)
\]

\[
C_g = \frac{m \varepsilon_0 \varepsilon_r W_w X}{h_2}
\]  

(3-4)  

(3-5)

where \( W_w \) is the width of the winding conductor, \( h_i \) is the thickness of the insulation material between the two winding layers, and \( \varepsilon_r \) is the relative permittivity of the insulation material. \( h_2 \) is the thickness of the insulation material between winding layer and the embedded ground plane.

From Eqs. (3-4) and (3-5), the length of the shield layer can be calculated to realize \( C_g = 2C_e \).

The designed CM capacitance is \( C_{CM} = 1nF \). The mean length of one turn is \( l_{mean} = 68mm \). The trace width is \( w_{trace} = 500\mu m \). To implement the CM capacitance in one layer, the required permittivity to thickness ratio is:

\[
\frac{\varepsilon_r}{d} = \frac{C_{CM}}{\varepsilon_0 \cdot m \cdot l_{mean} \cdot w_{trace}} = 9.135 \times 10^5
\]

(3-6)

Table 3-6 lists several kinds of dielectric materials that are available with their relative permittivity and thickness. Considering the desired CM capacitance value and the dimension of
the component, N1250 ceramic material with \( \frac{\varepsilon_{N1250}}{d_{N1250}} = \frac{174}{150 \mu m} = 1.16 \times 10^6 \) is selected. The main characteristics of N1250 dielectric material are listed in Table 3-7.

Table 3-6. Available dielectric materials.

<table>
<thead>
<tr>
<th>Material</th>
<th>Relative permittivity</th>
<th>Thickness(µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP0</td>
<td>82</td>
<td>270</td>
</tr>
<tr>
<td>N1250</td>
<td>174</td>
<td>150</td>
</tr>
<tr>
<td>X5S</td>
<td>2205</td>
<td>190</td>
</tr>
<tr>
<td>X5U</td>
<td>4200</td>
<td>450</td>
</tr>
<tr>
<td>X7R1</td>
<td>2200</td>
<td>200</td>
</tr>
<tr>
<td>X7R2</td>
<td>3500</td>
<td>180</td>
</tr>
<tr>
<td>Y5V</td>
<td>14000</td>
<td>150, 200, 300</td>
</tr>
</tbody>
</table>

Table 3-7. Characteristics of N1250.

<table>
<thead>
<tr>
<th>Material</th>
<th>N1250</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relative Permittivity</td>
<td>174</td>
</tr>
<tr>
<td>Thickness (µm)</td>
<td>150</td>
</tr>
<tr>
<td>Breakdown E (kV/mm)</td>
<td>15</td>
</tr>
<tr>
<td>Density (kg/m³)</td>
<td>4.3</td>
</tr>
<tr>
<td>Young's Modulus (GPa)</td>
<td>300</td>
</tr>
</tbody>
</table>

The capacitance value can be calculated as:

\[
C_{N1250} = \frac{\varepsilon_0 \cdot \varepsilon_{N1250} \cdot m \cdot l_{mean} \cdot w_{trace}}{d_{N1250}} \approx 1.4nF
\]  

(3-7)

Therefore each of the CM filters consists of three single-sided layers and one double-sided layer with N1250 ceramic substrate, and each layer has four turns per layer. Table 3-8 summarizes the CM choke design, and material properties are listed in Table 3-9.
Table 3-8. Summary of CM choke winding design.

<table>
<thead>
<tr>
<th>Total number of turns</th>
<th>216</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of layers</td>
<td>4</td>
</tr>
<tr>
<td>Number of double-sided layers</td>
<td>1</td>
</tr>
<tr>
<td>Number of single-sided layers</td>
<td>3</td>
</tr>
<tr>
<td>Number of turns per layer</td>
<td>4</td>
</tr>
<tr>
<td>Copper trace width</td>
<td>500 - 700µm</td>
</tr>
<tr>
<td>Space between copper traces</td>
<td>500 - 600µm</td>
</tr>
<tr>
<td>Copper thickness</td>
<td>70µm</td>
</tr>
</tbody>
</table>

Table 3-9. Material characteristics for CM windings.

<table>
<thead>
<tr>
<th></th>
<th>N1250 (Dielectric)</th>
<th>Kapton (Insulation)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relative permittivity</td>
<td>176</td>
<td>3.5</td>
</tr>
<tr>
<td>Thickness</td>
<td>150µm</td>
<td>50µm</td>
</tr>
</tbody>
</table>

(b) DM filter design

The DM inductor is realized by the leakage inductance of the CM choke. The intrinsic leakage inductance of the planar CM choke is usually not large enough to implement the total DM inductance. To increase the leakage inductance, an additional magnetic material can be inserted in the space between the two CM choke windings, as shown in Figure 3-28.

In Figure 3-28, the multilayer windings of the CM choke are simplified to a single-layer winding with the same total thickness. The error caused by this simplification is minor and can be neglected. Assuming uniform current distribution and applying Ampere’s law, the H field distribution in the winding window area can be obtained, as illustrated in Figure 3-28. The leakage inductance can be calculated using Eq. (3-8) [98].

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\[ L_{lk} = \mu_0 N^2 \frac{l_w}{b_w} \left( \frac{h_1 + h_2}{3} + \mu_r h_{\text{leak}} \right) \]  

(3-8)

where \( N \) is the turn’s number of the winding, \( l_w \) is the mean length per turn, \( h_1 \) and \( h_2 \) are the thickness of the windings, \( b_w \) is the winding width, and \( h_{lk} \) is the thickness of the leakage layer.

Figure 3-28. CM windings with a leakage layer in between.

The air gap between the magnetic core and the leakage layer, shown in Figure 3-29, will reduce the achievable leakage inductance dramatically and should be considered in the design. Due to processing limitations, it is difficult to reduce the air gap to less than 150\,\mu\text{m} for this integrated EMI filter design. Taking the air gap into consideration, the leakage inductance can be calculated from the following equation, where \( b_{\text{gap}} \) is the total length of the air gap.

\[ L_{lk} = \mu_0 N^2 \frac{l_w}{b_w} \cdot \frac{h_1 + h_2}{3} + \mu_0 \mu_r N^2 \frac{l_w}{b_w + (\mu_r - 1)b_{\text{gap}}} \cdot h_{\text{leak}} \]  

(3-9)
An LTCC ferrite material with a relative permeability of 200 is chosen as the leakage material. From Figure 3-30, knowing the required leakage inductance (400µH) and the relative permeability of the leakage material, the thickness of the leakage layer can be estimated as around 1.7mm.

A one-turn integrated LC structure connected as a pure capacitor is used for the DM capacitors. Considering the fact that a material with larger the permittivity is more sensitive to the temperature and the voltage bias, a very high permittivity material like Y5V is not chosen for
this design. The X7R material is used in this design, and the capacitance of one layer is not large enough for the DM capacitor, so two layers are paralleled to double the capacitance.

For each capacitor layer, a four-terminal transmission line connection method is used to minimize the ESL of $C_{DM}$, which is an important parasitic parameter that will influence the high-frequency DM attenuation. The two layers are connected in parallel with positive coupling, as shown in Figure 3-31. Table 3-10 summarizes the design of the DM capacitors.

![Figure 3-31. DM capacitor: a) four-terminal connection for each layer, (b) Paralleled connection.](image)

<table>
<thead>
<tr>
<th>Table 3-10. Summary of DM capacitor design.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dielectric material</strong></td>
</tr>
<tr>
<td><strong>Relative permittivity of X7R</strong></td>
</tr>
<tr>
<td><strong>Thickness of X7R</strong></td>
</tr>
<tr>
<td><strong>Number of layers in parallel</strong></td>
</tr>
<tr>
<td><strong>Calculated $C_{DM}$</strong></td>
</tr>
<tr>
<td><strong>Required $C_{DM}$</strong></td>
</tr>
<tr>
<td><strong>Total thickness of 2 DM capacitors</strong></td>
</tr>
</tbody>
</table>
(c) **Summary of the integrated EMI filter design**

Figure 3-32 illustrates the physical structure of the integrated EMI filter for the integrated ballast. A picture of the integrated EMI filter sample is shown in Figure 3-33. The measured DM and CM insertion voltage gains of the integrated filter are shown in Figure 3-34 and Figure 3-35, respectively. Both the DM attenuation and CM attenuation of the integrated EMI filter are better than that of the discrete EMI filter in the 10MHz-20MHz range.

Figure 3-32. Physical structure of the integrated EMI filter.

Figure 3-33. Prototype of the integrated EMI filter.
Figure 3-34. Measured DM insertion voltage gain of the integrated EMI filter.
3.3.4.2. **EPC cancellation for the integrated EMI filter**

In both discrete and integrated EMI filter implementations, the effective filter frequency range is limited because of the existence of parasitics of the filter components, such as the equivalent parallel capacitance (EPC) of the inductors, and the equivalent series inductance (ESL) of the
capacitors. It is clear that the high-frequency characteristic of EMI filters is mainly determined by parasitics [98, 103-105].

Figure 3-36 shows an example of the insertion voltage gain curve of a typical one-stage CM filter as a function of frequency. At frequency $f_{\text{EPC}}$, the insertion gain curve starts to divert from the ideal curve due to the self-resonance of the CM choke, which results in reduced HF attenuation. At frequency $f_{\text{ESL}}$, the HF attenuation is further reduced, which is due to the self-resonance of the CM capacitor. In a typical CM filter, the CM inductance is usually quite large, which requires a large number of turns for the CM winding and results in a large EPC as well. Therefore, in the CM filter, the EPC of the CM inductor is usually the most critical factor of the filter attenuation. When planar cores are used instead of toroidal cores to achieve low-profile structures, this problem becomes even worse. As a result, to improve HF filter performance, the EPC of the filter inductors must be effectively reduced.

![Figure 3-36. An example of insertion voltage gain of a CM filter.](image)
A. Concept of EPC cancellation

Several approaches have been proposed to reduce or cancel the EPC of filter inductors [95-98, 103-107]. In [106], an extra winding or RF transformer and a capacitor were introduced to cancel the effects of the winding capacitance. In [105], the theory of using mutual capacitance to cancel the effects of the parasitic capacitance of the inductors was proposed. In [96-98], the CM inductor is first center-tapped and only one grounded capacitor is inserted to its tap to cancel the EPC. The same concept is also implemented in the integrated EMI filter. An embedded conductive layer is inserted into the CM winding and grounded. The structural capacitance between the embedded layer and the CM winding is used to cancel the original EPC of the CM inductor. Below this EPC cancellation concept is further explored, and a general EPC cancellation condition is derived. Major influencing factors of EPC cancellation are analyzed and design guides are provided.

Considering an inductor $L$ with the equivalent parallel winding capacitance $C_e$ and neglecting the losses, the equivalent impedance of the inductor is given by: $Z_e = \frac{j\omega L}{1 - \omega^2 LC_e}$. If another resonance is introduced and the item of $\omega^2 L C_e$ is added into the denominator, when the equation $\omega^2 L C_e = \omega^2 L C_e$ is satisfied, the impedance can be simplified as: $Z_e = j\omega L$, which is the impedance of an ideal inductor.

To realize this idea, the inductor is split into two halves and a capacitor is connected from the center point to the ground, as shown in Figure 3-37 (a). The mutual inductance of the two winding halves is utilized to generate the second resonance. Assuming the coupling coefficient between the two winding halves is $k=1$, the decoupled T-equivalent circuit is shown in Figure 3-37 (b). By performing the $Y/\Delta$ transformation, Figure 3-37 (b) can be simplified to its $\pi$-
equivalent circuit, as shown in Figure 3-37 (c). The equivalent parameters in Figure 3-37 (c) are given by:

\[ Y_1 = Y_2 = \frac{1}{2} j\omega C_g \]  
\[ Y_{12} = \frac{1 + \omega L C_g - \omega^2 L C_g}{4 j\omega L} \]  

For Eq. (3-11), when \( C_e = 4C_c \),

\[ Y_{12} = \frac{1}{j\omega L} \]  
\[ Z_{12} = j\omega L \]

As a result, the parasitic winding capacitance is cancelled. The cancellation capacitor \( C_g \) can not only be implemented by an external lumped capacitor, it can also be realized by using the structural capacitance between the windings and the embedded ground layer [95-98].

![Figure 3-37. EPC cancellation concept](image)

Figure 3-37. EPC cancellation concept [96 R. Chen, et al, “Improving the Characteristics of Integrated EMI Filters by Embedded Conductive Layers”, IEEE Trans. on Power Electronics, vol. 20, May 2005, pp.611-619]: (a) Realization of EPC cancellation, (b) decoupled T-equivalent circuit, (c) \( \pi \)-equivalent circuit.
B. General EPC cancellation condition

In this EPC cancellation concept, the cancellation capacitor does not need to be inserted in the center point. Figure 3-38 shows a general case of the EPC cancellation. It is assumed that the turn’s ratio between the two winding halves is 1:n (n>=1); $C_1$ and $C_2$ represent the EPC of each winding part, and $C_3$ represents the inter-winding capacitance between the two winding parts. Assuming the coupling coefficient between the two winding parts is: $k$=1, the EPC of the inductor can be simplified as:

$$C_p = \frac{C_1 + n^2 C_2}{(n+1)^2} + C_3$$

(3-14)

The cancellation capacitor $C_g$ is inserted between these two winding parts. By performing the $Y/\Delta$ transformation, the $\pi$-equivalent circuit is solved. The parameters are given by the equations below.

$$Z_a = \frac{1}{j\omega \frac{n}{n+1} C_g}$$

(3-15)

$$Z_b = \frac{1}{j\omega \frac{1}{n+1} C_g}$$

(3-16)

$$Z_c = \frac{j\omega (n+1)^2 L}{1 + \omega^2 n L (C_g - \frac{C_1}{n} - nC_2 - \frac{(n+1)^2}{n} C_3)} = \frac{j\omega (n+1)^2 L}{1 + \omega^2 n L (C_g - \frac{(n+1)^2}{n} C_p)}$$

(3-17)

When $C_g = \frac{(n+1)^2}{n} C_p$, $Z_c = j\omega (n+1)^2 L$, which is an ideal inductor. Therefore the general cancellation condition is:

$$C_g = \frac{(n+1)^2}{n} C_p = \frac{C_1}{n} + nC_2 + \frac{(n+1)^2}{n} C_3$$

(3-18)
In order to verify the general cancellation condition, the insertion voltage gain of the inductor is simulated using the Saber simulation model shown in Figure 3-39. Simulation results are shown in Figure 3-40. In Figure 3-40 (a), the turn’s ratio is 1:2. By adding \( C_g = \frac{C_i}{n} + nC_2 + \frac{(n + 1)^2}{n}C_3 \), where \( n=2 \), the resonance in the insertion gain curve due to the EPC of inductor disappears. The inductor functions as an ideal inductor.

Figure 3-40 (b) shows the insertion gain changes slightly when the turn’s ratio changes, which means a different position in which to insert cancellation capacitor. Since \( C_g = \frac{(n + 1)^2}{n}C_p \) (\( n \geq 1 \)), with \( n \) increases, the required capacitance value of \( C_g \) increases. The impedance of \( Z_a \) and \( Z_b \), as expressed in Eqs. (3-15) and (3-16), shows that the inserted cancellation capacitor \( C_g \) is divided into two parts in the \( \pi \)-equivalent circuit: \( C_a = \frac{n}{n+1}C_g \), \( C_b = \frac{1}{n+1}C_g \). These two capacitors and the inductor form a \( \pi \)-filter. When the inductance value is the same, the higher capacitance value is, the higher the insertion gain will be.
Figure 3-39. General EPC cancellation simulation model.
Figure 3-40. General EPC cancellation simulation results: (a) Insertion gain at different $C_g$ at $n=2$, (b) Insertion gain at different $n$.

C. Influencing factors of EPC cancellation

In the above analysis and simulation, the inductor and capacitor are considered to have ideal coupling and no parasitics. In the real application, the effect of EPC cancellation will be reduced by these factors. In the following section, the critical influencing factors, such as the coupling coefficient between the winding parts, the ESL of the cancellation capacitor, and the coupling coefficient between the ESL of $C_g$ and the inductor parts, are analyzed.
Figure 3-41. EPC cancellation influencing factors.

(1) Effects of coupling coefficient between winding parts

When considering non-unity coupling coefficient $k_1 < 1$, the impedance of the $\pi$-equivalent circuit shown in Figure 3-38, can be derived using the same circuit transformation. When the turn’s ratio between two winding parts is 1: $n$ and the mutual inductance is $M = n k_1 L$, the derived impedances of the $\pi$-equivalent circuit are:

$$ Z_a = \frac{(n^2 + 2nk_1 + 1) - \omega^2 n^2 (1 - k_1^2)LC_g}{j\omega(n^2 + nk_1)C_g} \quad (3-19) $$

$$ Z_b = \frac{(n^2 + 2nk_1 + 1) - \omega^2 n^2 (1 - k_1^2)LC_g}{j\omega(1 + nk_1)C_g} \quad (3-20) $$

$$ Z_c = \frac{j\omega(L_1 C_n - \omega^2 n^2 (1 - k_1^2)LC_g)}{1 + \omega^2 nL C_g - \omega^2 L C_p [(n^2 + 2nk_1 + 1) - \omega^2 n^2 (1 - k_1^2)LC_g]} \quad (3-21) $$

For the impedance of the $\pi$-equivalent circuit, it is found that the resonance between the leakage inductance and the cancellation capacitor causes the EPC cancellation effect to suffer. The resonant frequency is given by:

$$ \omega_1 = \frac{\sqrt{n^2 + 2nk_1 + 1}}{\sqrt{n^2(1 - k_1^2)LC_g}} \quad (3-22) $$
When \( n=1 \), \( \omega_1 = \sqrt{\frac{2}{(1-k_1)LC_g}} \). Simulated insertion gain curves from the same simulation model with \( n=2 \) and difference coupling coefficient between inductor parts, \( k_1 \), are shown in Figure 3-42. The results show that the filter characteristics are very sensitive to the coupling coefficient between the two winding parts. The first parallel resonant frequencies in the simulation results match with the calculated frequencies from Eq. (3-22). In this simulation, the EPR of the inductor, which represents the losses of the inductor, is also considered; hence the insertion gain curve flattens due to the EPR effect.

![Figure 3-42. Effects of coupling coefficient between the inductor parts.](image-url)
(2) Effects of ESL of cancellation capacitor

The self-parasitic parameters of the cancellation capacitor $C_g$, especially the ESL of $C_g$, may also influence the filter characteristics. Simulation results indicate that the filter’s insertion gain is not very sensitive to ESL if there is no coupling between the ESL and main inductor parts. This is because in a decoupled T-equivalent circuit, ESL is in series with $-M$, and the ESL of $C_g$ usually is much smaller than $M$, so the influence of ESL is not significant.

However, if we consider the coupling between ESL of $C_g$ and the main inductor parts, $k_2=k_3>0$, the effect of ESL is more visible, and has the same trend as the effect of $k_1$. To differentiate the effect of ESL and $k_2$, $k_1$ is set to 1. To simplify the calculation, the $n=1$ case is considered. Then the parameters of the $\pi$-equivalent circuit can be derived as:

\[
Z_a = \frac{4L[1 - \omega^2\text{ESL}(1 - k_2^2C_g)]}{j\omega C_g \cdot (2L - 2\sqrt{L \cdot \text{ESL} \cdot k_2})} \quad (3-23)
\]

\[
Z_b = \frac{4L[1 - \omega^2\text{ESL}(1 - k_2^2C_g)]}{j\omega C_g \cdot (2L + 2\sqrt{L \cdot \text{ESL} \cdot k_2})} \quad (3-24)
\]

\[
Z_c = \frac{j \cdot 4\alpha L \cdot [1 - \omega^2\text{ESL}(1 - k_2^2C_g)]}{1 + \omega^2(L - \text{ESL}C_g - \omega^2C_p \cdot 4L \cdot [1 - \omega^2\text{ESL}(1 - k_2^2C_g)]} \quad (3-25)
\]

Therefore the resonant frequency is given by:

\[
\omega_z = \sqrt{\frac{1}{(1 - k_2^2)\text{ESL} \cdot C_g}} \quad (3-26)
\]

The simulated insertion voltage gain of the inductor with the cancellation capacitor is shown in Figure 3-43. The calculated resonant frequency matches with the simulated frequency well.
Figure 3-43. Effect of ESL of $C_g$ and coupling between ESL and inductor parts.

(3) Summary of influencing factors of EPC cancellation

Combining the effects of $k_1$, ESL, and $k_2$, the first parallel resonant frequency is given by the following equation when $n=1$:

$$\omega \approx \frac{1}{\sqrt{C_g \cdot \left[\frac{L(1-k_1)}{2} + ESL \cdot (1-k_2^2)\right]}} \quad (3-27)$$

which is also verified by the simulated insertion gain curve shown in Figure 3-44.
Eq. (3-27) shows that the resonant frequency is determined by the cancellation capacitance $C_g$, and the total effective leakage inductance. The higher the resonant frequency is, the better the cancellation performance can be achieved. To achieve higher resonant frequency, for a given $L$, $C_g$ and ESL should be as small as possible, while $k_1$, $k_2$ should be as large as possible. For a given original EPC, $C_p$, it is better to insert the cancellation capacitor in the middle, i.e. $n=1$, which results in the smallest required $C_g$. To achieve a high coupling coefficient, the winding structure needs to be designed carefully. In general, a planar structure is preferred to get high coupling.

![Figure 3-44. Effects of $k_1$, ESL and $k_2$.](image)

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A four-layer planar inductor is built for experimental verification. The cancellation capacitor is inserted in the middle. The parameters of the inductor are extracted by using an impedance analyzer. The extracted parameters are input into the Saber simulation model, as shown in Figure 3-45. The simulated insertion gain of this inductor with different cancellation capacitance values are shown in Figure 3-46, which matches the experimental results, as shown in Figure 3-47.
Figure 3-46. Simulated insertion gain.
Figure 3-47. Experimental results - insertion gain.
3.4. Experimental Verification of the Integrated Ballast

A prototype of the proposed integrated ballast has been built to demonstrate the improvement of the power density. A picture of the passive integrated ballast is shown in Figure 3-48. In the prototype, the active part is using the conventional surface mount and PCB technology. The dimensions of the prototype are 67mm (length) x 30mm (width) x 25mm (height), and the power density of the current prototype is 6.6W/in³, which is 1.5 times the power density of the discrete ballast.

The key waveforms and electrical characteristics of the integrated ballast are shown in Figure 3-49 to Figure 3-54. The results show that the integrated ballast can achieve almost the same electrical performance as the discrete ballast: high PF (> 98%), low $I_{THD}$ (< 10%), and constant output power over the 120±10% input voltage range. Only the efficiency is a little bit lower than the discrete ballast, which is mainly due to the higher losses on planar inductors $L_1$ and $L_2$.

Figure 3-48. Prototype of the passive integrated HID ballast: (a) top side, (b) bottom side.
Figure 3-49. Input voltage and current waveforms.

Figure 3-50. Lamp voltage and current waveforms at steady state.
Figure 3-51. Normalized output power as a function of input voltage.

Figure 3-52. Efficiency as a function of input voltage.
3.5. Summary

In this chapter, a passive integrated HID ballast is proposed and implemented. Packaging and integration technologies are explored to fully utilize the three-dimensional space, thereby improving the power density of the system. Technologies, design and implementation of power...
passive integration are explored. The power passives that are integrated include the integrated EMI filter, the integrated LC series resonator serving as the ignitor, and integrated LC output filter. Keeping the same electrical performance as the discrete ballast, and designing the components with an appropriate form factor, the volume utilization of the integrated ballast is increased to 80%, and the power density is increased to 6.6W/inch$^3$, which is 1.5 times the density of the discrete implementation. A prototype with integrated passive components was developed, and the preliminary experimental results show that the integrated ballast can achieve almost the same electrical performance as the discrete ballast.
4.1. Thermal Test Results of HID Ballast Prototype

The final target is to design the ballast, which will be installed inside the lamp fixture. This will most likely introduce a rather higher ambient temperature for the lamp ballast with a value around 60~70ºC. In order to study the thermal performance of the integrated ballast, temperature values of the key components are measured using K type thermal couples.

The temperature measurement set up is shown in Figure 4-1. The ballast operated under a 120Vdc input. It was not put in the original plastic case, but was covered by a quite large plastic box with the dimension of 60cm x 42cm x 30cm. The room temperature was around 25ºC. Temperatures of the inductors L1, L2, Mosfet S1, S2, and Cb are monitored within 2 hours of operation. The top surface of MOFET and Electrolytic capacitor Cb, and the inner surface of ferrite core of inductors are measured in this test. Figure 4-2 shows the thermal image of the integrated ballast, and the measured key components temperature is shown in Figure 4-3. In both figures, it is very clear that S1, L1, S2 are the top three hot spots as expected from the loss estimation, and the EMI filter and ignitor have low temperatures due to very low losses.
Figure 4-1. Temperature measurement set up.

Figure 4-2. Thermal image of HID ballast under 25°C ambient.
4.2. Thermal Simulation Model for the Integrated Ballast

In order to design an ultra compact ballast operating at a high ambient temperature, the thermal behavior of the integrated ballast needs to be studied and then the appropriate thermal management approaches are needed to retain the whole system under a certain temperature limit. For the power electronics system, it is too complicated to develop a mathematical model to study the thermal performance; instead, the FEM simulation tool is used to study the thermal behavior of the power converters [108, 109]. I-DEAS 12 simulation tool is used in this project.

I-DEAS is a powerful three dimensional thermal-fluid simulation software. Steps for the thermal simulation are listed as follows:

Step 1: Create model geometry using I-DEAS Master Modeler.
Step 2: Define finite Element (FE) model, assign material and physical properties.

Step 3: Define mesh for the FE model.

Step 4: Assign boundary conditions to the geometry, such as heat load, ambient temperature, vent condition, flow blockage condition.

Step 5: Run simulation and solve the model.

Step 6: Post process the results, such as temperature in solid or fluid, velocity-C.

4.2.1. Loss estimation

Before building the I-DEAS thermal model for the integrated ballast, the loss on each key component should be estimated. Since the thermal testing is under 120V_Dc input, losses of the key components under 120V_Dc input are estimated, and based on the loss estimation, heat loads are listed in Table 4-1. The total loss applied in the simulation is around 4W.

<table>
<thead>
<tr>
<th>Component</th>
<th>Heat load (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor L₁ Winding</td>
<td>0.65</td>
</tr>
<tr>
<td>Inductor L₁ Core</td>
<td>0.52</td>
</tr>
<tr>
<td>Inductor L₂ Winding</td>
<td>0.22</td>
</tr>
<tr>
<td>Inductor L₂ Core</td>
<td>0.4</td>
</tr>
<tr>
<td>Mosfet S₁</td>
<td>0.9</td>
</tr>
<tr>
<td>Mosfet S₂</td>
<td>0.3</td>
</tr>
<tr>
<td>Diode bridge</td>
<td>0.35</td>
</tr>
<tr>
<td>Diode D₆</td>
<td>0.25</td>
</tr>
<tr>
<td>Diode D₇</td>
<td>0.26</td>
</tr>
<tr>
<td>MOSFET S3/S4/S5/S6</td>
<td>0.033/0.033/0.033/0.033</td>
</tr>
</tbody>
</table>
4.2.2. IDEAs model of integrated HID ballast

Figure 4-4 shows the geometry model of the integrated ballast in I-DEAS thermal simulation. The model is constructed in I-DEAS with the master modeler tool. To simplify the simulation, all the components are modeled as a regular shape, such as square or cylindrical shape. Multi-layer PCB windings, electrolytic caps, and semiconductor devices are modeled as a uniform structure.

![Geometry model in I-DEAS thermal simulation tool.](image)

The required material property in the thermal simulation is the thermal conductivity. Thermal conductivity, \( k \), is the property of a material that indicates its ability to conduct heat. The thermal conductivities of most materials used in the integrated ballast are listed in Table 4-3.

However in the thermal simulation, most of the components with multi-material and complex structure are modeled as simple and uniform structure, approximate equivalent thermal
conductivities are needed for the simulation. For example, the thermal conductivity of the PCB is an estimated average value between the copper layer and the FR4 of the PCB. It may vary depending on the percentage of the copper area and the thickness of the copper layer and FR4 layer. Table 4-3 lists the approximate equivalent thermal conductivity of the components used in the simulation. These parameters have been tuned based on the following sensitivity.

Table 4-2. Thermal conductivity of materials in integrated ballast.

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal conductivity (W/m/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Air</td>
<td>0.025</td>
</tr>
<tr>
<td>FR4</td>
<td>0.23</td>
</tr>
<tr>
<td>Ferrite (MnZn)</td>
<td>3.5–5.0</td>
</tr>
<tr>
<td>Aluminum</td>
<td>205</td>
</tr>
<tr>
<td>Copper</td>
<td>401</td>
</tr>
<tr>
<td>Si</td>
<td>130</td>
</tr>
<tr>
<td>epoxy-molding compound</td>
<td>0.9–1</td>
</tr>
</tbody>
</table>

Table 4-3. Equivalent thermal conductivity of ballast components in I_DEAS model.

<table>
<thead>
<tr>
<th>Component</th>
<th>Equivalent thermal conductivity (W/m/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mosfet (DPAK), Diodes Bottom surface</td>
<td>240</td>
</tr>
<tr>
<td>Mosfet (DPAK), Diodes Molding</td>
<td>1</td>
</tr>
<tr>
<td>Copper</td>
<td>300</td>
</tr>
<tr>
<td>Ferrite core (MnZn)</td>
<td>4.5</td>
</tr>
<tr>
<td>SSPFC PCB</td>
<td>1.3</td>
</tr>
<tr>
<td>Inverter PCB</td>
<td>5</td>
</tr>
<tr>
<td>Motherboard PCB</td>
<td>7</td>
</tr>
<tr>
<td>Electrolytic cap</td>
<td>10</td>
</tr>
</tbody>
</table>
4.2.3. Sensitivity of the thermal conductivity of different materials

Both the preliminary simulation results and the tested results show that MOSFET S₁, S₂ and Inductor L₁ are the hottest components in the integrated ballast. So in the calibration we will first consider the temperature of MOSFETs, then the inductors and other components.

Temperatures of MOSFETs are determined by the losses of MOSFET and the thermal resistance from MOSFETs to the ambient. The losses of S₁ and S₂ are estimated in the previous part. Without forced air flow, the major heat transfer mechanism is the heat conduction from the MOSFETs to the copper traces, the SSPFC PCB and the motherboard PCB, then finally to the ambient. Therefore the thermal conductivity of the MOSFET, the SSPFC PCB and the motherboard PCB will be major influencing factors.

The SSPFC PCB and the motherboard PCB consist of FR4 (k=0.23 W/m/K) layers and copper (k=400 W/m/K) traces. In the simplified thermal model, both PCBs are modeled as a uniform block, therefore the equivalent thermal conductivity needs to be estimated based on the fill factor and copper thickness. For a double-layer PCB with 2oz Copper, the equivalent thermal conductivity is around 10~25 W/m/K with a fill factor of 30% ~ 60%.

In order to study the sensitivity of the thermal conductivity of different components, a bunch of simulations are conducted in IDEAS. Table 4-4 to Table 4-7 show the simulation results with the different thermal conductivity of the SSPFC PCB, the motherboard PCB, the MOSFET mold and the MOSFET bottom surface. The key component temperatures are listed in these tables.

The simulation results show that component temperatures are very sensitive to the thermal conductivity of the SSPFC PCB and the motherboard PCB. When these two thermal conductivities decrease, component temperatures increase.
Table 4-4 shows that the temperature difference between S1 and S2 is mainly determined by the thermal conductivity of SSPFC. Based on the testing results, the temperature difference between S1 and S2 is around 10°C. The simulation result from both Table 4-4 and Table 4-5 show that the thermal conductivity of SSPFC PCB should be no more than 2W/m/K in order to achieve the 10°C temperature difference in the simulation. However, a low thermal conductivity of SSPFC PCB will cause a high temperature of components. But if the thermal conductivity of SSPFC PCB is increased to achieve same temperature on S1 as in the testing results, the temperature difference between S1 and S2 will be much smaller than that in the test results.

It can be observed from Table 4-5 that the temperature difference between L1 and L2 is pretty much determined by the thermal conductivity of the motherboard PCB, since the motherboard PCB is the major path of the heat conduction for these two components. The higher the thermal conductivity is, the more heat is conducted from L1 through the motherboard PCB to L2, therefore the lower temperature difference between L1 and L2. Based on the testing results, the temperature difference is around 33°C. Therefore, the thermal conductivity of motherboard PCB should be around 5~10 W/m/K in the simulation model.

Table 4-6 shows that within a certain range, the component temperature is not sensitive to the thermal conductivity of the MOSFET mold. It is because the surface area of the MOSFET molding is much smaller than the surface area of the SSPFC PCB, so the heat transfer is mainly through the conduction of the SSPFC PCB. Component temperature is not sensitive to the thermal conductivity of the bottom surface as well, as shown in Table 4-7.
Table 4-4. Effect of thermal conductivity of SSPFC PCB (P_{S1}=0.9W, P_{S2}=0.3W).

<table>
<thead>
<tr>
<th>Thermal conductivity (W/(m.k))</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS _mold</td>
<td>MOS _surface</td>
</tr>
<tr>
<td>8</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>3</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>6</td>
</tr>
</tbody>
</table>

Table 4-5. Effect of thermal conductivity of motherboard PCB (P_{S1}=0.9W, P_{S2}=0.3W).

<table>
<thead>
<tr>
<th>Thermal conductivity (W/(m.k))</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS _mold</td>
<td>MOS _surf</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
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<tr>
<td>2</td>
<td>6</td>
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<tr>
<td>4</td>
<td>6</td>
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<tr>
<td>4</td>
<td>6</td>
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<tr>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>4</td>
<td>6</td>
</tr>
</tbody>
</table>
Table 4-6. Effect of thermal conductivity of MOSFET mold ($P_{S1}=0.9W$, $P_{S2}=0.3W$).

<table>
<thead>
<tr>
<th>Thermal conductivity (W/(m.k))</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$T_{max}$</td>
</tr>
<tr>
<td>SSPFC MOS mould MOS surface</td>
<td>Mother board</td>
</tr>
<tr>
<td>2 10 240 5 135 48.7 133 122 11</td>
<td></td>
</tr>
<tr>
<td>2 6 240 5 135 48.6 132 121 11</td>
<td></td>
</tr>
<tr>
<td>2 1 240 5 135 48.5 131 120 11</td>
<td></td>
</tr>
</tbody>
</table>

Table 4-7. Effect of thermal conductivity of MOSFET surface ($P_{S1}=0.9W$, $P_{S2}=0.3W$).

<table>
<thead>
<tr>
<th>Thermal conductivity (W/(m.k))</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$T_{max}$</td>
</tr>
<tr>
<td>SSPFC MOS mould MOS surface</td>
<td>Mother board</td>
</tr>
<tr>
<td>3.5 2 240 5 121 48.4 120 113 7</td>
<td></td>
</tr>
<tr>
<td>3.5 2 100 5 122 48.6 121 113 8</td>
<td></td>
</tr>
</tbody>
</table>

4.2.4. Thermal simulation results

It is assumed that the ballast is set in an ambient temperature of 25°C. The air vent is on the top of the circuit, and the gravity is from top to bottom when the ballast is set in the position as shown in the above picture. The ambient pressure is 101351 N/m². No forced air-flow is applied.

Figure 4-6 shows the simulated component temperature of the ballast. Key component temperatures are labeled in the figure, and measured temperatures are also labeled for comparison. The simulation results match with the measured results very well.
Since the ballast prototype is originally designed to be held in a plastic case, thermal simulation of the prototype within a plastic case under a 25°C ambient temperature is also conducted, and both the simulated component temperature and the simulated case temperature
are shown in Figure 4-7. It is shown that because the circuit is in an enclosed box and there is no efficient way to conduct heat out to the ambient, the temperature is very high on major thermal sources. $S_1$, $S_2$ and $L_1$ all have temperatures up to $161^\circ C$. 

(a)
Based on the simulation results, the prototype can’t survive if it is held in a plastic case, so necessary thermal management methods need to be applied in the prototype to reduce the component temperature. Thermal management methods will be analyzed, simulated and tested in the following part.

4.3. Thermal Management

4.3.1. Possible methods to reduce ballast temperature

There are several possible methods to reduce the temperature of the ballast. The first method is to use a high thermal conductivity material instead of plastic as the case so that more heat can be conducted to the ambient. It is expected that this method may not reduce the circuit temperature too much since most of the heat conducted to the case is via air convection, thermal
conduction and thermal radiation. If the heat that is finally conducted to the case is not significantly increased, the thermal improvement by using a high conductivity material would be insignificant.

The second method is to improve the air convection inside the case so that more heat can be carried out. This method may also have very limited improvement because the air convection inside the case is very limited. The case has only two small holes on the two sides. The air convection is contained in the case so that the heat carried out directly via air convection is very limited. Most of the heat will still be conducted to the ambient via the case.

The third method is to fill potting material inside the case. The potting material has a higher thermal conductivity so more heat can be directly conducted to the box. Since the thermal conduction is more efficient than air convection, air conduction and radiation, more heat can be conducted to the ambient. It is expected that the temperature may be greatly reduced if potting material is used. The potting material has a full or partial filling factor.

The fourth method is to optimize the component layout on the PCB so that the thermal sources do not crowd together. If thermal sources are close together, heat cannot be easily carried out so that the temperature is high. In order to do that, components with a high power loss should be located far away. One example is S1 and S2 are closed to the coupled inductor L1. All of them have a high power loss. If S1 and S2 are moved to the other places on the PCB such as the bottom of the motherboard, the thermal condition would be much better.

The fifth method is to use a heat-spreader on high power loss components such as S1 and S2. The heat-spreader has a high thermal conductivity so it can efficiently conduct heat. The heat spreader is attached to a piece of metal, such as one side of the case to further dissipate heat to the ambient.
The sixth method aims to reduce the temperature of the inductors, especially $L_1$. Inserting a high thermal conductivity material, such as aluminum nitride (AlN) laminates with thermal conductivity of 140~177W/m/K, to the ferrite core, will increase the effective thermal conductivity of the core and help conduct heat out more efficiently. However, in order to keep the design peak flux density, the size of the component needs to be increased. Another method is to increase the PCB winding trace width and copper thickness, which can both reduce the winding loss and increase the effective thermal conductivity of the PCB winding.

4.3.2. **Thermal simulation verification**

4.3.2.1. **Effects of case material**

It was expected that the metal case with the higher thermal conductivity would help reduce the component temperature. The simulation result with both plastic case and metal case are shown in Figure 4-8 and Figure 4-9, respectively. The case dimensions are the same, and the ambient temperature is 60°C. The thermal conductivities used in the simulation are 1W/m/K for the plastic box and 200W/m/K for the metal case (Al). The key components temperatures are listed in Table 4-8.
Figure 4-8. Simulated ballast temperature @Ta=60°C, with plastic case (k=1W/m/K): (a) component temperature, (b) case temperature.
Figure 4-9. Simulated ballast temperature $@T_a=60^\circ C$, with metal (Al) case ($k=200\text{W/m/K}$): (a) component temperature, (b) case temperature.
Table 4-8. Comparison of the key component temperature using different case material.

<table>
<thead>
<tr>
<th>Case material</th>
<th>Thermal conductivity (W/m/K)</th>
<th>Max</th>
<th>Min</th>
<th>S1_surface</th>
<th>S2_surface</th>
<th>L1</th>
<th>L2</th>
<th>Case_max</th>
<th>Case_min</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic</td>
<td>1</td>
<td>180</td>
<td>106</td>
<td>178</td>
<td>175</td>
<td>172</td>
<td>125</td>
<td>134</td>
<td>83.5</td>
</tr>
<tr>
<td>Al</td>
<td>200</td>
<td>158</td>
<td>102</td>
<td>156</td>
<td>155</td>
<td>150</td>
<td>115</td>
<td>104</td>
<td>102</td>
</tr>
</tbody>
</table>

By changing the case material from plastic to metal (Al), the maximum component temperature reduced by 22°C, a 12% reduction. The maximum case temperature is reduced by 30°C, which is a 22% reduction, and the temperature is more uniformly distributed over all the metal case.

4.3.2.2. Effects of ballast orientation

The orientation of the ballast may influence the thermal performance because it affects the air convection, which helps carry heat out from thermal sources. It has been analyzed before that the box has two very small holes, so the air convection is not good. As results, the heat directly carried out via air convection is very limited. The thermal improvement is therefore not good. The simulation results show that the weight direction does not affect the temperature of the ballast components and box. This verifies the analysis above.

4.3.2.3. Effects of potting

It is expected that the potting can efficiently conduct heat to the box so that the temperature of the components can be greatly reduced. From the preliminary simulation results, after the potting material is used, the maximum component temperature is dramatically reduced for both
the plastic box and the metal box. The improvement is so significant that it is the best method to reduce component temperatures so far.

The simulation results are shown in Figure 4-10 and Figure 4-11, and the temperatures of the key components are compared with the non-potted case in Table 4-9. The maximum component temperature is reduced by 59°C and 42°C for plastic case and metal case, respectively.

Adding potting material can also slightly reduce the maximum temperature of the plastic case. However, the temperature of the metal box won’t change much. In this simulation, only 1°C reduction, and in some case the case temperature may even increase a little. This is because the potting material efficiently carries the heat to the box, which can effectively reduce the component’s temperature.
Figure 4-10. Simulation results: plastic (k=1) case with potting (k=1): (a) component temperature, (b) case temperature.
Figure 4-11. Simulation results: metal (k=200) case with potting (k=1): (a) component temperature, (b) case temperature.

Table 4-9. Effects of potting.

<table>
<thead>
<tr>
<th>Case</th>
<th>Potting</th>
<th>max</th>
<th>min</th>
<th>S1_surface</th>
<th>S2_surface</th>
<th>Case_max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic case w/o potting</td>
<td>1</td>
<td>N/A</td>
<td></td>
<td>180</td>
<td>106</td>
<td>178</td>
</tr>
<tr>
<td>Plastic case with potting (k=1)</td>
<td>1</td>
<td>1</td>
<td>121</td>
<td>97</td>
<td>113</td>
<td>111</td>
</tr>
<tr>
<td>Metal case w/o potting</td>
<td>200</td>
<td>N/A</td>
<td></td>
<td>158</td>
<td>102</td>
<td>156</td>
</tr>
<tr>
<td>Metal case with potting (k=1)</td>
<td>200</td>
<td>1</td>
<td>116</td>
<td>102</td>
<td>108</td>
<td>107</td>
</tr>
</tbody>
</table>
In the previous simulation, the thermal conductivity of the potting material is 1W/m/K. In order to study the sensitivity of the potting material property, the thermal conductivity of potting is changed from 1 to 4 in the following simulation. The simulation results are shown in Figure 4-12, and the key component temperature are compared in. Since the thermal conductivity range for the potting material cannot be very large, the temperature difference due to different potting material is not that significant.
Figure 4-12. Simulation results with different potting materials, plastic case: (a) $k_{potting}=1\,\text{W/m/K}$, (b) $k_{potting}=2\,\text{W/m/K}$, (c) $k_{potting}=4\,\text{W/m/K}$.
Table 4-10. Sensitivity of potting materials.

<table>
<thead>
<tr>
<th>Case Potting (k=1)</th>
<th>Thermal conductivity (W/m/K)</th>
<th>Temperature (°C) (Ta=60°C)</th>
<th>Max</th>
<th>Min</th>
<th>S1_surface</th>
<th>S2_surface</th>
<th>Case_max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic case with potting (k=1)</td>
<td>1</td>
<td>1</td>
<td>121</td>
<td>97</td>
<td>113</td>
<td>111</td>
<td>112</td>
</tr>
<tr>
<td>Plastic case with potting (k=2)</td>
<td>1</td>
<td>2</td>
<td>115</td>
<td>97.9</td>
<td>109</td>
<td>108</td>
<td>109</td>
</tr>
<tr>
<td>Plastic case with potting (k=4)</td>
<td>1</td>
<td>4</td>
<td>112</td>
<td>99</td>
<td>107</td>
<td>106</td>
<td>107</td>
</tr>
</tbody>
</table>

In the real product, usually only partial potting is used considering weight, and parasitic effect. In the following simulation, full potting and half potting are compared in Figure 4-13 and Table 4-11. For the half-potted ballast, the maximum component temperature is increased by 21°C when compared with fully-potted condition, because MOSFET S2 is not covered by potting resin. However, when compared with the non-potted ballast, there is still a significant reduction in the maximum temperature. If the ballast layout is rearranged so that both hot MOSFETS will be on the bottom part of the ballast, half potting will be enough to reduce the maximum temperature.
\[ T_{\text{plastic_case_max}} = 134^\circ \text{C} \]
Figure 4-13. Simulation results with different ratio of potting (k=1), plastic box: (a) no potting, (b) half potting, (c) full potting.
Table 4-11. Sensitivity of potting ratio.

<table>
<thead>
<tr>
<th>Case</th>
<th>Potting</th>
<th>Max</th>
<th>Min</th>
<th>S(_{1_surf})</th>
<th>S(_{2_surf})</th>
<th>Case(_{\text{max}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic case w/o potting</td>
<td>1</td>
<td>180</td>
<td>106</td>
<td>178</td>
<td>175</td>
<td>134</td>
</tr>
<tr>
<td>Plastic case with 50% potting</td>
<td>1</td>
<td>142</td>
<td>97.3</td>
<td>124</td>
<td>140</td>
<td>125</td>
</tr>
<tr>
<td>Plastic case with 100% potting</td>
<td>1</td>
<td>121</td>
<td>97</td>
<td>113</td>
<td>111</td>
<td>112</td>
</tr>
</tbody>
</table>

4.3.2.4. Effects of heat spreader

MOSFETs S\(_1\), S\(_2\) and inductor L\(_1\) are three major heat sources. In order to reduce the temperature of these three components, an idea is to attach a metal plate to these three components to conduct the heat from them to the ambient. The simulation result is shown in Figure 4-14. The original simulation result without the heat spreader is also shown for comparison. There are almost no changes in the temperature of S\(_2\) and L\(_1\). The surface temperature of S\(_1\) is reduced by around 10°C. However, the maximum temperature, that is, the S\(_1\) junction temperature, is only reduced by 4°C. This is because the thermal conductivity of the MOSFET plastic package and ferrite core is small, which results in a large thermal resistance from junction to the surface of the components, and adding the heat spreader can’t reduce this part of thermal resistance. If the heat spreader is attached to the metal lid, the component temperature can be further reduced. The simulation will be shown in the following part and compared with the experimental results.
Figure 4-14. Simulated ballast temperature @Ta=60°C, w/o case: (a) without heat spreader, (b) with heat spreader.
4.3.3. Summary on thermal management simulation

The effects of the heat management method simulated above are summarized as follows.

The effect of the heat spreader depends on the surface area and how to attach the heat spreader to hot components. In this case, since the heat spreader is attached to the printed surface of the device, which has a low thermal conductivity, the heat spreader’s effect is suffered. If the heat spreader can be attached to the copper pad, which directly connected to the drain of the device, the component temperature can be further reduced.

Potting compound can greatly reduce the high temperature components, such as, S1, S2 and L1, and make the temperature more evenly distributed in the whole ballast. In some cases, adding potting compound may increase the temperature of some components which needs to have low temperature, such as electrolytic capacitors. In this design, potting actually also reduce the temperature of the electrolytic capacitor.

For the plastic case, adding a metal lid attached to the heat spreader will help extract the heat and decrease the temperature of the devices. However, compared to open-air case, the metal lid will block the air flow, so the temperature of the other components will increase.

Replacing the plastic case with the metal case can effectively reduce the component temperature when there is an effective conduction path from the heat load, such as potting compound, or heat spreader.

4.4. Experimental Verification of the Thermal Management Methods

There are two purposes of the thermal simulation in this chapter, which is needed to verify both the original thermal model of the prototype and also the thermal management method discussed above. Considering the first purpose, feasible thermal management methods with the
existing ballast prototype should be considered in the simulation. The prototype has been simulated and tested under open-case condition, and results match well. In the previous simulation, adding potting material can greatly reduce the temperature. The following two cases are simulated and measured with the current prototype.

**Case 1:** No potting, no case, metal lid, heat spreader on $S_1$, $S_2$ and attached to metal lid.

The measured temperature and simulation results of Case 1 are shown in Figure 4-16 and Figure 4-15, respectively. Key component temperatures are compared in Table 4-12. Relative error in percentage is also shown in the table. It shows that the testing results match with the simulation result very well.

![Figure 4-15. Temperature testing results of prototype with heat spreader and metal lid (Case 1).](image)
Figure 4-16. Simulation results of Case 1.
Table 4-12. Comparison between testing results and simulation results of Case 1.

<table>
<thead>
<tr>
<th>Case 1</th>
<th>( S_1 )</th>
<th>( S_2 )</th>
<th>( L_1 )</th>
<th>( L_2 )</th>
<th>( D_6/D_7 )</th>
<th>( C_b )</th>
<th>EMI filter</th>
<th>Ignitor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulated Temp. (°C)</td>
<td>77</td>
<td>75</td>
<td>110</td>
<td>67</td>
<td>100</td>
<td>61</td>
<td>76</td>
<td>60</td>
</tr>
<tr>
<td>Measured Temp. (°C)</td>
<td>79</td>
<td>76</td>
<td>103</td>
<td>64</td>
<td>103</td>
<td>61</td>
<td>79</td>
<td>55</td>
</tr>
<tr>
<td>Error (%)</td>
<td>-2.5%</td>
<td>-1.3%</td>
<td>6.8%</td>
<td>4.7%</td>
<td>-2.9%</td>
<td>0%</td>
<td>-3.8%</td>
<td>9.1%</td>
</tr>
</tbody>
</table>

**Case 2:** Partial potting (bottom half and electrolytic capacitors are included), plastic case, metal lid, heat spreader on \( S_1 \), \( S_2 \) and attached to metal lid.

The simulation results and the measured temperature of case 2 are shown in Figure 4-17 and Figure 4-18. In this test, the ballast prototype with heat spreader is put inside the plastic case, and potting compound is filled on the bottom part of the case. Potting compound reaches the height of 16mm. A metal lid is attached to the heat spreader. The thickness of the heat spreader is 0.5mm, and the thickness of the metal lid is 1mm. K type thermal couples are used to measure key components temperatures. The ambient temperature is 26°C. The measured result is labeled in Figure 4-18.

Table 4-13 shows the comparison between the testing results and simulation results of Case 2. It shows that the measured temperature values of most of the components are higher than the simulated value, except \( L_2 \), \( C_b \) and the ignitor. These three components generate small heat themselves, and are mainly heat absorber. Therefore, the discrepancy between the simulation and measurement is probably due to the over estimation of the thermal conductivity of the potting compound. In the real case, the thermal conductivity of the potting compound may be lower than the 0.7W/m/K used in the simulation. So the heat conduction to the components and the ambient is not as efficient as in the simulation.
Figure 4-17. Thermal simulation results of Case 2: (a) Component temperature, (b) plastic case temperature.
Figure 4-18. Temperature testing results of Case 2: (a) temperatures of the plastic case and the metal lid, (b) component temperatures.

Table 4-13. Comparison between testing results and simulation results of Case 2.

<table>
<thead>
<tr>
<th>Case 2</th>
<th>S_1</th>
<th>S_2</th>
<th>L_1</th>
<th>L_2</th>
<th>D_6/D_7</th>
<th>C_b</th>
<th>EMI filter</th>
<th>Ignitor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulated Temp. (°C) (k_{potting}=0.7)</td>
<td>72</td>
<td>69</td>
<td>86</td>
<td>71</td>
<td>80</td>
<td>67</td>
<td>78</td>
<td>63</td>
</tr>
<tr>
<td>Measured Temp. (°C)</td>
<td>80.3</td>
<td>74</td>
<td>96.6</td>
<td>66</td>
<td>93.4</td>
<td>67</td>
<td>83</td>
<td>58.4</td>
</tr>
<tr>
<td>Error (%)</td>
<td>-10.3%</td>
<td>-6.8%</td>
<td>-11%</td>
<td>7.6%</td>
<td>-7.9%</td>
<td>0%</td>
<td>-6.0%</td>
<td>9.2%</td>
</tr>
</tbody>
</table>

4.5. Theoretical Design of 35 cm³ Integrated Ballast

The size of the current prototype without case is 66mm (length) x 30mm (width) x 25mm (height), which in total is around 50cm³. It is still larger than the preliminary target size 35cm³.

In this chapter, the theoretical design of a 35cm³ integrated ballast is proposed, and the thermal simulation results of the 35cm³ design will also be provided and discussed.
4.5.1. Layout design considerations

Based on the current prototype design and the thermal management simulation results, the following aspects need to be considered in the theoretical 35cm³ ballast design.

From a size point of view:

a) The cylindrical shape electrolytic capacitor is replaced by the square shape capacitor to use the space more efficiently. The size of the square shape electrolytic capacitor $C_b$ is estimated to be 5mm x 20mm x 30mm.

b) Since the total component volume is already approaching 35cm³, there is no room for extra footprint for the input and output power cords. The space for the input and output power cords is not considered in this theoretical design.

c) Since some components in the SSPFC daughter board will be moved to the motherboard, so the left components of the SSPFC stage and inverter stage can be assembled in one daughter board to save the space.

From a thermal point of view:

a) In the current prototype, heat sources are too crowded, so in the 35cm³ design, it is better to separate these hot components, such as MOSFETs $S_1$, $S_2$ and inductor $L_1$. One idea is to move $S_1$ and $S_2$ to the bottom side of the motherboard, separate them as much as possible, and provide larger enough area of the copper traces connected to the drain of the MOSFETs.

b) Add potting compound to cover hot components.

c) Use a metal case to help conduct the heat out to the ambient. To fully utilize the heat sink effect of the metal case, it is better to attach all bottom devices and inductors to the metal
case. After rotating the EMI filter, \( L_1 \), \( L_2 \) and the daughter board, \( L_1 \) can be attached to the metal case.

From the above considerations, if the passive component design stays the same, the component layout of the 35cm\(^3\) design can be pretty much determined. From an electrical performance point of view, the new layout probably will enlarge the distance between the EMI filter and inductors \( L_1 \), \( L_2 \). Therefore the coupling effect between the EMI filter and the converter inductors is supposed to be reduced, which hopefully will reduce the EMI noise of the integrated ballast. On the other hand, parasitic parameters may increase due to a longer power delivering path, which may influence the operation condition and efficiency of the ballast. A four-layer PCB can be considered to reduce the parasitic parameters and increase the efficiency.

### 4.5.2. Layout of 35cm\(^3\) integrated ballast

Figure 4-19 shows the proposed layout design of the 35cm\(^3\) integrated ballast. The dimensions are 30mm (width) x 47mm (length) x 25mm (height). A square shape electrolytic capacitor is used with size of 30mm x 20mm x 5mm. The EMI filter, \( L_1 \), \( L_2 \) and SSPFC board (including inverter stage) are rotated by 90°, so \( L_1 \) can be attached to the side of the metal case. MOSFETs \( S_1 \) and \( S_2 \) are moved to the bottom side of the motherboard PCB, and attached to the metal case for better thermal conduction as well. The potting compound is going to be filled within the left part of the ballast, covering the EMI Filter, SSPFC & inverter board, \( L_2 \), \( L_1 \), the diode bridge, and \( S_1 \) & \( S_2 \) on the bottom side.
Figure 4-19. Proposed Layout of 35cm³ integrated ballast with metal case: (a) inside view without lid, (b) bottom side of ballast PCB (without case).
4.5.3. 35cm³ design simulation results

The thermal conductivities used in the following simulations are almost the same as the existing design except the thermal conductivity of the SSPFC & inverter PCB is changed to 3.2W/m/K, and the thermal conductivity of the motherboard PCB is increased to 2.8W/m/K or 4.2W/m/K.

The motherboard’s thermal conductivity is higher than the existing design considering S₁ and S₂ are on the bottom of motherboard so more copper is used for heat dissipating. The thermal conductivity of the SSPFC & Inverter PCB is the average value of the original SSPFC PCB and the inverter PCB since they are combined together in 35cm³ design.

The simulation condition is: Partial Potting (Electrolytic capacitors are not included), use metal Case, L₁ attached to case, S₁, S₂ on the bottom and attached to metal case, the ambient temperature is 60°C.

Case 1: Partial Potting (Electrolytic capacitors are not included), metal case, L₁ attached to case, S₁, S₂ on the bottom, and attached to case. k\text{potting}=1, \ k_{MB}=4.2 \ W/m/K, \ k_{SSPFC}=3.2 \ W/m/K, \ T_a=60°C.

Figure 4-20 shows that the temperature is much more evenly distributed in the 35cm³ design after applying all the thermal management method. The highest temperature is on the bottom of S₁ (128°C). The lowest temperature is 120°C. However, since the lowest temperature in the simulation is already higher than the highest component temperature limit (around 115°C), the 35cm³ design cannot survive at 60°C ambient temperature based on this simulation.

By increasing the thermal conductivity of the potting material from 1 W/m/K to 2 W/m/K, there is only 3°C reduction. The very limited temperature reduction indicates that thermal conductivity of potting is not the major barrier for the 35cm³ design.
(a)
Case II: Partial Potting (Electrolytic capacitors are not included), metal case, $L_1$ attached to case, $S_1$, $S_2$ on the bottom, and attached to case. $k_{\text{potting}}=2$, $k_{MB}=4.2$ W/m/K, $k_{SSPFC}=3.2$ W/m/K, $T_a=60^\circ C$. $k_{\text{PCBWinding}}=40$, $P_{S1}=0.25W$, $P_{S2}=0.17W$.

Assuming the power losses of MOSFETs $S_1$ and $S_2$ can be reduced to 0.25W and 0.17W by using a transition mode control and using better devices, and the thermal conductivity of PCB winding can be increased to 40W/m/K by a better winding design. Figure 4-21 shows the simulation results. It is shown that the temperature is still very high; there is only a 10°C reduction in the highest temperature compared to Case I. $D_6$ and $D_7$ have the highest temperature of 118°C. The lowest temperature is 113°C, which is still higher than the maximum allowed component temperature for the ballast.
4.5.4. Summary of 35cm$^3$ design

The thermal simulation results of the proposed 35cm$^3$ ballast design are shown in the previous part. Even with reduced losses on MOSFETs S$_1$ and S$_2$, increased thermal conductivity of potting compound and PCB winding, the highest component temperature is around 118$^\circ$C, and the lowest component temperature is around 113$^\circ$C. Table 4-14 shows the temperature limits for the ballast components. Comparing the simulation of case II with Table 4-14, the lowest temperature is already higher than the highest temperature limit for ballast components. For semiconductor devices and inductors, the distance to the target temperature is not that far, but for most of the ICs and electrolytic capacitors, around 25$^\circ$C ~30$^\circ$C needs to be reduced to meet the requirement.
If the ballast with case is installed in an enclosed lamp fixture as in the real case, the situation will be much worse.

Table 4-14. Ballast component temperature limits.

<table>
<thead>
<tr>
<th>Component</th>
<th>Operating temperature range (°C)</th>
<th>Simulated temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Junction</td>
<td>Ambient</td>
</tr>
<tr>
<td>Mosfet</td>
<td>STD5NM60</td>
<td>-55~150</td>
</tr>
<tr>
<td>Diode</td>
<td>MUR260</td>
<td>-65~175</td>
</tr>
<tr>
<td>IC</td>
<td>UC3845A</td>
<td>-55~150</td>
</tr>
<tr>
<td>IR2181</td>
<td></td>
<td>~150</td>
</tr>
<tr>
<td>AD633JR</td>
<td></td>
<td>0~70</td>
</tr>
<tr>
<td>LM7805</td>
<td></td>
<td>0~125</td>
</tr>
<tr>
<td>LM324</td>
<td></td>
<td>0~70</td>
</tr>
<tr>
<td>87LPC764</td>
<td></td>
<td>0~70</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Electrolytic cap</td>
<td>-40~125</td>
</tr>
<tr>
<td>Inductor</td>
<td>3E5 ferrite</td>
<td>~125</td>
</tr>
<tr>
<td></td>
<td>3F3 ferrite</td>
<td>~200</td>
</tr>
</tbody>
</table>

Considering an ideal scenario, a ballast with a power dissipation of $Q$ and a surface area of $A$ is put in the air with an ambient temperature of $T_a$. The whole ballast is treated as a thermally uniform block. The surface temperature of the block can be calculated from the following equation:

$$T_s = T_a + \frac{q}{h} = T_a + \frac{Q}{A \cdot h}$$  \hspace{1cm} (4-1)$$

Where $h$ is the convection coefficient.
Given the ambient temperature (60°C), maximum allowable surface temperature (90°C), and component surface area of the current 35cm³ design, the maximum allowable losses of the component is proportional to the convection coefficient, as shown in Figure 4-22. For free convection condition without any forced air, the convection coefficient is 5~25 W/(m²K). For a typical value h=15 W/(m²K), the maximum allowable loss is 3W, which is 1W lower than the losses in the current prototype.

![Figure 4-22. Maximum allowable losses as a function of the convection coefficient.](image)

The above simulation results show that the temperature difference between maximum and minimum temperature is only 5°C in the proposed 35cm³ ballast. It means the temperature distribution of the 35cm³ design is already very even. So the major barrier to reduce the temperature of the integrated ballast is the losses and the loss handling capability of the ballast.

Based on the above observation, in order to reduce the ballast temperature, the most effective methods are: 1) reducing the power losses of the ballast; 2) increasing the convection
coefficient; 3) increasing the equivalent surface area of the ballast which can radiate the heat to the ambient.

For given electrical design of the ballast, the power loss of the ballast is fixed. For the track lighting application, adding forced air flow to increase the convection coefficient is also not a practical solution due to its high cost. So how to increase the equivalent surface area is the key for the integrated ballast to survive at such a harsh environment.

Generally, from a shape point of view, different shape results in different surface area for given ballast size. It is clear that a flat ballast with a low profile will have a larger surface area compared with a square shape ballast with the same volume. However, in the track lighting application, the ballast with the case will be installed in the enclosed lamp fixture. In order to be close to the best scenario, the best solution is to attach the ballast with a metal case to the metal fixture of the HID lamp. The attachment between the ballast and the lamp fixture should have small thermal resistance, and the shape of the lamp fixture needs to be carefully designed to have a large surface area. For example, with a limited volume, adding fins to the lamp fixture can be considered to further increase the surface area.

In the best scenario, the ballast combined with the lamp fixture is considered a thermally uniform solid block. In order to make the real case more close to the ideal case, the following methods can be considered. The first method is to add heat spreaders to all major heat sources directly. This means the heat spreader is directly attached to the bottom of S₁, S₂, D₆, D₇ and the diode bridge. The L₁ and L₂ should be directly attached to the metal case too. However, this is practically difficult for surface mount components. Previous cases attach heat spreaders and metal case to the epoxy of devices, the heat cannot be most efficiently conducted to the ambient. The second method is to fill the case with the potting material with a higher thermal conductivity.
will help carry out the the heat. Thirdly, choosing a core material with higher thermal conductivity will definitely be a very good alternative to reduce the component temperature, because there is a lot of space and weight that is occupied by the core. So investigation of the core material is needed to find the answer, and so is the PCB material.

4.6. Summary

The target of this research is to build an ultra compact HID ballast, which can be installed inside the lamp fixture, where the ambient temperature is near 60°C. In order to investigate the feasibility of the integrated ballast with a target size of 35cm³ under such a severe thermal condition, the thermal behavior of the current prototype with a volume of 50cm³ is studied under different conditions, and a thermal simulation model is built in I-DEAS, and calibrated based on the experimental results to help analyze the thermal behavior of the future 35cm³ designs.

From the thermal simulation results, the current prototype can’t survive under 60°C ambient whether in a plastic case or not. The major reasons are: 1) losses are high. 2) Heat sources are too crowded together. 3) Free air convection is not efficient enough to carry heat out to ambient, and the situation is even worse if the ballast is inside the case.

The potting compound, heat spreader and metal case are proposed to reduce the component temperature. Both simulation results and experimental results are provided and compared for the existing prototype. The simulation results show that filling potting compound is the most effective method to reduce the temperature.

Based on the simulation and experimental results, a theoretical 35cm³ design is proposed. A square shape electrolytic capacitor is used to replace the cylindrical shape capacitor. Heat sources, such as semiconductor devices and inductor are separated as much as possible, and
attached to a metal case for better heat conduction. The potting compound will be filled within the left part of the ballast, covering the EMI Filter, the SSPFC & inverter board, L₂, L₁, the diode bridge, and S₁ & S₂ on the bottom side. The heat sources of the MOSFETs are also expected to be reduced by transition mode control.

I-DEAS simulation results show that by applying all the thermal management approaches, the proposed 35cm³ ballast has a very even temperature distribution, and a greatly reduced temperature compared with the current prototype. However, the lowest temperature is still higher than the temperature limit from a safety and lifetime point of view. Based on the analysis of the best scenario, attaching the ballast with the metal case to the metal fixture of the lamp, and carefully design the attachment and the fixture to maximize the surface area is the best solution for the ultral compact CHID for track lighting applications.

Acknowledgement

The author would like to thank Dr. Shuo Wang for his great help on the thermal simulation in this chapter.
Chapter 5. Conclusions and Future Work

5.1. Introduction

HID lamps have been widely used in both commercial and residential lighting applications due to their merits of high efficacy, long life, compact size and good color rendition. However, the typical three-stage structure has a large size and high cost, which unfortunately offsets the merits of HID lamps, especially in low wattage applications. In order to make HID lamps more attractive in low wattage and indoor applications, it is critical to reduce the size, weight and cost of HID ballasts.

A compact HID with a high power density built-in ballast installed inside the lamp fixture is proposed in this dissertation. The concept comes from the compact fluorescent lamp (CFL), but it is much more challenging than the CFLs considering the high power factor and low input current harmonic requirement, high ignition voltage requirement and acoustic resonance free requirement. Both circuit topologies and novel integration and packaging technologies are explored to achieve high power density of the HID ballast.

5.2. High Power Density HID Ballast

The first step to improve the power density is to simplify the system structure and circuit topology. Instead of a three-stage structure, a two-stage structure is proposed, which combines the PFC stage and DC/DC power regulation stage together into a single-stage PFC front-end, and followed by an unregulated DC/AC inverter/ignitor stage. To achieve both a high power factor,
low input current THD and a low bulky capacitor voltage stress within a wide load range is the major challenge for the single-stage PFC front-end.

An SSPFC AC/DC converter is proposed in this dissertation. A DCM non-isolated flyback PFC semi-stage and a DCM buck-boost DC/DC semi-stage share the semiconductor switch, driver and PWM controller, so that the component count and cost can be reduced. The proposed SSPFC AC/DC front-end converter can take advantage of the DCM operation of both PFC stage and DC/DC stage to achieve a near-unity power factor, low THD (less than 10%), low bulk capacitor voltage, and constant power regulation with a simple control circuit. Because the number of high-frequency switches is reduced compared to that of state-of-the-art two-stage HID ballast topologies, the switching frequency can be increased without sacrificing high efficiency, so the passive component size can be reduced. The power density of the whole ballast is increased using this two-stage structure.

A prototype of the proposed HID ballast is built. It achieves a high input PF of 0.996 and a very low input-current THD of 8%. The efficiency for the whole ballast is 84.2%. The power density of the entire ballast is 4.68W/inch³, which is twice the density of commercial products (2.4W/in³). The proposed two-stage HID ballast has been commercialized and was launched in the US market starting in June 2007. The new product features an even higher power density of 6W/in³, which counts for 2.5 times the power density of the previous commercial product.

The proposed SSPFC AC/DC front-end topology is very suitable for the low-power low-cost high performance ballast application. Due to the DCM operation of both inductors, this topology will start to see the limit for higher output power than 50W.
5.3. **System Integration for HID Ballast**

The power density of the converter in discrete fashion usually suffers from the poor three-dimensional (3D) volume utilization due to a large component count and the different form factor of different components. In the second step, integration and packaging technologies are explored to further increase the power density. A 3D passive integrated HID ballast is proposed in this dissertation. All power passive components are designed in planar shape with a uniform form factor to fully utilize the three-dimensional space. In addition, electromagnetic integration technologies are applied to achieve structural, functional and processing integration to reduce component volume and labor cost.

In the previous work, the spiral winding integrated LC structure has been successfully applied in power electronics, mainly in kilowatts systems, such as the LC resonator or the LCT or LLCT module in resonant converters for storing and processing electromagnetic energy at the switching frequency, and the integrated EMI filter for attenuating electromagnetic energy at the switching frequency and above. With the available materials and the processing technologies, the developed passive integration technology is applied in low wattage HID ballast application. It is the first demonstration of the power passive integration and filter integration in a whole system.

The whole ballast system is partitioned into two parts: the active part, including semiconductors like diodes and MOSFETs with their controller and drivers; and the power passive part, which includes inductors and capacitors. Since more than 90% of the component volume is occupied by large passive components, the passive integration is the key of the ballast integration.
Based on circuit functions, power passive components are further partitioned into several functional modules: the EMI filter, the ignitor and the LC output filter. Those passive components, that are not suitable for integration with other components due to material and processing limitations, such as the energy storage electrolytic capacitor $C_b$ and the coupled flyback inductor $L_1$, are optimized into a planar structure for better space usage and thermal performance.

In this integrated ballast, all the components are designed to have the same form factor, which enables the maximum usage of the 3D space. The volume utilization is expected to be increased to 80%.

The benefits of functional integration of the passive integration technology may be limited by material characteristics and processing technologies. In a functionally integrated LC module, the copper length and width is subject to the inductor design, while the total copper area is also related to the capacitor design. For given material characteristics, sometimes it is difficult to reach the minimum volume for the inductor and the capacitor at the same time. When there is a mismatch between the required copper area for the inductor and that for the capacitor, hybrid integration or structural integration can be alternative solutions.

Three type of the passive integration including functional, structural and hybrid integration are differentiated in the dissertation. All three types of passive integration are covered in the proposed integrated ballast. The EMI filter and the ignitor ($L_r$ and $C_r$) are implemented with a hybrid structure; the LC output filter ($L_2$ and $C_o$) is implemented by structural integration. The coupled inductor ($L_1$) is designed with the planar structure to have a better form factor. The design of each of the integrated passive components is discussed in the dissertation.
In the integrated EMI filter, EPC cancellation technology is applied to cancel EPC of the CM windings to improve the filter performance. In this dissertation, the EPC cancellation concept is further explored. A general EPC cancellation condition is derived. Major influencing factors of EPC cancellation are analyzed and design guides are provided as well.

All active components, including the MOSFETs, diodes and control circuitry, are divided into two parts according to the circuit function, i.e., the SSPFC stage and the inverter stage; implemented in two small PCBs with a shape consistent with the integrated passive modules, and vertically mounted on the motherboard PCB. A prototype of the proposed integrated ballast is developed with almost same electrical performance as the discrete prototype, while the power density is 6.6W/inch³, which is 1.5 times the density of the discrete prototype. Combining with further size reduction by using chip-on-board (COB) technology for the active part, and a better layout design, the integrated HID ballast is projected to double the power density of the discrete implementation.

5.4. Thermal Management for Integrated HID Ballast

By installing the HID ballast inside the lamp fixture, the ambient temperature for the ballast will be much higher than the conventional separately installed ballast, and combined with a reduced size, the thermal condition for the integrated ballast will be much more severe. In order to investigate the feasibility of the integrated ballast with a target size of 35cm³ under such a severe thermal condition, the thermal behavior of the current prototype with a volume of 50cm³ is studied under different conditions, and a thermal simulation model is built in I-DEAS, and calibrated based on the experimental results to help analyze the thermal behavior of the proposed 35cm³ designs.
From the thermal simulation result, the current integrated ballast prototype can’t survive under 60°C ambient whether in a plastic case or not. The major reasons are: 1) losses are high. 2) Heat sources are too crowded together. 3) Free air convection is not efficient enough to carry heat out to ambient, and the situation is even worse if the ballast is inside the case.

Several thermal management methods, such as adding potting compound, adding heat spreader and adding metal case are investigated using the IDEAS simulation model. Experimental verification of various thermal management methods is also provided for the existing prototype. The simulation results show that adding potting compound is the most effective method to reduce the temperature.

Based on the simulation and experimental results, a theoretical 35cm³ design is proposed. A square shape electrolytic capacitor is used to replace the cylindrical shape capacitor. Heat sources, such as semiconductor devices and inductor are separated as much as possible, and attached to a metal case for better heat conduction. The potting compound is to be filled in the the ballast case covering all the hot components.

I-DEAS simulation results show that by applying the above thermal management approaches, the proposed 35cm³ ballast has a very even temperature distribution, and a greatly reduced temperature compared with the current prototype. However, the lowest temperature is still higher than the temperature limit even with the reduced power losses of the ballast. Based on the analysis of the best scenario, it is observed that the major barrier to reduce the temperature of the integrated ballast is the high power loss and the low loss handling capability of the ballast. For given electrical design of the ballast, the power loss of the ballast is fixed. For the track lighting application, adding forced air flow to increase the convection coefficient is also not a
practical solution due to its high cost. So how to increase the equivalent surface area is the key for the integrated ballast to survive at such a harsh environment.

Generally, different shape results in different surface area for given ballast size. It is clear that a flat ballast with a low profile will have a larger surface area compared with a square shape ballast with the same volume. However, in the tracklighting application, the ballast with the case will be installed in an enclosed lamp fixture. In order to be close to the best scenario, the best solution is to attach the ballast with the metal case to the metal fixture of the HID lamp. The attachment between the ballast and the lamp fixture should have small thermal resistance. The shape of the lamp fixture needs to be carefully designed to have a large surface area. For example, with limited volume, adding fins to the lamp fixture can be considered to further increase the surface area.

5.5. Future Work

The following items are suggested as the future work of this dissertation:

Basically the further improvement of the power density will be limited by the thermal capability. In this dissertation, it has been observed that current circuit design with around 4W loss for 20W HID ballast has almost hit the loss handling capability limitation of a 35cm³ block. Further investigation on reducing the losses of the ballast circuit is needed, such as the reducing losses of inductors, and appropriate soft-switching techniques to reduce the output capacitance losses on MOSFETs.

The relationship between the ballast shape and the ballast thermal performance is also worthy of investigation.
In both the discrete and integrated version of the ballast prototype, EMI filter is still the largest passive component. In the experimental results, near field coupling effect is observed between the EMI filter and converter inductors, which deteriorate the EMI filter performance at low frequency range. Therefore, EMI performance of the integrated ballast needs further evaluation. And effective methods are needed to reduce or eliminate the near-field coupling effect, so that the EMI filter size would be further reduced.
References


[27] IEC 61000-3-2, Electromagnetic Compatibility Part 3: Limits, Section 2: Limits for Harmonic Current Emissions


