4.1 INTRODUCTION

In general, for a conventional two-stage PFC converter, the input current waveform and the bulk-capacitor voltage are well regulated, which are not critical. However, in the S\(^2\)PFC converters, the input current harmonics, bulk-capacitor voltage stress and overall conversion efficiency become very critical issues. A good design of the S\(^2\)PFC converter must find a careful trade-off among them. This chapter is going to provide further studies on the bulk-capacitor voltage stress and converter efficiency.

4.1.1 Bulk-capacitor voltage stress

In a S\(^2\)PFC converter, the bulk-capacitor voltage stress is critical since it is no longer regulated and increases while the RMS line voltage increases or load current decreases. In the basic DCM S\(^2\)PFC converter shown in Fig. 3.1, the capacitor voltage can be higher than 1000 V at high line light load. That is unacceptable. To solve this problem, the feedback-winding scheme has been proposed in order to limit the voltage stress to be lower than 450 V so that a 450 V-rated electrolytic capacitor can be used [B10].

In [B15] and [C5], the detailed analysis of the bulk-capacitor voltage \(V_B\) in the DCM S\(^2\)PFC converter has been present. It explains why the bulk-capacitor voltage \(V_B\) increases with output power decreases in the DCM S\(^2\)PFC converter. [C5] shows that the maximum voltage \(V_B\)
Chapter 4. Voltage and Current Stress of the S²PFC Converters and Their Design Considerations

(b) With CCM $L_B$, $V_B$ is reduced but still high, while input current has high distortion

Figure 4.1 Pushing $L_B$ into CCM mode reduces voltage stress $V_B$ of the DCM S²PFC converter
(c) The CCM $S^2$PFC converters achieve significantly lower $V_B$, while the input current waveforms are also improved.

Figure 4.2 Feed-forward component $L_1$ or $C_r$ significantly reduces $V_B$ stress in the CCM $S^2$PFC converters
decreases with the boost inductor \( L_B \) increases. If \( L_B \) further increase, the converter enters CCM mode and lost PFC function, but the capacitor \( V_B \) can be further reduced.

Figure 4.1(b) shows the capacitor voltage \( V_B \) vs. output power of the original integrated S\(^2\)PFC converter, at the highest input line voltage. It shows that \( V_B \) stress can be significant reduced by increasing \( L_B \) value and pushing it from DCM into CCM mode. The maximum \( V_B \) decreases from 1500 V to 700 V at high line and light load. Even though, it is too high for a 450 V-rated electrolytic bulk-capacitor. Furthermore, the CCM boost inductor current starts to have high distortion and can not meet the harmonics specifications.

Fortunately, as shown in Fig. 4.2, the CS and VS S\(^2\)PFC can further reduce the \( V_B \) stress significantly with CCM boost inductance \( L_B \), while the input current is also well shaped. In both the CS and VS S\(^2\)PFC converters, the maximum \( V_B \) is always lower than 450 V so that a 450 V-rated bulk-capacitor can be used. However, although there are some study published to discuss the design of the CCM CS S\(^2\)PFC converter [C3, C7, C8], no systematic study has been presented to explain why the bulk-capacitor voltage \( V_B \) is limited and how to design the circuit parameters to limit \( V_B \) in the CCM S\(^2\)PFC converters.

In summary, following questions need to be solved on the CCM S\(^2\)PFC capacitor voltage:

- Why the bulk-capacitor voltage \( V_B \) still increases with load decreases in CCM S\(^2\)PFC?
- Why the feed-forward component \( L_1 \) or \( C_r \) can reduce \( V_B \) stress?
- What is the general principle of the capacitor voltage \( V_B \)?
- How to design \( L_1 \) or \( C_r \) to control the capacitor voltage \( V_B \)?
- How to further reduce \( V_B \)?

The first part of this chapter will provide the answers of the above questions.
4.1.2 Converter efficiency and switch current stress

Other than the bulk-capacitor voltage stress, the efficiency is also important in the CCM $S^2$PFC converters. In a $S^2$PFC converter, since the power switch integrate both the PFC and the DC/DC stage, it needs to handle both currents. In general, the integrated switch has high current stress as well as high voltage stress. How to reduce the current stress on the integrated power switch and improve the efficiency is an important design issue.

In this chapter, analysis will shows that the feed-forward component can also reduce the switch current stress in both the CS and VS $S^2$PFC converters. Besides, it shows that the bulk-capacitor voltage feedback winding can further reduce the switch current stress.

In summary, the input current harmonics, the bulk-capacitor voltage stress and the converter efficiency are the three major issues in the $S^2$PFC converters. A good design always involves careful trade-off among these issues. To provide a design example, the CS $S^2$PFC design considerations and procedures are proposed in this chapter with experimental results. Besides, the design considerations of the VS $S^2$PFC converter is also discussed with simulated design curves.
4.2 STUDY ON THE BULK-CAPACITOR VOLTAGE IN CCM S\textsuperscript{2}PFC CONVERTERS

4.2.1 Capacitor voltage in the conventional boost converter

As shown in Fig. 4.1(a), since the original S\textsuperscript{2}PFC converter was developed by integrating the boost rectifier with the PWM DC/DC converter, it is very helpful to study the capacitor voltage stress in the conventional boost converter first. In this section, the boost converter bulk-capacitor voltage is analyzed for both the DCM and CCM cases. Figure 4.3(a) shows the boost circuit diagram for analysis.

4.2.1.1 Boost converter in DC/DC operations (open loop)

To simplify the problem, first, it is assumed that the boost converter is operated in the DC/DC converter mode with open loop control. It means if the input voltage is a constant value $V_{in}$, the switch duty-cycle $D$ is also constant. The boost inductor has identical switching waveforms in each switching cycle.

a) DCM mode operation

Figure 4.3 (b) shows the input inductor current in DCM mode. Following equations can be derived from its waveform (open-loop):

$$I_{PK} = \frac{V_{in}}{L_B} \cdot DT_S = \frac{V_B - V_{in}}{L_B} \cdot D_1 T_S$$

(4.1)

$$I_{LB(ave)} = \frac{1}{2} \cdot I_{PK} \cdot (D + D_1)$$

(4.2)

According to the power balance between input and output of the boost stage:

$$V_{in} \cdot I_{LB(ave)} = \frac{P_0}{\eta}$$

(4.3)

where $\eta$ is the boost converter efficiency.
Figure 4.3 Conventional boost converter and its different operation modes

(a) Circuit diagram, (b) DCM operation $i_{LB}$ waveform, and (c) CCM operation $i_{LB}$ waveform.
From Eq. (4.1) – (4.3), the bulk-capacitor voltage of the DCM boost converter is derived as:

\[
V_B = \frac{V_{in}}{1 - \frac{1}{2} \left( \frac{V_{in}^3}{L_B \cdot f_s} \right) \cdot D^3 \cdot \frac{1}{P_o / \eta}}
\]  

(4.4)

According to Eq. (4.4), the relationship between \(V_B\) and other circuit parameters in the DCM boost can be summarized in Table 4.1 (a), which shows that \(V_B\) increases with output power \(P_o\) or boost inductance \(L_B\) decreases.

**b) CCM mode operation**

Figure 4.3(c) shows the switching cycle inductor current waveform in the CCM mode operation. To maintain the flux-sec balance in each switching cycle, the bulk-capacitor voltage is given as:

\[
V_B = \frac{V_{in}}{1 - D}
\]  

(4.5)

It shows that in the CCM boost, \(V_B\) is independent of output power \(P_o\) or inductance \(L_B\). The DC/DC duty-cycle \(D\) and input voltage \(V_{in}\) determine \(V_B\).

**4.2.1.2 Boost converter in PFC operations (closed current loop, opened voltage loop)**

If the boost converter is operated as a PFC rectifier, the input voltage is a variable. In each half-line cycle, \(v_{in}=V_{in}\cdot \sin(\omega t)\). The boost inductor current is also a variable. In the DCM boost PFC rectifier, the switch duty-cycle is still a constant value. However, in the CCM boost PFC rectifier, in order to shape the input current, the switch duty-cycle \(d(t)\) has to be a variable.
a) DCM operation

Equation (4.1) and (4.2) can still be used in the DCM boost PFC rectifier, except $V_{in}$ should be replaced by $v_{in}(t) = V_{in} \cdot \sin(\omega t)$ and $i_{LB(ave)}$ should be replaced by $i_{LB(ave)}(t)$. Besides, the discharging time $d_1(t)$ is also a function of time.

The input/output power balance equation is re-written as:

$$P_{in} = \frac{1}{\pi} \int_0^\pi v_{in} \cdot i_{LB(ave)} dt = \frac{P_o}{\eta} \tag{4.6}$$

From Eq. (4.1), (4.2) and (4.6), it can be derived as:

$$\frac{1}{2} \cdot \frac{V_{in}^2 \cdot D^2}{(L_B \cdot f_s) \cdot \pi} \int_0^\pi \left( \frac{\sin^2(\alpha t) \cdot V_B}{V_B - V_{in} \cdot \sin(\alpha t)} \right) dt = \frac{P_o}{\eta} \tag{4.6}$$

Equation (4.6) is complicated and it is hard to get a close form solution of $V_B$. However, Eq. (4.6) can still be used to get the numerical solution of $V_B$. Figure 4.4 is the numerical curve obtained from Eq. (4.6), which shows that $V_B$ increases while output power $P_o$ decreases or boost inductor $L_B$ increases. This result is consistent with the result obtained from the DC/DC operation.

b) CCM operation

For the CCM boost PFC rectifier in Fig. 4.5(a), the continuous PWM switch-cell model can be used as shown in Fig. 2.12(a). Therefore, the following equation is obtained:

$$v_{LB(ave)} = V_{in} \cdot |\sin(\alpha)| \cdot (V_B - d_{PFC} \cdot V_B) \tag{4.7}$$

Consider the DC model of the circuit in Fig. 2.12(a), the inductor should be shorted. It means the DC value of $v_{LB(ave)}$=0. Therefore, $V_B$ is given as:
\[ V_B = \frac{1}{T} \int_0^T V_{in} \cdot | \sin(\omega t) | d\omega t \]

\[ \frac{1}{1 - \frac{1}{T} \int_0^T d_{PFC} (\omega t) d\omega t} = \frac{<V_{in\,(rec)}>}{1 - <d_{PFC}>} \quad (4.8) \]

Where \(<V_{in\,(rec)}>\) represents the DC average value of the rectified input voltage and \(<d_{PFC}>\) represents the DC average value of the PFC duty-cycle in Eq. (2.8). Figure 4.5(b) shows the variable boost duty-cycle \(d_{PFC}\) and its DC value. In the CCM PFC boost rectifier, the bulk-capacitor voltage \(V_B\) is independent of boost inductor \(L_B\) or output power \(P_o\). In the two-stage PFC converter with boost-rectifier front-end, the DC average duty-cycle \(<d_{PFC}>\) is always regulated by the control loop to regulate the bulk-capacitor voltage \(V_B\).

**Table 4.1 Summary of the \(V_B\) in the boost converter (opened voltage loop)**

<table>
<thead>
<tr>
<th>Operation modes of the boost converter</th>
<th>Change of circuit parameters</th>
<th>Change of (V_B)</th>
<th>(V_B) Equations</th>
</tr>
</thead>
<tbody>
<tr>
<td>As DC/DC converter</td>
<td></td>
<td></td>
<td>(V_B = \frac{V_{in}}{1 - \frac{1}{2} \frac{V_{in}^2}{(L_B \cdot f_S)^2} \cdot D^2 \cdot \frac{1}{P_o \cdot \eta}})</td>
</tr>
<tr>
<td>(a) DCM Mode</td>
<td>(P_o \downarrow)</td>
<td>(V_B \uparrow)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>((L_B \cdot f_S) \uparrow)</td>
<td>(V_B \downarrow)</td>
<td></td>
</tr>
<tr>
<td>(b) CCM Mode</td>
<td>(P_o) or (L_B) changes</td>
<td>(V_B) constant</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(V_B = \frac{V_{in}}{1 - D})</td>
</tr>
<tr>
<td>As PFC converter</td>
<td></td>
<td></td>
<td>Close form equation not available</td>
</tr>
<tr>
<td>(c) DCM PFC</td>
<td>(P_o \downarrow)</td>
<td>(V_B \uparrow)</td>
<td>(V_B = \frac{&lt;V_{in,(rec)}&gt;}{1 - &lt;d_{PFC}&gt;})</td>
</tr>
<tr>
<td></td>
<td>((L_B \cdot f_S) \uparrow)</td>
<td>(V_B \downarrow)</td>
<td></td>
</tr>
<tr>
<td>(d) CCM PFC</td>
<td>(P_o) or (L_B) changes</td>
<td>(V_B) constant</td>
<td></td>
</tr>
</tbody>
</table>

In summary, in the boost rectifier with open loop and constant duty-cycle, the operation mode of the boost inductor \(L_B\) determines the relationship between the bulk-capacitor voltage \(V_B\) and the circuit parameters. If \(L_B\) is operated in CCM mode, \(V_B\) is independent of the output power and boost inductance; whereas if \(L_B\) is operated in DCM mode, \(V_B\) will increase with lower output power or higher boost inductance. However, in practice, with closed voltage-loop and controlled duty-cycle, \(V_B\) of the boost PFC rectifier is regulated to be a constant value.
Figure 4.4 Calculated capacitor $V_B$ of the DCM boost PFC rectifier

Figure 4.5 CCM boost PFC rectifier and its capacitor voltage $V_B$ expression

(a) CCM boost PFC rectifier with DC/DC output stage
(b) Line cycle duty-cycle and $V_B$ expression
4.2.2 Effective duty-cycle and bulk-capacitor voltage in the CCM $S^2$PFC converter

As shown in Fig. 4.6, no matter the boost inductor $L_B$ is in DCM or CCM, the front-end of the integrated $S^2$PFC converter is an integrated boost converter. Different from the two-stage PFC converter, this integrated boost rectifier is operated without any voltage feedback control loop. Therefore, the bulk-capacitor voltage $V_B$ in this integrated boost stage should present similar trend as $V_B$ does in the conventional boost rectifier with opened voltage-loop.

4.2.2.1 The bulk-capacitor voltage in the DCM $S^2$PFC converter [B15, C5]

Generally, without the feed-forward component $P_1$ and $P_2$, the converter in Fig. 4.6 is designed as the DCM $S^2$PFC converter. The duty-cycle $D$ is also the DC/DC converter duty-cycle $d_{DC}$, there is an equation to determine the relationship between $d_{DC}(=D)$ and $V_B$:

For CCM forward DC/DC stage:

$$V_o = \frac{V_B \cdot d_{DC}}{n}$$  (4.8)

$$P_o = \left(\frac{V_B \cdot d_{DC}}{n}\right)^2 / R_{\text{Load}}$$  (4.8-a)

Or, for CCM flyback DC/DC stage:

$$V_o = \frac{V_B \cdot d_{DC}}{n \cdot (1 - d_{DC})}$$  (4.9)

$$P_o = \left(\frac{V_B \cdot d_{DC}}{n \cdot (1 - d_{DC})}\right)^2 / R_{\text{Load}}$$  (4.9-a)

where $n$ is the transformer turns-ratio and $n= N_p/N_s$. Combining Eq. (4.6) and (4.8) / (4.9), the bulk-capacitor in the DCM $S^2$PFC converter can be calculated. The capacitor voltage $V_B$ is depended on the load resistance $R_{\text{Load}}$ and the output power. Similar to the DCM boost converter in Section 4.2.1, it can be concluded that $V_B$ increases with output power $P_o$ decreases, and a larger $L_B$ reduces $V_B$. 

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In the DCM S²PFC converter, when the output DC/DC stage is operated in DCM output inductor current mode, the output power of the DC/DC stage can be calculated by following equations:

For DCM forward stage: \[ P_o = V_o \cdot i_{LF(ave)} = \frac{1}{2} \left( \frac{(V_B / n - V_o) \cdot (V_B / n)}{L_F \cdot f_S} \right) \cdot d_{DC}^2 \] (4.10)

Or, for DCM flyback stage: \[ P_o = \frac{1}{2} \cdot \frac{(V_B / n)^2}{L_F \cdot f_S} \cdot d_{DC}^2 \] (4.11)

Where \( L_F \) is the output filter inductance of the DC/DC stage. Equation (4.10) and (4.11) shows that the output power is controlled by \( d_{DC} \) and \( R_{Load} \) is not shown in these two equations. Substitute Eq. (4.10) or (4.11) into Eq. (4.6), if the DC/DC stage enters DCM mode, it turns out that the DCM S²PFC \( V_B \) is independent of the load resistance \( R_{Load} \) and the output power \( P_o \). Besides, the maximum \( V_B \) stress is proportional to the ratio of \( L_F / L_B \). The analysis and calculation data in [B15][C5] also prove this conclusion.

Table 4.2 summarizes the capacitor voltage \( V_B \) in the DCM S²PFC converters.

<table>
<thead>
<tr>
<th>PFC boost stage</th>
<th>DC/DC stage</th>
<th>Change of Circuit parameters</th>
<th>Change of ( V_B )</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCM mode</td>
<td>CCM mode</td>
<td>( P_o \downarrow )</td>
<td>( V_B \uparrow )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( (L_B \cdot f_S) \uparrow )</td>
<td>( V_B \downarrow )</td>
</tr>
<tr>
<td>DCM mode</td>
<td>( (L_F / L_B) \uparrow )</td>
<td>( V_B(\text{max}) \uparrow )</td>
<td>( P_o ) changes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{Independent of} \ P_o )</td>
<td></td>
</tr>
</tbody>
</table>

### 4.2.2.2 Analysis of the bulk-capacitor voltage in the CCM S²PFC converter

a) **Switch duty-cycle \( d_{DC} \) and effective boost PFC duty-cycle \( d_{eff} \)**

By adding the feed-forward component \( L_i \) or \( C_i \) in the boost charging or discharging paths in Fig.4.6, the CCM S²PFC converters have been developed. Based on the similarity of the CCM boost rectifier in Section 4.2.1, the bulk-capacitor voltage \( V_B \) of CCM S²PFC should be given as:
If the DC/DC stage is in CCM mode, from Eq. (4.12), since $d_{DC}$ is only determined by Eq. (4.8) or (4.9), $V_B$ should be independent of output power and boost stage component parameters.

However, the above conclusion does not agree with the experimental results. Figure 4.7 shows the measured bulk-capacitor $V_B$ vs. the output power $P_o$ of the CS $S^2$PFC converter. As shown in Fig. 4.7, the capacitor voltage $V_B$ has strong relationship with the output power.

Furthermore, the above conclusion does not explain why adding inductor $L_1$ or capacitor $C_r$ in the CCM $S^2$PFC can significantly reduce $V_B$, as shown in Fig. 4.2.

As discussed in Section 2.3.4, the feed-forward component $L_1$ or $C_r$ introduced the effective duty-cycle $d_{eff}$ on the boost inductor to shape the input current. It means $L_1$ or $C_r$ changes the switching cycle voltage waveform on the boost inductor $L_B$, as well as the boost converter output voltage $V_B$. In this case, the boost output voltage should be calculated by the effective duty-cycle $d_{eff}$, in stead of the switch duty-cycle $d_{DC}$. Equation (4.12) should be re-written into:

$$ V_B = \frac{< V_{in\,(rec)} >}{1 - < d_{DC} >} \tag{4.13} $$

In Eq.(4.13), the effective duty-cycle $d_{eff}$ changes with output power and boost stage parameters. To further explain the concept, the effective duty-cycle $d_{eff}$ and capacitor voltage $V_B$ of the CCM CS and VS $S^2$PFC will be discussed to show how $V_B$ changes with the output power and circuit parameters.
Figure 4.6 The S\textsuperscript{2}PFC converter and its integrated boost PFC stage

Figure 4.7 CCM S\textsuperscript{2}PFC capacitor voltage $V_B$ increases with output power $P_o$ decreases
($P_1 = L_1$ with diode, no $P_2$ – CS S\textsuperscript{2}PFC converter)
b) $d_{\text{eff}}$ and $V_B$ in the CCM CS $S^2$PFC converter

Figure 4.8 shows that the CS inductor $L_1$ changes the boost-inductor voltage waveform $v_{LB}$ in each switching cycle, in the CS $S^2$PFC converter. By adding inductor $L_1$, the analysis in Section 2.3.2 and 2.3.4 shows the effective duty-cycle $d_{\text{eff}}$ can be calculated as:

$$d_{\text{eff}} = \frac{d_{\text{DC}}}{1 - \frac{d_{\text{eff}}}{d_{\text{DC}}}} = \frac{(L_1 f_S) \cdot i_{LB}}{V_{B}}$$

(4.14)

From Eq. 4.13 and 4.14, the bulk-capacitor voltage in the CCM CS $S^2$PFC converter is given by:

$$V_{B,\text{CS}} = \frac{<V_{\text{in} \cdot \text{rec}}\rangle}{1 - <d_{\text{eff}}\rangle} = \frac{<V_{\text{in} \cdot \text{rec}}\rangle}{1 - d_{\text{DC}} - \frac{(L_1 f_S) \cdot i_{LB}}{V_{B}}}$$

(4.15)

To verify the above equations, a MathCAD® program has been developed. Figure 4.9(a) shows the calculated input current waveform $i_{LB}$ and Fig. 4.9(b) shows the effective duty-cycle $d_{\text{eff}}$. Figure 4.9(c) proves that the bulk-capacitor voltage $V_B$ can be calculated by Eq.(4.15). Also, it is verified that Eq. (4.13) is valid for CCM CS $S^2$PFC converter.

Several conclusions can be drawn from Eq. (4.15):

1) Adding modulation inductor $L_1$ will reduce the boost duty-cycle from $d_{\text{DC}}$ to $d_{\text{eff}}$. As a result, the bulk-capacitor $V_B$ is significantly reduced. (As shown in Fig. 4.2).

2) The modulation effect of the inductor $L_1$ is proportional to the switching frequency $f_S$.

3) To limit bulk-capacitor voltage stress, large $L_1$ is desirable.
Figure 4.8 Effective duty-cycle and capacitor voltage $V_B$ expression in the CS $S^2$PFC circuit

(a) Circuit diagram, (b) circuit waveforms W/O $L_1$, and (c) circuit waveforms with $L_1$
Figure 4.9 Calculated effective duty-cycle and bulk-capacitor voltage of the CS $S^2$PFC converter (at 100 V$_{RMS}$, full load).
c) $d_{\text{eff}}$ and $V_B$ in the VS $S^2$PFC converter

Similar to the CS $S^2$PFC converter, adding a modulation capacitor $C_r$ will changes the effective boost duty-cycle on the input inductor $L_B$. As a result, the bulk-capacitor voltage $V_B$ is also changed. Figure 4.10 shows the waveforms of the VS $S^2$PFC converter to define its effective boost duty-cycle. Based on the analysis in Section 2.3.3 and 2.3.4, the effective duty-cycle in VS $S^2$PFC converter can be calculated as:

$$d_{\text{eff}} = \frac{(C_r \cdot f_s)}{i_{LB}} \cdot \frac{V_B}{2 \cdot (1 - D)^2}$$

(4.16)

The assumptions of Eq. (4.16) are that the charging time of $C_r$ is shorter than $(d_{DC} \cdot T_S)$, and, the output stage is the flyback DC/DC converter.

The bulk-capacitor voltage in the CCM VS $S^2$PFC has equation as:

$$V_{B_{\text{VS}}} = \frac{< V_{\text{in (rec)}} >}{1 - < d_{\text{eff}} >} = \frac{< V_{\text{in (rec)}} >}{1 - \frac{(C_r \cdot f_s)}{i_{LB}} \cdot \frac{V_B}{2 \cdot (1 - D)^2}}$$

(4.17)

Similarly, Several conclusions can be drawn from Eq. (4.17) for the VS $S^2$PFC:

1) Adding modulation capacitor $C_r$ will reduce the boost duty-cycle from $d_{DC}$ to $d_{\text{eff}}$.

As a result, the bulk-capacitor $V_B$ is significant reduced. (As shown in Fig. 4.2).

2) The modulation effect of the capacitor $C_r$ is proportional to the switching frequency $f_S$.

3) To limit bulk-capacitor voltage stress, small $C_r$ is desirable.
Figure 4.10 Effective duty-cycle and capacitor voltage $V_B$ expression in the VS S$^2$PFC circuit
(a) Circuit diagram, (b) circuit waveforms W/O $C_r$, and (c) circuit waveforms with $C_r$
d) Summary of the relationship between bulk-capacitor voltage $V_B$ and the feed-forward component parameters in the CCM $S^2$PFC converters

Combining the results of the bulk-capacitor voltage $V_B$ in the CS and VS $S^2$PFC, $V_B$’s relationship with the feed-forward component can be qualitatively summarized as shown in Fig. 4.11. In the CCM $S^2$PFC converters, the feed-forward components provide the effective duty-cycle on the boost inductor. As shown in Eq. (4.14) and (4.16), the duty-cycle modulation (reduction) effects are proportional to the products of $(L_1 \cdot f_S)$ or $1/(C_r \cdot f_S)$, which can be summarized as the boost charging path impedances $Z_B$:

$$Z_{B_{ \, \, CS}} = L_1 \cdot f_S \quad \text{or} \quad Z_{B_{ \, \, VS}} = \frac{1}{C_r \cdot f_S} \quad (4.18)$$

In order to reduce the bulk-capacitor voltage stress, it is helpful to increase the boost impedance $Z_B$ to alleviate the boost function. Figure 4.12 experimentally verified that large boost impedance reduces the effective duty-cycle and bulk-capacitor voltage stress.

Furthermore, Fig. 4.13 shows a more general $S^2$PFC circuit model with the charging path and discharging path feed-forward components. Following the previous thinking process, the charging and discharging components are represented by two boost impedance $Z_{B1}$ and $Z_{B2}$. Adding the impedance $Z_{B2}$ should be able to further reduce the bulk-capacitor voltage. Although Fig. 4.11 and 4.13 only shows the structure of the three-terminal feed-forward cells, due to the equivalent relationship between the 2-terminal and 3-terminal cells, all the conclusions also apply to the 2-terminal $S^2$PFC converters.
Figure 4.11 Summary of the qualitative relationship between CCM $S^2$PFC capacitor voltage $V_B$ and the $S^2$PFC feed-forward component with $Z_B$.

\[ V_B = \frac{V_{in(AVE)}}{1 - \langle d_{eff} \rangle} \]

$Z_B$ defined as $L_1 \cdot f_s$ or $1/(C_r \cdot f_s)$

Figure 4.12 Measured bulk-capacitor voltage $V_B$ decreases with boost impedance $Z_B$ increases:
(a) CS $S^2$PFC converter, (b) VS $S^2$PFC converter

\[ d_{eff} = d_{DC} - \frac{L_1 \cdot f_s \cdot i_{LB}}{V_B} \]
\[ d_{eff} = \frac{C_r \cdot f_s \cdot i_{LB}}{k} \]
Figure 4.13 Further reduce effective duty-cycle and bulk-capacitor voltage $V_B$ by adding $Z_{B2}$
e) Bulk-capacitor voltage vs. output power in the CCM S\textsuperscript{2}PFC converters

Equation (4.14) and (4.16) also explain why the bulk-capacitor voltage $V_B$ increases with the decreases of the output power, while the DC/DC stage is in CCM mode. When the output power decreases, the input current $i_{LB}$ will eventually decrease to maintain the input/output power balance in the converter. As a result, the effective duty-cycle $d_{eff}$ in the CS or VS S\textsuperscript{2}PFC increases. According to Eq. (4.15) and (4.16), the bulk-capacitor voltage $V_B$ will increase. This explains the experimental results shown in Fig. 4.14(a) and (b) for the CS and VS S\textsuperscript{2}PFC converters.

It is necessary to point out that the DC/DC stage inductor $L_F$ and the boost inductor $L_B$ of the CCM S\textsuperscript{2}PFC converters will eventually enter the DCM mode, when the output power further decreases. For this case, the in-depth study and analysis has not been done in this dissertation. If DC/DC stage inductor $L_F$ enter DCM mode, it is predicted that the capacitor voltage $V_B$ is independent to output power, but proportional to $L_B/L_F$ ratio. Besides, it is believed and verified later that the modulation inductor $L_1$ or $C_1$ has same effect as they do when DC/DC stage is in the DCM mode. Table 4.4. Summarizes the capacitor $V_B$’s features in the CCM S\textsuperscript{2}PFC converter. Nonetheless, further study on the capacitor voltage $V_B$ in the full power range is very necessary to be done in the future.
Figure 4.14 Measured bulk-capacitor voltage $V_B$ increases while output power $P_o$ decreases

(a) CS $S^2$PFC converter, (b) VS $S^2$PFC converter

Table 4.4 Summary of the capacitor voltage $V_B$ in the CCM $S^2$PFC converter

<table>
<thead>
<tr>
<th>PFC stage</th>
<th>DC/DC stage</th>
<th>Change of Circuit parameters</th>
<th>Change of $V_B$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCM $S^2$PFC Front-end</td>
<td>CCM mode</td>
<td>$P_o \downarrow$</td>
<td>$V_B \uparrow$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(L_1 f_S) \uparrow$ or $(C_r f_S) \downarrow$</td>
<td>$V_B \downarrow$</td>
</tr>
<tr>
<td></td>
<td>DCM mode</td>
<td>$P_o \downarrow$</td>
<td>$V_B$ does not change (?)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(L_1 f_S) \uparrow$ or $(C_r f_S) \downarrow$</td>
<td>$V_B \downarrow$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$L_B/L_F \uparrow$</td>
<td>$V_B$ (?)</td>
</tr>
</tbody>
</table>
4.2.3 Bulk-capacitor voltage feedback windings in the CCM S^2PFC converters

The concept of the bulk-capacitor voltage feedback windings was first introduced by [B10] in the DCM S^2PFC converters. However, it can be also applied to the CCM S^2PFC circuits to further reduce the bulk-capacitor voltage \( V_B \) stress [B6, B9].

Figure 4.15 shows the generalized CCM three-terminal S^2PFC topology with feedback winding \( N_1 \) on the charging path and \( N_2 \) on the discharging path. Every time when the switch \( S \) is turned on, the voltage on winding \( N_1 \) is \( v_{N1} = (N_1/N_p) \cdot V_B \) and \( v_{N1} \) is in the opposite direction of input voltage \( v_{in(\text{rec})} \); when the switch is off, the voltage on winding \( N_2 \) is \( v_{N1} = (N_1/N_p) \cdot V_B \) and \( v_{N2} \) is also in the opposite direction of \( v_{in(\text{rec})} \). In this case, Eq. (4.13) should be re-written as:

\[
\frac{(V_{in(\text{ave})} - k_1 \cdot V_B) \cdot <d_{eff}> + (V_{in(\text{ave})} - k_2 \cdot V_B) \cdot (1 - <d_{eff}>)}{1 - <d_{eff}>}
\]

(4.19)

Where, \( k_1 = N_1/N_p \) and \( k_2 = N_2/N_p \). Equation (4.19) can be re-written as:

\[
V_B = \frac{V_{in(\text{ave})}}{1 - [<d_{eff}] - k_1 \cdot <d_{eff}] - k_2 \cdot (1 - <d_{eff}>)} = \frac{V_{in(\text{ave})}}{1 - <d_{eff}>}
\]

(4.20)

As shown in Eq. (4.19), the feedback windings reduce the average effective duty-cycle from \( d_{eff} \) to \( \tilde{d}_{eff} \). Therefore, the bulk-capacitor voltage is further reduced. Again, the penalty of feedback winding is the dead conduction angle on the input current introduced by \( N_1 \).

It is necessary to point out that Eq. (4.19) and (4.20) just roughly evaluate the effect of the feedback windings. Since the \( N_1 \) also introduces dead conduction angle on the input current, the average of the effective duty-cycle \( <d_{eff}> \) will be different. Therefore, Eq. (4.19) and (4.20) are not mathematically accurate. Even though, these two equations show the fact that feedback windings can also reduce \( V_B \) in the CCM S^2PFC converters. Figure 4.16 shows the experimental verification of the above conclusion.
Figure 4.15 Generalized CCM S²PFC with feedback windings N₁ and N₂

Figure 4.16 Experimental results show that the feedback winding further reduces bulk-capacitor voltage stress in the CCM CS S²PFC converter
4.2.4 Further discussions and conclusions

In above sections, the boost effective duty-cycle and boost impedance concept has been proposed to provide a simple model to explain and study the bulk-capacitor voltage in the CCM S²PFC converters. It shows that the feed-forward S²PFC components L_i or C_i can reduce the effective duty-cycle and limit the bulk-capacitor voltage. Larger boost impedance will provide a lower capacitor voltage. This gives the directions in the converter design. To further reduce the bulk-capacitor voltage stress, feedback windings are also effective. Of course, a good design need not only reduce voltage stress, but also meet input current harmonics limits and provide good efficiency.

It is necessary to point out that the effective duty-cycle concept is a relative simple concept, which is only good while the boost inductor is in CCM operation mode. As a matter of fact, generally, the boost inductor current $i_{L_B}$ of a CCM S²PFC converter always has DCM and CCM time intervals during one line cycle, which makes the problem more complicated. Therefore, to accurately calculate the bulk-capacitor voltage $V_B$, the numerical analysis approach or circuit simulation has to be used. Even though, since most of the power is transferred during the CCM interval, the effective duty-cycle is still a good concept to design guideline qualitatively.

However, when the output power $P_o$ is very low, the boost inductor will eventually be operated only in the DCM mode. In this case, the effective duty-cycle concept is no longer valid. That is why this concept can not explain why the bulk-capacitor voltage $V_B$ stops increasing when the output power drop to certain value, as shown in Fig. 4.16. To solve this problem, further in-depth study is still needed. This is one of the future works of this dissertation research.
4.3 STUDY ON THE CONVERTER EFFICIENCY AND SWITCH CURRENT STRESS

4.3.1 Discussion on the power losses in the CCM S\textsuperscript{2}PFC converters

To reduce the thermal component size and the total cost of a power supply, it is always necessary to design the S\textsuperscript{2}PFC converter with reasonable good efficiency. In the S\textsuperscript{2}PFC converter, the major power losses are consumed by the semiconductor devices, including the high-voltage side switch(es) and diode(s), and the low-voltage side output rectifiers. Among them, the high-voltage side device losses can be reduced with a careful design of the S\textsuperscript{2}PFC cell.

The power losses on the main switch(es) contain two different losses: the switching loss and the conduction loss. In a CCM S\textsuperscript{2}PFC converter, the switching loss is caused by the boost diode reverse-recovery, the leakage current of the power transformer and the voltage/current overlapping of the power switch turn-on and turn-off. In the CCM CS S\textsuperscript{2}PFC converter, the CS inductor L\textsubscript{1} can limit the di/dt of the boost diode current when the switch is turned on. Therefore, the diode-reverse-recovery-related loss is alleviated. On the other side, in the CCM VS S\textsuperscript{2}PFC converter, the VS capacitor C\textsubscript{r} can absorb the transformer leakage current so that the switch turn-off loss can be reduced. In most cases, when the input line voltage is low, the diode reverse-recovery loss is larger than the transformer-leakage loss. It means the CS S\textsuperscript{2}PFC converter may has lower switching loss than the VS S\textsuperscript{2}PFC converter. In general, the switching loss can be reduced if the bulk-capacitor voltage is reduced. In conclusion, a large impedance Z\textsubscript{B1} in the boost charging path can reduce the bulk-capacitor voltage and the switching loss on the power switch.
In fact, in the $S^2$PFC converters, it is more important to reduce the conduction loss, especially at low input line condition when the input current is high. As shown in Fig. 4.17, in the $S^2$PFC converter, since the PFC and DC/DC stages are integrated into one stage, the integrated switch S has to handle both the boost PFC current $i_{PFC}$ and the DC/DC converter current $i_{DC/DC}$, i.e., $i_S = i_{PFC} + i_{DC/DC}$. And the input power still needs to be transferred through two conversion stages to the output. Therefore, total conduction loss of the $S^2$PFC converter is not lower than the conduction loss in the two-stage PFC converter. On the contrary, if the MOSFET switch is used as the power switch S in Fig. 4.17, the switch conduction loss is proportional to its RMS current. The conduction loss of the main switch can be calculated by:

$$P_{S\_con\_S^2PFC} = R_{ds\_DC/DC} \cdot \left[ i_{PFC} + i_{DC/DC} \right]_{RMS} \tag{4.21}$$

The conduction loss on the $S^2$PFC switch is actually higher than the total switch conduction losses in the two-stage PFC converter. To improve the $S^2$PFC efficiency, it is critical to reduce its switch current stress and related conduction loss.

![Integrated boost PFC stage](image)

Figure 4.17 $S^2$PFC switch current $i_S$ contains DC/DC current $i_{DC/DC}$ and PFC current $i_{PFC}$
4.3.2 Reduce the switch current stress by using large boost impedance $Z_B$

Since the DC/DC stage current $i_{DC/DC}$ is determined by the output power, to reduce the $S^2$PFC switch current stress, it is necessary to reduce the PFC charging path current $i_{PFC}$, which is also represented as $i_{ZB1}$ in Fig. 4.17. Conceptually, when the input voltage and output power is fixed, the boost inductor current $i_{LB}$ is fixed. However, the boost charging-path only conducts current during the time interval, which is proportional to the effective boost duty-cycle $d_{eff}$. It means a lower $d_{eff}$ will can reduce the RMS current of $i_{ZB1}$, as well as the RMS current stress on the switch.

Figure 4.18 conceptually shows that using large impedance in the CCM $S^2$PFC cell can reduce the effective boost duty-cycle and the switch current stress. This conclusion is verified by the switching cycle waveform of the CS and VS $S^2$PFC converters. As shown in Fig. 4.19, in the CS $S^2$PFC converter, a large CS inductor $L_1$ (large $Z_B$) increases the inductor $L_1$ charging time $\Delta t$ after switch S is turned on. Therefore, the current $i_{L1}$ has less area, as shown in Fig. 4.19(b) and the switch RMS current is reduced consequently. Similarly, Fig. 4.20 shows that in VS $S^2$PFC converter, a smaller $C_r$ (large $Z_B$) reduces the capacitor $C_r$ charging time $\Delta t$ after switch S is turned on. As a result, the current $i_{Cr}$ has less area, as shown in Fig. 4.20(b). The switch RMS current is also reduced. In conclusion, increasing the impedance $Z_B$ (which is defined as $L_1 \cdot fs$ or $1/(C_r \cdot fs)$ can effectively reduce the switch RMS current and the related conduction loss.
Figure 4.18 Reduce switch current stress with large boost impedance $Z_B$

CS $S^2$PFC, $Z_B = L_1 \cdot f_s$

Figure 4.19 Large CS inductor $L_1$ reduces the current $i_{L1}$ and the switch RMS current
Figure 4.20 Small VS capacitor \( C_r \) reduces the current \( i_{Cr} \) and the switch RMS current

Figure 4.21 Measured CCM \( S^2\)PFC full-load efficiency with different \( L_1 \) or \( C_r \)
As shown in Fig. 4.21, the measured CCM S²PFC converters full-load efficiency further verified that large boost impedance $Z_B$, which means large $L_1$ in the CS S²PFC or small $C_r$ in the VS S²PFC converter, increases the converter efficiency.

### 4.3.3 Reduce switch current stress by using bulk-capacitor voltage feedback windings

As discussed in Section 4.2.3, the bulk-capacitor voltage feedback windings can further reduce the effective duty-cycle $d_{eff}$. Therefore, adding the feedback windings in the CCM S²PFC cells also reduces the RMS value of the switch current as well as its conduction loss. This conclusion is conceptually shown in Fig. 4.22 of the switching waveforms of the CS S²PFC converter with and without the feedback winding $N_1$, respectively. As shown in Fig. 4.22(c), during the $\Delta t$ time interval, adding the winding $N_1$ will reduce the voltage applied on $L_1$ from $V_B$ to $V_B(1-N_1/N_P)$. As a result, the charging rate and the area of $i_{L1}$ are decreased. Besides, during the switch turn-on time interval, the total switch current can be calculated as:

$$i_s = I_{out} + i_{L1} - i_{L1} \cdot \frac{N_1}{N_P}$$  \hspace{1cm} (4.19)

$I_{out}$ is the averaged current to the output side, which is constant with fixed DC/DC output power. Therefore, $N_1$ reduces the switch current, which is also shown in Fig. 4.22(b) and (c).

The simulated circuit waveforms in Fig. 4.23 verifies that the feedback winding $N_1$ changes the switch current $i_s$ and the transformer winding $N_P$ current $i_{DC/DC}$, during the time interval $\Delta t$ while winding $N_1$ is conducting current.

It is necessary to point out that the winding $N_1$ not only reduces the current $i_{L1}$, but also provides the “direct-energy-transfer” from the input to the output rectifier on the low voltage side. Since the total output power is fixed, the power go through the DC/DC stage is reduced, as
Figure 4.22. Reduce the switch RMS current by adding feedback-winding $N_1$ in the boost charging path (CS S$^3$PFC with forward DC/DC stage)
Figure 4.23 Simulated waveforms show that feedback-winding N1 reduce switch current $i_S$
($V_{in}=180V_{RMS}$, output 5V/40A, output stage is forward DC/DC converter)

$23\% P_{in}$ is $P_{direct}$
($N_1/N_p=0.45$)

$32\% P_{in}$ has to go through two stages to keep constant $P_{output}$

Totally $77\%$ input power goes through two stages

$45\%$

Total input power = 100%

Figure 4.24 Simulated power distribution of the CS $S^2$PFC converter with $N_1$
($N_1/N_p=0.45$, $V_{in}=180V_{RMS}$, full load)
well as the DC/DC current \( i_{\text{DC/DC}} \). Therefore, the total loss is further reduced. Figure 4.24 shows the amount of the simulated “direct-transferred-power” \( P_{\text{direct}} \) from the input side to the transformer output-side through the feedback winding \( N_1 \). In general, as proposed in [B19], to have the unit input power factor and keep constant DC output power, theoretically, 32% of the input power has to go through “two stages”, while 68% of the input power can be directly transferred to output. In the \( S^2\)PFC converter without the feedback windings, 100% of the input power will be converted twice to reach output. However, if the feedback winding \( N_1 \) is add to the CS \( S^2\)PFC, the simulation data show that 23% of input power can be “directly transferred” with only one conversion step, at 180V\(_{ac}\) input and \( N_1/N_p=0.45 \). In fact, \( P_{\text{direct}} \) can be represented by:

\[
P_{\text{direct}} = \frac{1}{T_{\text{line}}} \int_{0}^{T_{\text{line}}} i_{L1} \cdot V_B \cdot \frac{N_1}{N_p} \, dt
\]  

(4.20)

In conclusion, adding the feedback winding \( N_1 \) is more effective to reduce the switch current stress than increasing the boost impedance \( Z_B \). Again, the penalty of adding \( N_1 \) is the dead conduction angle and related input current distortion on the input current. A good design should maximum \( N_1 \) and the input current still meet harmonics limits. In section 4.4, a detailed study and design will be given on the CS \( S^2\)PFC converter as an example.
4.4 DESIGN CONSIDERATIONS OF THE CCM CS S\textsuperscript{2}PFC CONVERTER

4.4.1 Introduction

4.4.1.1) General design considerations

Generally, the design optimization of a S\textsuperscript{2}PFC circuit needs to meet several objectives:

(1) **Input current harmonics** have to meet the input current harmonic limits, such as the IEC1000-3-2 Class D specifications.

(2) **Bulk-capacitor voltage stress** has to provide sufficient margins for 450 V capacitor.

(3) **Good efficiency** with minimized component ratings and low cost.

For the CS S\textsuperscript{2}PFC converter shown in Fig. 4.22(a), generally, boost inductor $L_B$, CS inductor $L_1$, and turns ratio $N_1/N_p$ are the three key design parameters. The design considerations of these parameters will be discussed in this section.

4.4.1.2) Previous work in the literature

It is necessary to point out that there are several design approaches proposed in the literature for the CCM CS S\textsuperscript{2}PFC converter. Especially, [C6] and [C7] are about the design of this particular converter.

[C7] provides a design approach which uses the concept of lossless resistor to design the CS S\textsuperscript{2}PFC converter. The boost inductor current conduction angle $\phi_c$ is used to indicate the input current distortion. The maximum $L_1$ is chosen at the point that the minimum bulk-capacitor voltage $V_B(\text{min})$ is equal to the minimum peak input voltage $V_{\text{in,peak}(\text{min})}$. This design approach is simple but not precise. Furthermore, it does not clearly describe the design trade-off between the input current distortion, bulk-capacitor voltage and efficiency.
[C6] is a well-written paper, which provides the detailed mathematical equations and numerical approach for the design of the CS $S^2$PFC converter with feedback windings for universal-line input. This approach uses a numerical program to calculate and check the averaged boost inductor current waveform. And, choose the parameters $L_B$, $L_1$, and $N_1/N_p$ according to the minimum and maximum bulk-capacitor voltage $V_B$. The principle of input-output power balance is used to calculate $V_B$.

However, this paper has following aspects need to be improved:

a) To clearly define and separate the physical functionality of inductors $L_1$ and $L_B$,

b) To clearly explain the trade-off on the input current harmonics, bulk-capacitor voltage and converter efficiency with different parameters, especially $L_1$ and $N_1$,

c) To provide straightforward design curves which shows how to optimize the key components.

4.4.1.3) Design assumptions and conditions

To articulate the effects of different circuit parameters, this section focuses on the CS $S^2$PFC converter and provides a straightforward design approach to explain the design trade-off on the input current ripple, the switch current stress, the energy-storage bulk-capacitor voltage stress, and overall efficiency. Simulation and experimental data are also provided to support the analysis and design.

Several assumptions or conditions are made to simplify the design process. First, the universal-line input voltage is generally required. However, as shown in Chapter 5, the $S^2$PFC converters have the general problems with universal-line input and the corresponding solution is given in Chapter 6. In this case, in this section, the design process of the CS $S^2$PFC converter is
focus on the narrow line-range input, i.e. 180-265 V_ac input. And the design results can apply to
the improved CS S^2PFC converter with universal line input in Chapter 6. Second, the IEC61000-
3-2 current harmonics specification is chosen. Third, the design of the front-end input-current-
shaping stage should be independent with the output stage, while the output stage use the
conventional PWM DC/DC power stage and control design.

As an example, the simulation/experimental circuit is designed to have a line input (180-
265Vac) and 5V/40A output with forward DC/DC stage. The key experimental circuit
components have been chosen as follows: L_B: 45 - 190 µH, L_1: 30 - 100 µH, N_1 / N_p = 0.45,
C_{B1,2}: 470 uF/250V, switch S: IXYS 12N100 and Schottky diode on the output side D_{S1-2}:
IR81CND45, switching frequency f_s=70kHz.

4.4.2 Design considerations of the key parameters of the CS S^2PFC converter

4.4.2.1) Feedback windings ratio N_1/N_p

As discussed in Section 4.3, both a large inductor L_1 or feedback winding ratio N_1/N_p
can reduce the bulk-capacitor voltage stress and switch current stress. In addition, the feedback
winding N_1 provides additional benefit to “direct-transfer” the energy from transformer input to
output. Therefore, to achieve the maximum N_1/N_p is the first design step. As discussed in
previous sections, the trade-off of choosing N_1/N_p is between the dead-conduction-angle related
input current distortion and the low voltage/current stress. Simulation and experiments have been
done to verify above conclusions. For example, as shown in Fig. 4.25(a), the feedback winding
N_1 introduces the input current dead conduction angle, which causes the high input current
harmonics, as shown in Fig. 4.25(b). However, with high feedback winding N_1/N_p ratio, the CS
Figure 4.25 Input current distortion with different N\textsubscript{1}/N\textsubscript{p}:

(a) input current waveforms, (b) measured input current harmonics comparison.
Figure 4.26 Measured full load efficiency of the CS S$^2$PFC converter with different $N_1$

($V_{in}$=180 – 265 V$_{RMS}$, output-5V/90A, $f_s$=70kHz)
S$^2$PFC converter has high conversion efficiency, as shown in Fig. 4.26.

Considering the input current harmonics, bulk-capacitor voltage stress and converter efficiency, based on the experiences from simulations and experiments, the maximum $N_1/N_p$ in the CS S$^2$PFC converter should be chosen as:

\[
\frac{N_1}{N_p} \max = 0.4 - 0.5
\]  

(4.21)

After the $N_1/N_p$ ratio is defined, the rest design parameters are the boost inductor $L_B$ and CS inductor $L_1$.

**4.4.2.2) Current Source inductor $L_1$**

Conceptually, after the feedback-winding ratio $N_1/N_p$ is chosen, the CS modulation inductor $L_1$ is the key component to be designed. According to previous discussions, the choice of inductor $L_1$ is also determined by considering the trade-off between the maximum bulk-capacitor voltage and current distortions.

As shown in Eq. (4.13) and (4.14), a larger $L_1$ reduces the effective duty-cycle of boost inductor $L_B$, therefore decreasing both the bulk-capacitor voltage stress and the switch current stress, which is proved experimentally in Fig. 4.27. In addition, a larger $L_1$ introduces a stronger modulation to the boost inductor current and reduces line-current distortions. However, if too large of $L_1$ is selected, the bulk-capacitor voltage $V_B$ can become lower than the peak input voltage. Since this violates the boost operation condition, the line-current distortion increases because of the peak charging of the bulk cap around the line-voltage peaks. This conclusion is proved by simulation and experiment. As shown in Fig 4.28, the over-designed $L_1$ reduces $V_B$ too much and hurts the input current waveform.
Figure 4.27 Large $L_1$ reduces $V_B$ and improves converter efficiency
(Experimental result of CS $S^2$PFC with output-5V/40A, $f_s=70$kHz)
Figure 4.28 Over-designed $L_1$ makes $V_B$ to be lower than $v_{in, pk}$, causes current distortion
(Experimental waveform of CS $S^2$PFC)

Figure 4.29 Simulated boost inductor current waveforms with different $L_1$
(Fixed $L_B = 100\ \mu\text{H}$, $N_1/N_p=0.45$, $V_{in}=230\ \text{V}_{\text{RMS}}$, output 5V/40A, $f_s=70\ \text{kHz}$)
Different $L_1$ values have been studied with simulation and experiment for the design optimizations. To study the $L_1$ effect on the input current, $L_B$ was fixed at 100 $\mu$H and several different $L_1$ have been used in the circuit in Fig. 4.22(a). Figure 4.29 shows different input current waveforms in simulations with different $L_1$ inductance at 230 V$_{ac}$, full load. This figure was obtained with a closed voltage-loop simulation with Simplis® software. As shown in Figure 4.29(d), if $L_1$ is over designed, there is high distortion on the input current because $V_B$ is lower than $V_{in(peak)}$. The input current THD is about 85%. After $L_1$ was decreased to 78 $\mu$H, $V_B$ was already higher than $V_{in(peak)}$. Therefore, the input current has much less distortion and input current THD was reduced to 78.1%, as shown in Fig. 4.29(c). After that, if $L_1$ was too small, the converter did not have enough PFC modulation and the distortion increased again. For example, as shown in Fig. 4.29(a), input current has high distortion again and THD = 88%.

Because the IEC61000-3-2 Class D standard sets the limits on the input current harmonics instead of the input current THD, it is necessary to check each order of the input current harmonics with different CS inductance $L_1$. The simulated input current 3$^{rd}$, 5$^{th}$, 7$^{th}$, and 9$^{th}$ harmonics vs. $L_1$ curves are given in Fig. 4.30, while other higher order harmonics are also checked. By comparing the simulated data with the IEC standards on each order of harmonics, the acceptable $L_1$ range can be defined with certain margins on harmonics (e.g.10%). Combining the results in Fig. 4.30, Fig. 4.31 shows the input current THD vs. the CS inductance $L_1$ curve, which is with 200W-output, and switching frequency is 70 kHz. In Fig. 4.30, the shaded area shows the $L_1$'s range with which the input current harmonics can meet the IEC limits with 10% margin. To minimize the bulk-capacitor voltage stress and maximize the converter efficiency, the largest value of $L_1$ should be chosen as the optimized design value. Figure 4.31 also shows the experimental input current THD curve, which is quite close to the simulated curve.
Figure 4.30 Define the range of $L_1$ to meet IEC61000-3-2 class D with 10% margin

(Compared with IEC61000-3-2 class D limits at 230 $V_{\text{RMS}}$ nominal line, full load)
Figure 4.31 Simulated and experimental $L_1$ design curve for the CS $S^2$PFC converter: shaded area shows the acceptable area for the input current harmonics to meet IEC limits with 10% margins. ($V_{in} = 230\ V_{RMS}$, $f_s = 70\ kHz$, $(N_1/N_p)_{max} = 0.45$, $P_o = 200W$)
Although the $L_1$ design curve is for a specified output power and switching frequency, it is necessary to point out that this curve can be normalized to provide more general design guideline for the CS $S^2$PFC converter with different power rating and switching frequency. The effective-duty-cycle equation in Eq. (4.14) gives following relationship among $d_{ef}$, ($L_1 \cdot f_s$), and output power $P_o$:

$$d_{ef} \approx d_{DC} - \left( \frac{L_1 f_s}{V_B} \right) i_{LB} \approx d_{DC} - \left( \frac{L_1 f_s}{V_{in}^2} \right) P_o$$

Therefore, for different power rating and switching frequency, the CS inductance $L_1^*$ can be given by normalized as:

$$L_1^* = L_1 \cdot f_s \cdot P_o$$

And for different output power $P_{o2}$ and switching frequency $f_{s2}$, the desired CS inductor $L_{1(2)}$ can be calculated by:

$$L_{1(2)} = L_1^* / \left( f_{s2} \cdot P_{o2} \right)$$

Then the curve in Fig. 4.31 can be use as a general design curve for $L_1$.

4.4.2.3) Boost inductor $L_B$

After the feedback winding ratio $N_1/N_p$ and the CS inductance $L_1$ are determined, the last design variable is the boost inductance $L_B$. Conceptually, $L_B$ has small effect on the boost effective duty-cycle, as well as the input current distortion and conversion efficiency. Therefore, the design of $L_B$ is not as critical as the previous two parameters. However, since $L_B$ “sees” the effective duty-cycle, the inductance of $L_B$ should determine the magnitude of the switching-frequency input current ripple, which will impact the differential mode EMI filter size.
To show the $L_B$’s effects on the input current and verify the above statements, $L_1$ is fixed as $L_1=68 \ \mu H$ and several different $L_B$ values were used in the 5V/40A-output simulation/experiment circuit. Figure 4.32 shows the different boost inductor current waveforms and their spectrum at switching frequency in simulations. As shown in Fig. 4.32 (a), (c) and (e), when the boost inductance changes, the input current THD just has very small difference from each other. Furthermore, the low-frequency harmonics of the input current with different $L_B$ are very close to each other, as shown in Fig. 4.33. It shows that different $L_B$ values have small impact on the low-frequency input current harmonics. However, as shown in Fig. 4.32(b), (d) and (f), the high-frequency (switching-frequency) ripple on the boost inductor current changes with the inductance $L_B$ changes. Therefore, the choice of $L_B$ is related with the DM-EMI filter design. The design of $L_B$ is similar to the boost inductor in the conventional CCM boost PFC converter.

4.4.2.4) Summary of the design process

In summary, many different issues need to be considered during the design of this converter. The feedback winding ratio $N_1/N_P$, inductor $L_B$ and $L_1$ are important design parameters of the CS $S^2$PFC converter. Generally, as to $N_1$, the feedback ratio should be chosen as high as possible to achieve high efficiency and low $V_B$ stress, until it is hard for the converter to meet IEC61000 Class D harmonics limits. The optimized $N_1/N_P$ is in 0.4–0.5 range. $L_1$ and $L_B$ should be selected by considering Figs. 4.27 - 4.32. The design objective is to get the lowest $V_B$ stress and highest efficiency while the converter can still meet IEC harmonics limits. Within the IEC limits, $L_1$ should be chosen a large value based on Fig. 4.31. To provide a straightforward design approach, Fig. 4.34 summarizes the design steps and provides clear design guidelines of
Figure 4.32 Simulated boost inductor current waveform and its spectrum at switching-frequency with different \( L_B \) (Fixed \( L_1 = 68 \, \mu\text{H}, 5\text{V}/40\text{A}-\text{output}, f_s=70\text{kHz} \))
Harmonics Comparison @ 230Vac

Figure 4.33 Input current has similar harmonics with different $L_B$ (Fixed $L_1$)

Choose feedback winding ratio = 0.4~0.5

Choose $L_1$ from Fig. 4.30
1. Choose $L_1$ in the range to meet IEC.
2. To get good efficiency and low $V_B$ stress, large $L_1$ is preferred.

Choose $L_B$ for acceptable current ripple and EMI. The current ripple can be obtained from simulation.

Simulation and experimental verification, check harmonics, $V_B$ stress and efficiency

Figure 4.34 Design process of the CCM CS $S^2$PFC converter
the CCM CS $S^2$PFC converter with narrow line range. It is necessary to point out that a few straightforward steps are not enough for the design optimization of this converter. Numerical analysis, simulations, and experiments are all necessary to get the optimal design. In addition, the dc/dc output stage design should be quite similar as the conventional dc/dc converter design.

### 4.4.3 Performance of the CS $S^2$PFC converter with universal-line input

Above design is target at the CS S2PFC converter with narrow line-voltage range. Following the similar design principle, another experimental prototype has been developed with universal-line-input, 5V/20A-output. Since the input voltage has a 90-265 VRMS range, it is quite hard to design the converter to have the input current meet both the IEC limits at 230 VRMS and the corresponding Japan limits at 100VRMS. In this case, the feedback winding ratio $N_1/N_p$ should be very small. Actually, in out design, feedback winding $N_1$ is not used to guarantee the input current harmonics can meet the standards.

The key experimental circuit components have been chosen as follows: $L_B$: 500 µH, $L_1$: 300 µH, $N_p = 39$ T, $N_s = 3$ T, $C_{B1,2}$: 220 uF/450V, switch S: IXYS 12N100 and Schottky diode $D_{S1,2}$: IR40CND45, switching frequency $f_s=70$kHz. The active-clamp reset scheme has to be used in the forward DC/DC stage to provide enough duty-cycle so that the converter can be designed to meet IEC Class D specification.

Figure 4.35 shows the experimental circuit diagram. Figure 4.36(a) shows its input current harmonics, which meet IEC Class D standard with small margins. Figure 4.36(b) shows that the maximum bulk-capacitor voltage stress $V_B$ is close to 430 volt, so a 450 V-rated electrolytic capacitor can be used. As shown in Fig. 4.36(c), with the universal-line input, the CS $S^2$PFC converter efficiency is reduced compared to the previous design with narrow-line voltage.
Figure 4.35 Experimental circuit diagram of the CCM CS $S^2$PFC converter

Figure 4.36 Experimental results of the CCM CS $S^2$PFC with universal line input
(a) Input current harmonics, (b) bulk-capacitor voltage stress, and (c) measured full load efficiency
input in Fig. 4.27. Even though, the universal-line CS $S^2$PFC converter has 3-4% higher efficiency than the DCM $S^2$PFC converter [B15] with high feedback winding ratio ($N_1/N_p=0.7$).

In conclusion, the CCM $S^2$PFC converter has better performance than the DCM $S^2$PFC converters with universal line input voltage.
4.5 SIMULATION STUDY OF THE CCM VS S²PFC CONVERTER

4.5.1 Introduction

Following the similar methodology in the study of the CCM CS-S²PFC converter, the simulation-based study and design guideline has been done to the CCM VS-S²PFC converter. Figure 4.37 shows the circuit diagram of the CCM VS-S²PFC converter with feedback winding $N_1$. The flyback converter is chosen to be the DC/DC stage, because that flyback converter is more suitable for the VS-S²PFC converter. In this converter, the design of the DC/DC stage and controller is same as the design of the conventional flyback DC/DC converter, while the key design parameters is in the front-end PFC quasi-stage. The boost inductor $L_B$, the voltage-source capacitor $C_r$, and the feedback-winding ratio $N_1/N_p$ are the three important design parameters.

Similarly, the major design objectives includes: 1) the input current of this converter should meet IEC 61000-3-2 Class D specification; 2) the maximum bulk-capacitor voltage should be lower than the capacitor rated voltage with sufficient margins; 3) the converter should have good efficiency and low cost.

As a design example, the simulation circuit is designed to have a narrow line input (180-265Vac) and 5V/20A output with flyback DC/DC stage. The key experimental circuit components have been chosen in the following range: $L_B$: 200 - 1200 µH, $C_r$: 3.3 - 10 nF, $N_1 / N_p = 0 - 0.5$. Switching frequency $f_s=100$ kHz.
Figure 4.37 Circuit diagram of the CCM VS $S^2$PFC converter for design study
(with 180 – 265 V$_{ac}$ input, 5V/20A – rated output)

Figure 4.38 Simulated input voltage and boost inductor current waveforms of the VS-$S^2$PFC converter (at 230 V$_{ac}$ input, 5V/20A output, $L_B=800 \ \mu H$, $C_r=4.7 \ \text{nF}$, $N_1/N_p=0.5$, $f_s=100 \ \text{kHz}$)
4.5.2 Design considerations of the key parameters in the CCM VS S²PFC converter

4.5.2.1 Feedback winding ratio \(\frac{N_1}{N_P}\)

As discussed in previous sections, a large feedback winding ratio \(\frac{N_1}{N_P}\) is always preferred in the S²PFC converter to get low bulk-capacitor voltage stress, the “direct-energy-transfer” effect with reduced switch current stress, and therefore, good efficiency. In the CCM VS S²PFC converter, it is also desirable to get a high \(\frac{N_1}{N_P}\) ratio. Different from the CS S²PFC converter, there is no dead-conduction angle come with a high \(\frac{N_1}{N_P}\) ratio, as shown in the simulated waveform in Fig. 4.38. The VS S²PFC converter does not have a clear dead conduction angle on the input current because the initial VS-capacitor voltage \(v_{C_r}(0)\) compensates the winding voltage \(v_{N_1}\) at the switch turn-on moment in each switching cycle. Nonetheless, a high \(\frac{N_1}{N_P}\) ratio causes distortion on the input current. The trade-off on feedback ratio \(\frac{N_1}{N_P}\) is still between the input current distortions and the low-voltage and current stress. In an optimized design, the maximum \(\frac{N_1}{N_P}\) ratio is chosen while the converter input current can still meet IEC limits. Based on our experience from simulation, the maximum feedback ratio \(\frac{N_1}{N_P}\) is in the range 0.5-0.6. In our design, \(\frac{N_1}{N_P}=0.5\) is chosen in the first step of the design.

4.5.2.2 Voltage Source Capacitor \(C_r\)

After the feedback ratio \(\frac{N_1}{N_P}\) is determined, the next study is focus on the choice of the VS capacitor \(C_r\). As discussed in previous sections, to achieve strong modulation effect to shape the input current, a large capacitance of \(C_r\) is preferred. On the other side, to achieve low bulk-capacitor voltage stress and low switch current stress, a small \(C_r\) is preferred. To study \(C_r\) ‘s effects on the input current harmonics and the bulk-capacitor voltage \(V_B\), a series of close simulations have been done with fixed \(L_B\) and \(\frac{N_1}{N_P}\) values.
Figure 4.39 Simulated boost inductor current waveforms with different VS-capacitance $C_r$

(at $230\, \text{V}_{\text{ac}}$ – input, 5V/20A-output, and fixed $L_B = 800\, \mu\text{H}$, $N_1/N_P = 0.5$, $f_s=100\, \text{kHz}$)
Fig. 4.40 Comparison between the simulated input current harmonics and IEC-ClassD standard with 10% margin

(3\textsuperscript{rd}, 5\textsuperscript{th}, 7\textsuperscript{th}, 9\textsuperscript{th}, and 11\textsuperscript{th} harmonics, fixed $L_B=800\mu$H and $N_1/N_p=0.5$)
Figure 4.39 shows the simulated boost inductor current $i_{LB}$ waveforms with fixed $L_B$ and varied VS capacitor $C_r$, at 230 $V_{\text{RMS}}$ nominal line input and full load output. The capacitance of $C_r$ has been chosen as 3.3 nF, 4.7 nF, 6.1 nF and 8.1 nF, respectively. As shown in Fig. 4.39, when $C_r$ is small, the input current has high distortion. With the increase of $C_r$ from 3.3 nF to 8.1 nF, the input current THD decreases from 77% to 60%. In addition, Fig. 4.40 shows the 3rd, 5th, 7th, 9th, and 11th input current harmonics vs. the VS capacitance $C_r$. Figure 4.40 also shows that each order of current harmonics decreases with $C_r$ increases.

There are two reasons that a larger $C_r$ offers better input current waveform and lower current harmonics. First, as discussed in Chapter 2, a large $C_r$ provides a strong modulation effect on the boost inductor $L_B$ and strong shaping of the input current. Second, as discussed in Chapter 4, the bulk-capacitor voltage $V_B$ is proportional to VS capacitance $C_r$. If the capacitance of $C_r$ is too small, voltage $V_B$ can be lower than the peak of instantaneous input voltage, which violates the boost condition and high distortion occurs on the boost inductor current. Figure 4.41 provides the simulation waveform to verify this conclusion. As shown in Fig. 4.41 (a), when $C_r$ equals to 3.3 nF, voltage $V_B$ is below peak input voltage $v_{\text{in(peak)}}$, results in high distortion on $i_{LB}$ waveform. By increasing $C_r$, as shown in Fig. 4.41(b), $V_B$ is higher than $v_{\text{in(peak)}}$ and input current waveform has much less distortion.

However, it is necessary to point out that $C_r$ can not be too large. Otherwise the VS S^2PFC converter will have a bulk-capacitor voltage stress higher than 450 V, so that a 450 V-rated electrolytic bulk-capacitor can not be used. Figure 4.42 shows the simulated maximum bulk-capacitor voltage $V_{B(\text{max})}$ vs. VS capacitance $C_r$, with fixed $L_B=800\mu\text{H}$ and 265 $V_{\text{rms}}$ input voltage. As can be seen, the capacitor voltage stress increases with the increase of $C_r$. When $C_r$ is
Figure 4.41 Simulated waveforms shows that if $C_r$ is too small, the bulk-capacitor voltage $V_B$ can be lower than the peak-input-voltage and cause high-distortion on the input current.
Figure 4.42 Maximum bulk-capacitor voltage vs. VS-capacitance $C_r$

(at 265 $V_{ac}$ input, light load. $L_B=800\mu H$ and $N_1/N_P=0.5$)

Figure 4.43 Input current THD vs. the VS-capacitance $C_r$, the shaded area shows the design range of $C_r$ (at 230$V_{ac}$ input, full load)
higher than 7 nF, the margin on the capacitor voltage is less than 5% of the capacitor’s rated voltage, which is not acceptable. Summarizing the results in Fig. 4.40 and 4.42, Fig. 4.43 shows the acceptable design range of \( C_r \) for this particular case. As shown in Fig. 4.43, to meet IEC Class D specification with 10% margins as well as to limit the capacitor voltage stress to be lower than 430 V, the VS capacitor \( C_r \) has to be in the range from 3.6 nF to 7 nF. In this range, the optimal design point is close to \( C_r = 3.7-4.0 \) nF range, where the converter can meet IEC and also have low capacitor voltage stress, low switch current stress and high efficiency.

4.5.2.3 Boost inductor \( L_B \)’s effects on the input current THD and bulk-capacitor voltage stress

To further understand the VS \( S^2 \)PFC converter, another group of simulations have been done with fixed VS capacitance \((C_r=4.7\text{nF})\) but varied boost inductance \( L_B \). As discussed in Section 4.4, in the CS \( S^2 \)PFC converter, \( L_B \) has small effect on the input current harmonics and THD. However, simulation results show that this is not true for the VS \( S^2 \)PFC converter.

Figure 4.44(a) and (b) shows the simulated boost inductor current waveforms with fixed \( C_r \) but two different \( L_B \). As can be seen, by reducing boost inductance from 800 \( \mu \)H to 400 \( \mu \)H, the DCM part current on \( i_{LB} \) increases significantly. As a result, the input current THD decreases from 67% to 58%. Figure 4.45 further shows how the input current THD changes with \( L_B \). It is observed that, if \( L_B \) is larger than 800 \( \mu \)H in this particular converter, \( L_B \) has weak effect with input current THD. On the other side, if \( L_B \) is smaller than 800 \( \mu \)H, the input current THD decreases significantly with the \( L_B \) decreases. Figure 4.46 further shows that the bulk-capacitor voltage stress also has a strong relationship with \( L_B \), if \( L_B \) is less than 800 \( \mu \)H.

In conclusion, families of curves with different \( L_B \) and \( C_r \) are needed to further understand and design the VS \( S^2 \)PFC converter. This is an important future work of this research.
Figure 4.44 Boost inductor current waveforms with different $L_B$

(a) $L_B = 800 \mu H$, THD=67%

(b) $L_B = 400 \mu H$, THD=58%

Figure 4.45 Input current THD vs. boost inductance $L_B$

($V_{in}=230V$, $C_r=4.7nF$, full load)

Figure 4.45 Input current THD vs. boost inductance $L_B$

(at 230 $V_{RMS}$ input, full load, fixed $C_r=4.7 nF$, $N_1/N_p=0.5$, $f_S=100$ kHz)
Figure 4.46 Bulk-capacitor voltage stress vs. boost inductance $L_B$
(at 265 V_{RMS} input, light load, fixed $C_r=4.7$ nF, $N_1/N_F=0.5$, $L_F=600 \ \mu H$, $f_s=100$ kHz)
4.6 SUMMARY

This chapter provides the study on the bulk-capacitor voltage stress and switch current stress in the S²PFC converters, as well as the design considerations of the CCM CS and VS S²PFC converters.

It starts with a study on the conventional boost converter, for which the equations of the bulk-capacitor voltage \( V_B \) in the DCM and CCM PFC operations have been derived to understand \( V_B \) in the S²PFC converters. It shows that in the CCM S²PFC converters, the averaged effective duty-cycle \( \langle d_{eff} \rangle \) determines the bulk-capacitor voltage \( V_B \). And \( \langle d_{eff} \rangle \) of the CCM S²PFC converters changes with different feed-forward component parameters, which are generalized as the impedance \( Z_B \) in the boost charging and discharging paths. In general, larger boost impedance \( Z_B \) offers smaller effective duty-cycle \( d_{eff} \) and lower capacitor voltage \( V_B \). Furthermore, the averaged effective duty-cycle \( \langle d_{eff} \rangle \) as well as the bulk-capacitor voltage stress \( V_{B(max)} \) can be further reduced by the feedback windings \( N_1 \) and \( N_2 \). In addition, the analysis on the switch current also shows that a large \( Z_B \) and feedback winding reduce the switch current stress, therefore, increase the converter efficiency.

Next, the design considerations of the CCM CS S²PFC converter have been presented. The objectives are to minimize the converter voltage stress and semiconductor losses, while still maintain the input current harmonics to be lower than the specifications. The simulation and experimental study provide the design curves and results of the CS S²PFC converter. The tested data prove that the CCM S²PFC converter has superior performance than the DCM S²PFC converters with universal-line input. The VS S²PFC converter is also studied with simulation results. The primary results show that the design of VS S²PFC converter is quite complicated, which are needed to be solved in the future research.