A Hybrid DSP and FPGA System for Software Defined Radio Applications

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Master of Science
In
Electrical Engineering

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Dr. Patrick Schaumont, Member

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Description of item under review for fair use: Figure 2.2: Input connector of the COM-2001 DAC [7]

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Description of item under review for fair use: Figure 2.3: Wiring and prototyping board for the TMS320C6455 DSK [34]


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Description of item under review for fair use: Table 2.1: External memory (EMIF) expansion connector pinout [5]

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Description of item under review for fair use: Figure 2.5: Timing Diagram for the EMIF interface in the writing mode [13]


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Description of item under review for fair use: Figure 3.2: Direct down-converter used in the project [8]


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Description of item under review for fair use: Figure 3.3: Output of the COM-3002B receiver module [8]

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Description of item under review for fair use: Figure 3.7: DC blocking filter block diagram [4]


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Description of item under review for fair use: Table 3.4: Host Port Interface (HPI) external connector pinout [5]

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Description of item under review for fair use: Figure 3.19: HPI strobe control logic [16]

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Description of item under review for fair use: Table 3.5: Access type based on control signal value [16]

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Description of item under review for fair use: Figure 3.20: HPI interface DMA logic [16]

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Description of item under review for fair use: Figure 3.21: HPI interface write timing diagram [16]

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Description of item under review for fair use: Figure 4.4: TMS320C6455 DSK Memory Map [5]

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Description of item under review for fair use: Table 4.1: Partial TMS320C6455 internal memory map [23]

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Description of item under review for fair use: Table 4.8: Configuration switched for different DSP boot options [5]

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Description of item under review for fair use: Figure 4.21: Diagram of how FlashBurn works [33]

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