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In

Electrical Engineering

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Modeling and Control Design of a Bidirectional PWM Converter for Single-Phase Energy Systems

Dong Dong

Abstract

This thesis proposes a complete modeling and control design methodology for a multifunctional single-phase bidirectional PWM converter in renewable energy systems. There is a generic current loop for different modes of operation to ease the transition between different modes, including stand-alone inverter mode, grid-tied inverter mode, grid-tied rectifier mode and grid-tied charger/discharger mode. Under stand-alone mode operation, ac voltage regulation is of importance because of the sensitive loads. In this thesis, different multi-loop-based control schemes are investigated and compared, especially between the load current feedback control, PR control and capacitor current loop control. It shows that PR controller reduces the steady-state error, while load current feedback controller improves the transient response. However, the load current feedback controller and capacitor current loop controller presents unstable outputs under some filter load condition. Single-phase d-q frame control is also studied. In order to ease the implementation effort, an unbalanced d-q frame control is proposed to achieve zero steady-state error voltage regulation without generating β-axis component. Based on the same principle, a d-q frame-based single-phase PLL is also proposed to achieve the fast dynamic response with the zero steady-state error phase tracking.

The entire control system is verified on a modified 7 kW single-phase PWM converter prototype with a simple DSP-based digital implementation. The load step response test is presented under different modes of operation. The controllers for stand-alone mode are also done under no load, 1 kW resistive load, 1kVar capacitive load, and non-linear load conditions verifying that the single-phase d-q achieves 70% steady-state error improvement if taking the normal PID controller as the baseline design. In the end, the proposed PLL is compared with the standard PLL by experiments showing that the steady-state error can be reduced by 80%.
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Chapter 1. INTRODUCTION

1.1. Thesis Background

With pressing demand for and limited production of chemical energy resources, such as petroleum and natural gas, energy problems have become more urgent, and have become a focus of people around the world. According to the latest reports from BP, the world reserves of petroleum now represent 41 years of production at the current rate [1]. So-called “energy crisis” has been a hot topic recently.

The direct consumption of chemical energy resources has significant environmental impacts. In particular, the emission pollution from vehicles, which leads to global warming, pushes governments to make efforts towards the development of clean renewable energy resources, such as wind, bio-gas, and solar energy to address energy and environmental problems. Figure 1.1 shows a plot of the world market of energy use by energy type [2].

![Figure 1.1: World market energy use by energy type](image)

Renewable energy technologies such as solar power, wind power, hydroelectricity, micro hydro power, biomass and biofuels could be used to replace conventional chemical energy resources. In 2006, about 18% of global energy consumption came from renewable resources. Wind power is growing at the rate of 30% annually, with a worldwide installed capacity of over 100 GW [3], and is widely used in several European countries and the United States [4]. The manufacturing output of the photovoltaic industry reached more than 2,000 MW in 2006 [5], and photovoltaic (PV) power stations are particularly popular in Germany [6]. Solar thermal power stations operate in the USA and Spain, and the largest of these is the 354 MW SEGS power plant in the Mojave Desert. The world's largest geothermal power installation is The Geysers in California, with a rated capacity of 750 MW [7]. Brazil has one of the largest renewable energy programs in the world, involving production of ethanol fuel from sugar cane, and ethanol now provides 18% of the country's automotive fuel. Ethanol fuel is also
widely available in the USA. Figure 1.2 shows the distribution of renewable energy use in 2006 [8].

Figure 1.2: Renewable energy distribution in 2006

As such, within recent years, interest has risen in the installation of solar-based, wind-based, and various other renewable distributed energy resources (DERs) and energy storage (ES) systems to transfer and transmit clean renewable energy into electrical-based energy.

1.2. Renewable Energy Systems Overview

Currently, industrial countries generate most of their electricity in large centralized facilities, such as coal, nuclear, hydropower or natural gas-powered plants. These plants have excellent economies of scale, but usually transmit electricity over long distances. Most plants are built this way due to a number of economic, healthy, safety, logistical, environmental, geographical and geological factors. For example, coal power plants are built away from cities to prevent their heavy air pollution from affecting the populace; in addition, such plants are often built near collieries to minimize the cost of transporting coal.

Distributed generation is another approach to the manufacture and transmission of electric power. It reduces the amount of energy lost in transmitting electricity because the electricity is generated very near where it is used, perhaps even in the same building. This reduces the size and number of power lines that must be constructed [9]. If renewable energy resources are used as distributed generation resources, the distributed hybrid power systems can also be referred as renewable energy systems. Figure 1.3 illustrated a typical renewable energy system with a conventional utility grid [9].
Distributed hybrid power systems (DHPS) consist of ac and dc sub-systems connected to various load types, where the DG resources can be either dc or ac sub-system-based [10]. A self-sustainable energy system has been built in the lab of Center for Power Electronics Systems (CPES), and was interconnected with a solar converter, a utility grid, and load in both the power and communication sense; in addition, a wind converter was wired to be part of the system.

The small-scale single-phase renewable energy system at CPES contains two major renewable energy sources: 5 kW PV solar panels, and a 3.5 kW wind turbine generator. The PV panels used in the solar array are Suntech PV panels, with a maximum power of 170 W per unit (Figure 1.4). The total power of the array is 5 kW, and it is interfaced with a Xantrex DC/DC converter featuring maximum power tracking capability. The wind turbine, also shown in Figure 1.5, is a Cleanfield Energy 3.5 kW turbine with a three-phase permanent magnet generator (PMG) with a rated wind speed of 12.5 m/s. The temporary energy storage for the system is a Nilar NiMH battery pack [11].
The critical component of this system is the bi-directional converter, which connects the dc and ac sub-systems together, and connects the system with the utility grid. Figure 1.6 shows a probable single-phase DHPS with energy storage on the dc side and other renewable energy resources through the system.

As we can see in Figure 1.6, the bi-directional single-phase converter in a distributed hybrid power system should fulfill the following modes of operation:

1. **Stand-alone inverter mode**: When the grid is lost, the converter regulates the ac bus voltage and frequency to sustain the ac load, while the renewable energy resources or energy storage on the dc side provide power. The ac-side renewable energy resources would act as current sources.

2. **Grid-tied inverter mode**: When the grid is connected, the converter acts as a current source to source or sink power to the grid to balance the power flow between the dc and ac subsystems, while one of the dc resources regulates the dc bus voltage.

3. **Grid-tied rectifier mode**: When the grid is connected, the converter regulates the dc bus voltage to sustain the dc load while all the dc-side renewable energy resources run as current sources.

4. **Grid-tied charger/discharger mode**: When the grid is connected, the converter charges energy storage elements, such as a battery pack. When the grid is lost, the battery discharges...
supplying power to sustain both the dc and ac load.

### 1.3. Single Phase Converter

The full-bridge pulse-width-modulation (PWM) single-phase converter is widely used in uninterruptable power supplies (UPS), wind and solar power dc-ac interfacing, stand-alone voltage regulators in distributed power systems, and many other industry applications. Single-phase converters are used where transformation between dc and ac voltage is required; more precisely where converters transfer power back and forth between dc and ac. The single-phase full-bridge converter in Figure 1.7 shows the basic circuit topology. Ac output voltage is created by switching the full-bridge in an appropriate sequence. The output voltage of the bridge, $v_{ac}$, can be either $+V_{dc}$, $-V_{dc}$ or 0 depending on how the switches are controlled [12].

![Figure 1.7: Single-phase full-bridge converter topology and its waveforms](image)

Notice that both switches on one leg cannot be ON at the same time; otherwise there would be a short circuit across the dc source, which would destroy the switches or the converter itself. Table 1.1 summarizes all the possible switching combinations for the single-phase inverter and their corresponding created full-bridge voltage, $v_{ac}$.

<table>
<thead>
<tr>
<th>Mode</th>
<th>$S1$</th>
<th>$S2$</th>
<th>$S3$</th>
<th>$S4$</th>
<th>$v_{ac}$</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>0</td>
<td>Freewheeling</td>
</tr>
<tr>
<td>II</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>$-V_{dc}$</td>
<td>-</td>
</tr>
<tr>
<td>III</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>$+V_{dc}$</td>
<td>-</td>
</tr>
<tr>
<td>IV</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>0</td>
<td>Freewheeling</td>
</tr>
</tbody>
</table>

### 1.4. Current Work on Single-phase Full-bridge Converter

Many grid-tied converter control strategies have been proposed in recent work, such as hysteresis control and predictive control for the grid-tied inverter mode [13, 14]; fuzzy control, sliding mode control, repetitive control for the stand-alone inverter mode [14-16]; and predictive control for the rectifier mode [17]. Few papers have addressed the seamless
transition between different modes [14-16]. Many of the existing methods actually require a
different control system for each mode of operation, which increases the complexity and
affects the reliability of the system, as well as causing difficulty in the transition between
modes. Moreover, the existing work has not explored all of the possible modes of operation;
the battery charger mode in particular has been neglected.

Among these different modes of operation, the ac voltage control under stand-alone
mode presents the most difficulty since the traditional control design for a dc/dc converter
cannot be applied directly to a dc/ac inverter. The main goal of a full-bridge converter control
system is to achieve a fast dynamic ac voltage and frequency regulation during transients,
while maintaining zero steady-state error under different types of loads. Many control
schemes for this converter have been proposed during the past years.

Deadbeat control [18-21] has been proposed for use in uninterruptable power supply
(UPS) applications for many years. It can achieve very fast dynamic response for digital
implementation. However, a deadbeat control technique requiring exact system parameters
and work environment is very sensitive to the system parameters, which can degrade the
performance or even the stability. The repetitive controller [15, 22] is another control
approach. It originates from the internal model principle, which has a good steady-state
performance; however, the transient performance is limited because the repetitive controller
cannot achieve sub-cycle response. Using sliding mode control [16, 23-24] as one of the
nonlinear controllers is also used in UPS applications. Sliding mode control is well-known for
its fast dynamic response and high robustness. The difficulties with this control mode are
determining a suitable sliding surface, its chattering phenomena, and limited switching
frequency. Many papers apply non-linear adaptive control schemes to UPS inverters [25-27],
including the popular model of reference adaptive controllers and self-tuning regulator.
However, the computational complexity is high, not practical to reduce the cost of the digital
signal processor. Other non-linear controllers, such as online trained neural network controller
[28-29], also have drawbacks due to their high computational complexity. Compared with
these, multi-loop current-voltage PID controls based on frequency response analysis represent
advantages in terms of design simplicity and ease of implementation, providing a predictable
stability region and a good regulation performance. However, a steady-state error always
exists for PID regulators due to the finite gain they present at 60 Hz (line frequency), and
their performance depends on the actual load conditions. To address this problems, several
improvement schemes have been proposed, namely load-current feed-back [30-31],
proportional plus resonant (PR) controls [32-34], and single-phase d-q frame controls with
imaginary stationary β-axis terms [35-41].

1.5. Thesis Objective and Outline

This thesis proposes a complete modeling and control mythology to design the control
system for a single-phase bidirectional PWM converter for different modes of operation. The
thesis focuses on ac voltage regulation at stand-alone mode to achieve zero steady-state error
under large load variations. The mode transition and system-level operation is also discussed
in this thesis.

Chapter 1 of this thesis details the application and motivations of this work while
Chapter 2 covers the modeling of a single-phase full-bridge converter at different modes of operation. Chapter 3 focuses on the control analysis and design of the system, and Chapter 4 concentrates more on the voltage control at stand-alone mode of operation. Chapter 5 presents the single-phase PLL design and mode of transfer. Finally, the conclusion and future work is summarized in Chapter 6.
Chapter 2. Modeling and Design of Multifunction Single-Phase Converter

2.1. Converter Modeling

As we know, the objective of this project is to build a set of control systems to make the single-phase converter work at different modes of operation. In order to design the control system, a set of mathematical differential equations describing the plant system need to be established according to KCL and KVL. As a physical system, the state variables of the control system should be the energy storage elements, such as the inductor current and capacitor voltage, as well as the control input variable, which are the PWM gate signals.

Before establishing the model of single-phase converter for different modes of operation, the parameters need to be defined beforehand, as shown in Table 2.1.

<table>
<thead>
<tr>
<th>Variables and parameters</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}$</td>
<td>Constant dc-link voltage</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>Dc-link voltage</td>
</tr>
<tr>
<td>$I_{dc}$</td>
<td>Average value of dc-link current</td>
</tr>
<tr>
<td>$i_{dc}$</td>
<td>Dc-link current</td>
</tr>
<tr>
<td>$i_l$</td>
<td>Ac inductor current</td>
</tr>
<tr>
<td>$s_a, s_b$</td>
<td>Phase leg switching function</td>
</tr>
<tr>
<td>$v_a, v_b$</td>
<td>Phase leg terminal voltage</td>
</tr>
<tr>
<td>$v_{ab}$</td>
<td>Full-bridge terminal voltage</td>
</tr>
<tr>
<td>$s_{ab}$</td>
<td>Full-bridge switching function</td>
</tr>
<tr>
<td>$d_{ab}$</td>
<td>Averaged full-bridge switching function</td>
</tr>
<tr>
<td>$C_{ac}$</td>
<td>Ac output filter capacitor</td>
</tr>
<tr>
<td>$C_{dc}$</td>
<td>Dc-link capacitor</td>
</tr>
<tr>
<td>$L$</td>
<td>Ac line filter boost inductor</td>
</tr>
</tbody>
</table>
### 2.1.1. Modeling of Full-bridge Switches

The standard single-phase full-bridge converter topology consists of two phase legs. Each phase leg has two solid-state devices in series. Based on the functionality of the semiconductor switch, the solid-state switch can be represented as a single-pole-single-throw (SPST) ideal switch [43] when losses, parasitics and the interior structure are ignored, which is shown in Figure 2.1.

![Ideal switch representation](image)

Figure 2.1: Ideal switch representation

The switching function of the SPST switch is provided below.

\[
    s = \begin{cases} 
    1, & v(t) = 0, \text{if switch S is closed} \\
    0, & i(t) = 0, \text{if switch S is open} 
    \end{cases} 
\]  

(2.1)

Thereby, one phase leg switches can be represented as a single-pole-double-throw (SPDT) ideal switch with the same modeling method as shown in Figure 2.2.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{dc}$</td>
<td>Dc charging inductor</td>
</tr>
<tr>
<td>$Z_{dc}$</td>
<td>Dc side load</td>
</tr>
<tr>
<td>$Z_{ac}$</td>
<td>Ac side load</td>
</tr>
<tr>
<td>$v_o$</td>
<td>Ac output voltage</td>
</tr>
<tr>
<td>$v_{grid}$</td>
<td>Grid voltage</td>
</tr>
<tr>
<td>$v_{battery}$</td>
<td>Energy storage terminal voltage</td>
</tr>
<tr>
<td>$i_{battery}$</td>
<td>Energy storage current</td>
</tr>
</tbody>
</table>
2.1.2. Modeling of Stand-alone Inverter Mode

Applying the ideal SPDT instead of one phase leg switch gives the simplified inverter topology illustrated in Figure 2.3.

The switching function can be deduced in accordance with the inverter operation principle.

\[
\begin{align*}
V_a &= s_a \cdot V_{dc} \\
V_b &= s_b \cdot V_{dc} \\
\Rightarrow V_{ab} &= s_{ab} \cdot V_{dc}
\end{align*}
\]  

(2.2)

The switching model is calculated based on the power stage topology. All the passive components are on the ac side. Following are the state-space representation equations of this mode.

\[
\begin{align*}
v_{ab} &= s_{ab} \cdot V_{dc} \\
L \frac{di_L}{dt} &= v_{ab} - v_o \\
C_{ac} \frac{dv_o}{dt} &= i_L - \frac{v_o}{Z_{ac}}
\end{align*}
\]  

(2.3)
Applying the moving average operator $\frac{1}{T} \int_t^{t+T} x(t) \cdot dt$ to the switching model gives the average model:

$$\begin{align*}
\bar{v}_{ab} &= d_{ab} \cdot V_{dc} \\
L \frac{d\bar{i}_L}{dt} &= \bar{v}_{ab} - \bar{v}_o \\
C_{ac} \frac{d\bar{v}_o}{dt} &= \bar{i}_L - \frac{\bar{v}_o}{Z_{ac}}
\end{align*}$$

After rearrangement, the state-space representation is expressed below in matrix form.

$$\begin{bmatrix} \frac{\dot{x}}{\bar{v}_o} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\
-\frac{1}{C_{ac}} & -\frac{1}{Z_{ac}C_{ac}} \end{bmatrix} \begin{bmatrix} i_L \\
\bar{v}_o \end{bmatrix} + \begin{bmatrix} V_{dc} \\
0 \end{bmatrix} d_{ab}$$

As long as obtaining the state space representation, the plant model can be studied and then the design of controller can be looked into.

### 2.1.3. Modeling of Grid-tied Inverter Mode

The grid-tied inverter topology illustrated in Figure 2.4 is actually the same as the stand-alone inverter mode. The difference between them is that the ac capacitor is removed because its dynamics are ignored by the connection with the strong grid source.

![Figure 2.4: Ideal model of grid-tied inverter mode](image)

The switching model of the grid-tied inverter mode is as follows.

$$\begin{align*}
v_{ab} &= s_{ab} \cdot V_{dc} \\
L \frac{di_l}{dt} &= v_{ab} - v_{grid}
\end{align*}$$

The average model is shown below with the similar processing technique.
The model of the grid-tied inverter is simpler due to the nature of this first order system.

\[
L \frac{di_L}{dt} = d_{ab} \cdot V_{dc} - v_{grid} \tag{2.8}
\]

### 2.1.4. Modeling of Grid-tied Rectifier Mode

The topology of this mode is illustrated in Figure 2.5. It is clear to see that the capacitor is moved from the ac side to the dc side to stabilize the dc voltage and improve the transient response.

The following equations show the switching model of the rectifier mode. Note that the direction of dc-link current is reversed.

\[
\begin{aligned}
v_{ab} &= s_{ab} \cdot V_{dc} \\
iv_{dc} &= s_{ab} \cdot i_L \\
L \frac{di_L}{dt} &= v_{ab} - v_{grid} \\
C_{dc} \frac{dv_{dc}}{dt} &= i_{dc} - \frac{v_{dc}}{Z_{dc}}
\end{aligned} \tag{2.9}
\]

Applying the moving average operator on the switching model gives the average model as follows.

\[
\begin{aligned}
L \frac{di_L}{dt} &= d_{ab} \cdot \overline{v}_{dc} - v_{grid} \\
C_{dc} \frac{dv_{dc}}{dt} &= d_{ab} \cdot \overline{i}_L - \frac{\overline{v}_{dc}}{Z_{dc}}
\end{aligned} \tag{2.10}
\]

The matrix form of the state-space representation of the grid-tied rectifier mode is shown...
below.

\[
\begin{bmatrix}
\dot{v}_{dc} \\
\dot{i}_L
\end{bmatrix} = \begin{bmatrix}
\frac{1}{Z_{dc}C_{dc}} & \frac{d_{ab}}{d_{ab}} \\
\frac{L}{d_{ab}} & 0
\end{bmatrix} \begin{bmatrix}
v_{dc} \\
i_L
\end{bmatrix} + \begin{bmatrix}
0 \\
-1
\end{bmatrix} v_{grid}
\]

(2.11)

### 2.1.5. Modeling of Grid-tied Charger/Discharger Mode

Figure 2.6 shows the circuit of the charger/discharger mode. The difference between this mode and the rectifier mode is that with the charger/discharger mode, a charging inductor is hooked up on the dc side in series with an energy storage element, such as a battery.

![Ideal model of grid-tied charger/discharger mode](image)

In accordance with the topology of the charger/discharger circuit, the switching model can be derived as follows.

\[
\begin{align*}
v_{ab} &= s_{ab} \cdot v_{dc} \\
i_{dc} &= s_{ab} \cdot i_L \\
L \frac{di_L}{dt} &= v_{ab} - v_{grid} \\
C_{dc} \frac{dv_{dc}}{dt} &= i_{dc} - i_{battery} \\
L_{dc} \frac{di_{battery}}{dt} &= v_{dc} - v_{battery}
\end{align*}
\]

(2.12)

The average model can be derived with the same method used above;
The matrix form of the state-space representation of the grid-tied charger/discharger mode is shown below. As we can see, the grid-tied charger/discharger mode presents the most complicated system among all modes.

\[
\begin{bmatrix}
\dot{v}_{dc} \\
\dot{i}_{t} \\
\dot{i}_{battery}
\end{bmatrix} =
\begin{bmatrix}
0 & d_{ab} & -1 \\
\frac{d_{ab}}{C_{dc}} & 0 & 0 \\
\frac{1}{L} & 0 & 0 \\
\frac{1}{L_{dc}} & 0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{dc} \\
i_{t} \\
i_{battery}
\end{bmatrix}
+ \begin{bmatrix} 0 \\ -1 \\ 0 \end{bmatrix} v_{grid} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{battery}
\]

(2.14)

2.2. Modulation Scheme

2.2.1. Modulation Strategy

Pulse-width modulation (PWM) is used to create proper gating signals for four switches, the two main advantages of PWM are the control of the output voltage amplitude and fundamental frequency, and the filter requirements are decreased for minimizing the harmonics. The switches must be controlled in a certain sequence to create a sinusoidal output voltage in a single-phase inverter. So, a reference sinusoidal waveform is required. The reference waveform is also called the modulation or control signal and it is compared to a carrier signal. The carrier signal is usually a triangular signal that controls the switching frequency while the reference signal controls the output voltage amplitude and its fundamental frequency.

This section describes two common methods of modulation, bipolar and unipolar modulation [43]. Fig 2.7a illustrates bipolar pulse-width modulation. This method is called bipolar since the \( v_{dc} \) voltage of the full-bridge is either \(+V_{dc}\) or \(-V_{dc}\). When the reference signal is larger than carrier signal S1 and S4 are ON; and when the reference signal is smaller than the carrier signal, S2 and S3 are ON. In a unipolar PWM, the output is switched from either \(+V_{dc}\) or \(-V_{dc}\) to zero. Fig 2.7b illustrates the switching method for unipolar modulation where S1 and S2 are controlled using \( V_{sin} \), and S3 and S4 are controlled using \(-V_{sin}\).

Unipolar modulation has the particular attraction that it can be implemented with very simple circuitry since one phase leg maintains the inverse switch state of the other. However, unipolar modulation generates substantial carrier frequency and sideband harmonics, unlike the double carrier frequency and sideband harmonics generated by bipolar modulation. This is because unipolar modulation doesn’t cancel the harmonics between the two phase legs and
the reduced roll-off in magnitude of the baseband harmonics that occurs with this modulation strategy. Therefore, the bipolar modulation strategy is the natural selection.

![Figure 2.7: Unipolar and bipolar modulation scheme](image)

2.2.2. Carrier Selection

The carrier signal can be either a saw tooth or a triangular waveform. Both of these waveforms can generate the PWM signal. However, different carrier waveforms have different harmonics distributions.

The PWM signal can be observed by applying double Fourier integral analysis [43]. If applying the naturally sampled reference, single-edge carrier, the output waveform of the converter is

\[
v_{ab}(t) = 2V_{dc} M \cos(\omega_c t) + \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_m(m \pi M) \sin \frac{n \pi}{2} \cos(m \omega_c t + n \omega_s t) \quad (2.15)
\]

If applying the naturally sampled reference, double-edge carrier, the output waveform of the converter is

\[
v_{ab}(t) = 2V_{dc} M \cos(\omega_c t)
+ \frac{8V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} J_{2m-1}(m \pi M) \cos([m + n - 1] \pi) \cos(2m \omega_c t + [2n - 1] \omega_s t) \quad (2.16)
\]

The harmonics spectrum waveforms for both types of carrier are shown in Figure 2.8 and Figure 2.9.
Here we can see clearly that the triangular waveform type of carrier can cancel out the odd-ordered switching harmonics components, which profoundly reduce the total harmonics. Thus, the selection of carrier is the triangular waveform type.

2.3. Passive Components Design
### 2.3.1. Filter configuration Selection

For the grid-connection, ac output filter need to be considered. There are several prospective filters for choosing [44-47].

a. L filter  

b. LC filter  

c. LCL filter

![Figure 2.10: Three different types of filter](image)

The attenuation of the basic inductor filter shown in Figure 2.10(a) is -20 dB/decade over the whole frequency range. Since the converter needs to be run in stand-alone inverter mode, when using this filter, the inverter switching frequency has to be high enough to sufficiently attenuate harmonics. Normally only one L filter cannot meet the ripple reduction requirement.

The LCL filter shown in Figure 2.10(b), which is a three-order filter, has some advantages. It has low grid current distortion and reactive power production. It produces attenuation of -60dB/decade for frequencies in excess of the resonance frequency, and allows the possibility of using a given harmonic attenuation. On the other hand, the LCL filter may cause both dynamic and steady-state input current distortion due to resonance.

The LC filter is a second-order filter, giving -40 dB/decade attenuation. Since the previous L filter achieves low attenuation of the inverter switching components, a shunt element is needed to further attenuate the switching frequency components. This LC filter is suited to configurations where the load impedance across C is relatively high at and above the switching frequency.

For our baseline design, we take LC filter for our application, since it is easy to design and implement. The further comparison of LCL filter and LC filter will be studied in future work.

### 2.3.2. Filter Parameters Design

Some requirements need to be considered before designing the filter.

a. Current harmonics injections must meet the IEEE 1547 Standards [48], which is IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems

b. It is necessary to achieve better attenuation on the switching and high frequency harmonics.

c. The cut-off frequency should be higher than controller bandwidth
d. It must have a compact size and low power loss.

Using information from [48], the harmonics requirement is shown below in Table 2.1.

<table>
<thead>
<tr>
<th>Individual harmonic order h (odd harmonics)</th>
<th>Percent (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$h &lt; 11$</td>
<td>4.0</td>
</tr>
<tr>
<td>$11 \leq h &lt; 17$</td>
<td>2.0</td>
</tr>
<tr>
<td>$17 \leq h &lt; 23$</td>
<td>1.5</td>
</tr>
<tr>
<td>$23 \leq h &lt; 35$</td>
<td>0.6</td>
</tr>
<tr>
<td>$35 \leq h$</td>
<td>0.3</td>
</tr>
</tbody>
</table>

The total rms harmonics current should be less than 5% of the rated current. In practice, different modulation index results in different total demand distortion (TDD). Under a bipolar modulation scheme, the highest TDD occurs at the middle of the modulation index, which is around 0.6 in Figure 2.11. We take this modulation index as the worst case for our design consideration.

\[
TDD = \frac{I_{\text{harmonics rms}}}{I_{\text{rate}}} < 0.5\% 
\]  

(2.17)

The objective is

\[
v_{ab}(t) = 2V_{dc}M \cos(\omega_0 t) + \frac{8V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} J_{2n-1}(m\pi M) \cos([m+n-1]\pi) \cos(2m\omega_0 t + [2n-1]\omega_0 t) 
\]  

(2.18)
\[ I_{rate} = 70A \]
\[ M = 0.6 \]
\[ V_{dc} = 170V \]

Without consideration of other fault conditions, the minimum inductance is
\[ L = 220 \mu H \]  \hspace{1cm} (2.19)

The above method actually is a little overdesign, since normally the high frequency ripple comes from the switching action. The high switching noise should be attenuated by the EMI filter, not by boost inductor.

The second factor which should be taken account is the ripple current. The simple method is to ensure the current ripple is less than 20% of the current peak.

\[ L \frac{di}{dt} = V_L \]
\[ \Rightarrow 20\% \frac{P_o}{V_o} = V_{dc} - DV_{dc} \]
\[ \Rightarrow L = \frac{(V_{dc} - DV_{dc})DT_s}{20\% \frac{P_o}{V_o}} \]  \hspace{1cm} (2.20)

The calculated inductor is
\[ L = 170 \mu H \]  \hspace{1cm} (2.21)

This means that as long as the inductor is bigger than 220 uH, the current harmonics injected into the grid can be guaranteed. The capacitor is designed in light of two concerns. One concern is to enhance the output impedance to maintain the stability for large load variations. Another concern is that to maintain good attenuation, the cutoff frequency should be almost equal or larger than the bandwidth of the controller as well as less than the half of the switching frequency. The final design is one 75 \( \mu \)F film capacitor. Therefore, the cutoff frequency of this filter is
This is roughly around the 20th harmonic.
Chapter 3. CONTROL DESIGN OF MULTIFUNCTIONAL SINGLE-PHASE CONVERTER

3.1. Small-Signal Modeling and Control Structure

3.1.1. Stand-alone Inverter Mode

Although the operating point for duty-cycle is not constant because of the nature of sinusoidal output, the coefficients of the state space are a constant value. Therefore, at every operating point, the small-signal model is always the same, independent of the varying operating point. Therefore, we can deduce the small-signal model of the stand-alone inverter mode.

Applying the small-signal perturbation at any operating point gives

\[
\begin{bmatrix}
\tilde{i}_L + \tilde{i}_L \\
\tilde{V}_o + \tilde{V}_o
\end{bmatrix} = \begin{bmatrix}
0 & -\frac{1}{L} \\
\frac{1}{C_{ac}} & -\frac{1}{RC_{ac}}
\end{bmatrix} \begin{bmatrix}
\tilde{i}_L + \tilde{i}_L \\
\tilde{V}_o + \tilde{V}_o
\end{bmatrix} + \begin{bmatrix}
V_{dc} \\
0
\end{bmatrix} \tilde{d}_{ab}
\]

Based on the small-signal model, we can design the controller for stand-alone mode operation.

3.1.2. Grid-tied Inverter Mode

The small-signal model can be easily obtained from the average model using the following equation.

\[
\tilde{i}_L = \frac{V_{dc}}{L} \tilde{d}_{ab}
\]

3.1.3. Grid-tied Rectifier/Charger/Discharger Mode

Because the dc-link voltage is one of the state-variables for the grid-tied rectifier mode, the dynamic of the dc-link voltage should be taken into consideration, since it leads to the non-linearity for the rectifier mode. From the average state-space model, the state matrix is not constant, varying with the duty cycle. The Eigen-value of the system would be changing with the duty cycle. In other words, the characteristics of the system would vary all the time.

We cannot obtain the small-signal model since it is hard to select a proper operating point to inject the perturbation. We will see that at low frequencies, the system dynamics would be more affected by the dc-link capacitor. At high frequencies, the system dynamics are dominated by the line inductor. It is hard to model the middle frequency range since the system dynamics would be affected both by the dc-link capacitor and the ac line inductor. Although one paper [49] proposes a modeling method which can cover from dc up to half of
the switching frequency, the methodology is still not well accepted.

The fact is that our controller consists of an inner current loop and an outer voltage loop. It means that we don’t really need to know the whole system dynamics. We only need to know the high-frequency response for the current loop design, and low-frequency response for the outer loop design. We also know that at high frequencies the ac inductor dynamics would be dominant, so we just can ignore the influence from the dc-link capacitor. At the same time, we only consider the dc-link capacitor dynamics when looking at the low-frequency system response. Hence we can decouple the inner loop and outer loop. Then we can design the current loop and voltage loop separately.

3.2. Control Structure

The control structures for each mode are shown in Figures 3.1 to 3.4.

Figure 3.1: Stand-alone inverter mode control structure

Figure 3.2: Grid-tied inverter mode control structure
We can see that all modes have an inner-line inductor current loop. This paper proposes that all modes share the same inner current loop. In order to combine the inner current loops, the current loop dynamic response should be checked particularly at the crossover frequency. The proposed control structure is selected as double loop feedback controller as shown in Figure 3.5. The inner loop is selected as the ac current of the line inductor to achieve fast dynamic response for input disturbances, and the outer loop is designed with different compensators to regulate the desired control variables, such as ac voltage, dc voltage and dc charging current.
3.3. Generic Inner Current Loop Design

Figure 3.6 presents a simplified topology with all probable modes of operation of the passive components. Our main objective is to see the possibility of building a generic inner current loop for all modes of operation.

3.3.1. Stand-alone Inverter Mode

From the small-signal model, we know that the control-to-current small-signal transfer function at stand-alone inverter mode is:

$$G_{id} = \frac{i_{d}}{\Delta i_{dc}} = V_{dc} \frac{1 + sZ_{ac}C_{ac}}{Z_{ac} + sL_{ac} + s^{2}L_{ac}Z_{ac}C_{ac}}$$  \hspace{1cm} (3.3)$$

The plant transfer function is a two-order system which has double-pole, left half-plan zero.

3.3.2. Grid-tied Inverter Mode
The control-to-current small-signal transfer function at grid-tied inverter mode is
\[ G_{id} = \frac{\tilde{i}_L}{\tilde{d}_{ab}} = V_{dc} \frac{1}{sL_{ac}} \] (3.4)

### 3.3.3. Grid-tied Rectifier/Charger/Discharger Mode

For the grid-tied rectifier mode, since there is no fixed operating point and the dc-link voltage changes, the dynamics of both sides of the bridge should be considered. This results in a lack of a complete small-signal model covering from dc to half of the switching frequency [50]. However, we can model the current loop for only the high-frequency range and the voltage loop for only the low-frequency range. Therefore, the quasi-static modeling [50] is used to approximate the current loop. Firstly, the switching and average model of the full bridge is shown below.

\[
\begin{aligned}
    \tilde{v}_{dc} &= s_{ab}v_{dc} \\
    \tilde{i}_{dc} &= s_{ab}\tilde{I}_L \\
    \tilde{v}_{ac} &= d_{ab}\tilde{V}_{dc} \\
    \tilde{I}_{dc} &= d_{ab}\tilde{I}_L
\end{aligned}
\] (3.5)

The small signal model of the full-bridge is

\[
\begin{aligned}
    \tilde{v}_{ac} + \tilde{v}_{ac} &= (d_{ab} + \tilde{d}_{ab})(\tilde{v}_{dc} + \tilde{v}_{dc}) \\
    \tilde{I}_{dc} + \tilde{I}_{dc} &= (d_{ab} + \tilde{d}_{ab})(\tilde{I}_L + \tilde{I}_L) \\
\Rightarrow \tilde{v}_{ac} &= d_{ab}\tilde{v}_{dc} + \tilde{d}_{ab}\tilde{v}_{dc} \\
\tilde{I}_{dc} &= d_{ab}\tilde{I}_L + \tilde{d}_{ab}\tilde{I}_L
\end{aligned}
\] (3.6)

From the dc-side and ac-side power stages, the quadric-linear small-signal model of the full-bridge rectifier is:

\[
\begin{aligned}
    \tilde{v}_{ac} &= d_{ab}\tilde{v}_{dc} + \tilde{d}_{ab}\tilde{v}_{dc} \\
    \tilde{i}_{dc} &= d_{ab}\tilde{I}_L + \tilde{d}_{ab}\tilde{I}_L \\
    \tilde{v}_{ac} &= \tilde{I}_sL_{ac} \\
    \tilde{v}_{dc} &= \frac{Z_{dc}}{sZ_{dc}C_{dc} + 1}\tilde{i}_{dc}
\end{aligned}
\] (3.7)

Then, we can deduce the control-to-current loop transfer function
If we suppose the 120Hz ripple superimposed on the averaged dc voltage is very small, in other words, if we ignore the dc-link cap dynamics to the current loop, then

$$\ddot{V}_{dc} = \frac{1}{sZ_{dc}C_{dc}}(d_{ab} \ddot{T}_L + \ddot{d}_{ab} \ddot{T}_L) + \ddot{d}_{ab} V_{dc} - \ddot{V}_{dc} sL = 0$$

(3.8)

$$\Rightarrow \frac{d_{ab} Z_{dc}}{sZ_{dc}C_{dc} + 1 sL \ddot{L}_L} = \frac{-d_{ab} Z_{dc} \ddot{T}_L}{sZ_{dc}C_{dc} + 1} + \ddot{V}_{dc} \frac{d_{ab}}{sL \ddot{L}_L}$$

(3.9)

If we suppose the 120Hz ripple superimposed on the averaged dc voltage is very small, in other words, if we ignore the dc-link cap dynamics to the current loop, then

$$\ddot{V}_{dc} = V_{dc} + v_{ripple} \approx V_{dc}$$

$$-d_{ab} Z_{dc} \ddot{T}_L = V_{dc} + v_{ripple} \approx V_{dc}$$

Then the equation (3.8) can be simplified as

$$\frac{d_{ab} Z_{dc}}{sZ_{dc}C_{dc} + 1 sL \ddot{L}_L} = \frac{-d_{ab} Z_{dc} \ddot{T}_L}{sZ_{dc}C_{dc} + 1} + \ddot{V}_{dc} \frac{d_{ab}}{sL \ddot{L}_L}$$

(3.10)

The current compensator can be designed based on the above equations. The problem is that for different modes of operation, the plant of the system changes. The rectifier and charger/discharger modes have the worst situations since the steady-state operating point is not constant, which leads to difficulty in controller design. However, looking at the bode plot of the control to current transfer function for different modes of operation shown in Fig 4-6, we see that in stand-alone inverter mode, different load values change the low-frequency response around the resonance. For the grid-tied rectifier mode, different load values change the low frequency response as well. At different operating points, the low frequency response combines with the resonance shifts. However, compared with the stand-alone inverter mode, the resonance of the rectifier is always lower than that of inverter because the dc-link capacitor is normally much larger than the ac line capacitor.
From the bode plots, we can see that for all the different modes under different conditions the system has the same frequency response after the resonant pole. Thus, if the designed current loop controller can achieve very high cross-over frequency, all of the small signal transfer functions of the different modes can be reduced to

\[
G_{sd} = \frac{\tilde{i}_d}{d_{ab}} = V_{dc} \frac{1}{sL_{ac}} \tag{3.11}
\]

The reduced small-signal model is only related to the dc-link voltage and the ac line inductor value. This means that different modes of operation will have different phase/gain values at low frequencies, but the same bandwidth and phase margin can be achieved for all
modes at mid to high frequencies. It is possible to design a single ac current controller for all of the modes, with the only requirement being that the bandwidth is large enough to cover all modes of operation [51].

The difference between the low-frequency responses can be compensated through the use of an integrator. Since the inverter mode is the worst case, the current loop compensator is designed for this case. The design of the current compensator is performed under light or no-load conditions.

### 3.3.4. Current Loop Design

After the sensor, we implement a low-pass filter to filter out the noise picked up by the environment. The low-pass filter for the current sensor is a two-order low-pass filter. The specifications are

$$G_{LPF} = \frac{1}{(\frac{s}{\omega_o})^2 + (\frac{s}{Q\omega_o}) + 1}$$

$$\omega_o = 2\pi f_o = 2\pi \times 7.35 \times 10^3 \text{ rad/s}$$

$$Q = 0.73$$

For a digital modulator, at least one switching period time delay needs to be counted in our current loop. We use the Pade transfer function to mimic the digital time delay.

$$G_{delay} = e^{-sT_{delay}} \frac{1 - 0.5sT_{delay} + (sT_{delay})^2 / 12}{1 + 0.5sT_{delay} + (sT_{delay})^2 / 12}$$

The current loop block diagram is shown in Figure 3.10.

![Current loop block diagram](image)

**Figure 3.10: Current loop block diagram**

The current open loop gain can be obtained based on Figure 3.10

$$G_i = G_{LPF} \cdot G_{id} \cdot G_{delay}$$

The bode plot of the current loop gain is shown in Figure 3.11
The current compensator is designed under light load conditions. The designed current compensator is as follows,

\[
H_i = 46444.44 \frac{(s + 8333)(s + 1.408 \times 10^4)}{s(s + 1.961 \times 10^3)(s + 6.25 \times 10^3)}
\]

(3.15)

Two zeros are placed around the resonant pole to compensate the phase shift to obtain enough phase margin, and two poles are placed before half of the switching frequency to attenuate the switching frequency gain. One integrator is placed to enhance the gain at the low-frequency component. The proportional gain is tuned to make the crossover frequency large enough.

The compensated current loop is shown below in Figure 3.12.
In Figure 3.12, the crossover frequency is 2.87 kHz, the phase margin is 26.4°, and the gain margin is 2.7dB.

**3.4. Outer Loop Controller Design**

**3.4.1. Stand-alone Inverter Mode**

After designing the current compensator, the current-to-voltage transfer function is

\[
G_{vi} = \frac{V_o}{i_L} = \frac{Z_{ac}}{1 + sZ_{ac}C_{ac}} \quad (3.16)
\]

The voltage sensor filter is the same as current sensor filter, which is

\[
G_{LPF} = \frac{1}{\left(\frac{s}{\omega_o}\right)^2 + \left(\frac{s}{Q\omega_o}\right) + 1} \quad (3.17)
\]

\[
\omega_o = 2\pi f_o = 2\pi \times 7.35 \times 10^3 \text{rad/s}
\]

\[
Q = 0.73
\]

The voltage loop includes the inner current loop. We need obtain the closed-loop current transfer function, as shown in (3.18).

\[
G_{i-CL} = \frac{H_i G_{id} G_{delay}}{1 + H_i \cdot G_{LPF} \cdot G_{id} \cdot G_{delay}} \quad (3.18)
\]
The block diagram of the voltage loop is shown in Figure 3.13.

![Figure 3.13: Voltage loop block diagram](image)

The voltage open-loop gain can be obtained based on Figure 3.13.

\[
G_v = G_{LPF} \cdot G_{vi} \cdot G_{delay} \cdot G_{r, CL} \quad (3.19)
\]

The bode plot of current loop gain is shown in Figure 3.14

![Figure 3.14: Voltage loop gain](image)

We can see that due to the existence of the current compensator, the resonant poor has been compensated, which simplifies the design of the voltage compensator. The voltage compensator is still designed under the same load conditions. The designed voltage compensator is as follows.

\[
H_v = \frac{0.1 (s + 3885)(s + 6.41 \times 10^4)}{s(s + 2.44 \times 10^4)} \quad (3.20)
\]
Two zeros are placed around the crossover frequency to compensate the phase shift to obtain enough phase margins. One pole is placed before half of the switching frequency to attenuate the switching frequency gain. One integrator is placed to enhance the gain at low frequencies component. The proportional gain is tuned to make the crossover frequency large enough.

The compensated voltage loop is shown below.

---

**3.4.2. Grid-tied Rectifier Mode**

**3.4.2.1. Control Design**

The voltage loop is designed under the presumption that the current loop has already been designed and it can track the current reference very well. This means, the inductor dynamics can be ignored. Since the voltage loop is very slow, we can use power balance [52] to model the voltage loop.

---

**Figure 3.16: Input and output of rectifier mode**
in which, \( V_{ac RMS} I_{ac RMS} \) is the input power, while \( V_{dc} I_{dc} \) is the output power. The voltage controller can be modeled as follows based on the control configuration in Figure 3.3.

\[ I_{ac RMS} = V_c \frac{V_{ac RMS}}{K} \]  

(3.22)

in which, \( V_c \) is the output of the voltage loop, and \( K \) is the scaling factor of the sensor. Combining these two equations gives

\[ I_{ac RMS} = V_c \frac{V_{ac RMS}}{K} \]  

(3.23)

Exerting a perturbation on this equation gives

\[ (V_c + \tilde{V}_c) \frac{V_{ac RMS}^2}{K} = (V_{dc} + \tilde{V}_{dc})(I_{dc} + \tilde{I}_{dc}) \]

\[ \Rightarrow \tilde{I}_{dc} = \frac{2M \tilde{V}_{ac}}{r_o} + \frac{V_{ac RMS} \tilde{V}_c}{KM} - \frac{1}{r_o} \tilde{V}_{dc} \]  

(3.24)

in which,

\[ r_o = \frac{V_{dc}}{I_{dc}} \quad M = \frac{V_{dc}}{V_{ac RMS}} \]  

(3.25)

The equivalent circuit is shown below.

![Figure 3.17: Small-signal equivalent circuit of rectifier mode](image)

If a resistor load is connected,

\[ \frac{\tilde{V}_{dc}}{\tilde{V}_c} = \frac{V_{ac RMS}}{KM \left[ 2 + sC_{dc} R_{dc} \right]} \]  

(3.26)

The voltage loop transfer function is shown in Figure 3.18.
The voltage compensator is designed based on light-load conditions. The designed voltage compensator is as follows.

\[
H_v = \frac{508.14s + 8.32}{s(s + 118)}
\]  

(3.27)

One integrator is placed at zero frequency to achieve infinite loop gain at dc component to eliminate the dc error. One zero is placed to cancel the plant zero and another pole is placed after the crossover frequency to attenuate the loop gain at the 120Hz component. The compensated the voltage loop transfer function is shown below.
3.4.2.2. DC Ripple Analysis

One interesting scenario at the rectifier mode is the dc-link voltage ripple. The dc-link ripple should be as small as possible, and is analyzed here. Figure 3.20 shows the equivalent circuit on the ac side of the single-phase converter.

On the ac side, the terminal of the converter can be modeled as a controllable voltage source, and then we can get the above equivalent circuit. We suppose $V_{ac}$ is much greater than $\omega LI_{ac}$. 

Figure 3.19: Compensated voltage loop gain at rectifier mode

Figure 3.20: Equivalent circuit on ac side of the converter
\[ d = \frac{\sqrt{V_{ac}^2 + (\omega LI_{ac})^2}}{V_{dc}} \sin(\omega t - \varphi) \]

\[ \Rightarrow d \approx \frac{V_{ac}}{V_{dc}} \sin(\omega t) = \sqrt{2} \frac{V_{acRMS}}{V_{dc}} \sin(\omega t) = \sqrt{2} D_{max} \sin(\omega t) \]

Then we suppose \( V_{dc} \gg v_{dc\_ripple} \), so the load voltage is constant.

\[ I_{load} = \frac{P}{V_{dc}} \] (3.29)

Then

\[
\begin{cases}
    d = \frac{\sqrt{2}}{V_{dc}} V_{acRMS} \sin(\omega t) \\
    I_{dc} = \frac{2}{V_{dc}} \sqrt{2} I_{acRMS} \sin(\omega t) = \frac{2P}{V_{acRMS}} \sin(\omega t) \\
    \Rightarrow I_{dc\_rail} = dI_{dc} = \frac{2P}{V_{dc}} (\sin(\omega t))^2
\end{cases}
\]

Making \( I_{dc\_rail} = I_{load} \) gives \( \omega t = \frac{\pi}{4}, \frac{3\pi}{4} \).

\[
\Delta v_{dc\_val} = \frac{1}{C_{dc}} \int_0^{\frac{3\pi}{4\omega}} (I_{dc\_rail} - I_{load}) dt = \frac{1}{C_{dc}} \int_0^{\frac{3\pi}{4\omega}} \left( \frac{2P}{V_{acRMS}} \sin(\omega t) \right)^2 dt = \frac{P}{\omega V_{dc} C_{dc}} \]

(3.31)

The waveforms of the currents can be compared in Figure 3.21.

![Diagram showing current profiles](image)

**Figure 3.21:** Current profile on both ac and dc side within half line cycle

Thus, we know the expression of dc voltage ripple is
For our operation requirement, the ac side rms voltage is 120 V, and the dc side is 340 V. The dc side capacitance of the converter is 7.5 mF. Thus for full power of 7 kW, the dc ripple (peak-peak) would be 7 V. For light power of 700 W, the dc ripples (peak-peak) are 0.7 V.

3.4.3. Grid-tied Charger/Discharger Mode

The difference between the rectifier mode and the charger/discharger mode is the outer loop control variable. Since both modes have the same pulsating power characteristics, the outer loop modeling method is similar for each mode. We can use the same small-signal equivalent circuit to design the outer loop controller. The equivalent circuit is shown below in Figure 3.22.

![Small signal equivalent circuit of charger/discharger mode](image)

\[
\Delta V_{dc,peak} = \frac{P}{oV_{dc}C_{dc}} \tag{3.32}
\]

In which

\[
r_o = \frac{V_{dc}}{I_{dc}} , M = \frac{V_{dc}}{V_{ac,RMS}} \tag{3.34}
\]

Then we can get

\[
\tilde{i}_d = g_c \tilde{v}_c - \frac{1}{r_o} \tilde{v}_{dc}
\]

\[
\Rightarrow \tilde{i}_d = g_c \tilde{v}_c - \frac{1}{r_o} \frac{sL_{dc}}{1 + s^2L_{dc}C_{dc}} \tilde{i}_d \tag{3.35}
\]

\[
\Rightarrow \frac{\tilde{i}_d}{\tilde{v}_c} = \frac{g_c}{1 + \frac{1}{r_o} \frac{sL_{dc}}{1 + s^2L_{dc}C_{dc}}} = \frac{V_{ac,RMS}}{KM} \frac{1}{r_o \frac{1}{1 + s^2L_{dc}C_{dc}}}
\]
The compensator is designed based on the above small-signal transfer function. The normal operation is selected as 5 A current and 300 V dc voltage. At the normal condition, the compensator is as follows:

\[ H_v = \frac{1}{s(s + 96.3)} \]  

(3.36)

One integrator is placed at zero frequency to achieve infinite loop gain at the dc component to eliminate the dc error. One pole is placed after the crossover frequency to attenuate the loop gain at the 120 Hz component.

The compensated voltage loop transfer function is shown below.

Figure 3.23: Compensated voltage loop

The bandwidth of the designed dc current loop is 6.35 Hz, phase margin is 67.4°.

3.5. Experimental Evaluation

3.5.1. General Description

The control designs are evaluated by experiment. The experiment setup specifications are shown below in Table 3.1, and the hardware is shown in Figure 3.24. The critical component is the modified 7 kW single-phase bidirectional converter. The prototype of this converter is the TBwoods commercial three-phase motor drive. More information on the modification can
be found in Appendix A.

### Table 3.1: System Test Setup and Parameters

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modified 7 kW single-phase converter</td>
<td>1.2 mH ac line inductor (L)</td>
</tr>
<tr>
<td>1.5 mH dc charging Inductor (L_{dc})</td>
<td>Nilar NiMH Battery pack</td>
</tr>
<tr>
<td>75 μF filter capacitor (C_{ac})</td>
<td>6 kW resistive load (Z_{ac})</td>
</tr>
<tr>
<td>7.4 mF dc-Link capacitor (C_{dc})</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3.24: System setup, photo by author

The single-phase converter hardware and test setup are showed below. The different modes of operation are verified. The inverter mode and load transient response is first connected to a 300 V dc-link voltage source. The grid-tied inverter mode is then tested with different power factors to see the reactive power compensation capability. This is followed by testing in the grid-tied rectifier mode with load transient response verification. In the end, the grid-tied charger mode is verified by using the Nilar NiMH battery pack.

### 3.5.2. Stand-alone Mode Test

The stand-alone mode test is done under resistive load condition to generate a 120 V rms output voltage, with the equivalent output power as 5 kW. One ac relay is connected in series with the load to do the load step response test between no loads and full loads. Figure 3.25 shows the load step response from no loads to full loads. The transient response with small output voltage dip is shown clearly in the figure, presenting fast dynamic response under this mode. Also the test from full load to no load is shown in Figure 3.26. The transient looks pretty slow due to the reason that the relay switch can really disconnect the load at the current zero crossing for the existence of the arch. The scope scale is 10 A/DIV for current waveform, and 100 V/DIV for voltage waveform.
3.5.3. Grid-tied Inverter Mode Test

The Grid-tied inverter mode is done under a 2 kW power condition. The grid is 120 V rms. Figure 3.27 to 3.39 show the power factor angle control to verify the active and reactive power regulation and bi-directional power control capability. Figure 3.27 shows the pure reactive power control, which means the phase shift between ac current and voltage is 90°. Figure 3.28 and 3.29 shows the generative and regenerative current regulation. The scope scale is 5 A/DIV for current waveform, and 100 V/DIV for voltage waveform.
Figure 3.27: 90 degree power factor (pure reactive power mode) at grid-tied inverter mode

Figure 3.28: Unity power factor (generative mode) at grid-tied inverter mode

Figure 3.29: 180 degree power factor (re-generative mode) at grid-tied inverter mode

3.5.4. Grid-tied Rectifier Mode Test

The Grid-tied rectifier mode is done under a 5 kW power condition. Similarly, the grid
voltage is 120 V rms. The equivalent resistor load is connected on the dc side. Also, a high power rated solid-state switch is used to switch in and out the dc load. Figure 3.30 shows the load step change from no loads to full loads. Still, the voltage dip happens during transient time, but it can return to the rated voltage reference very fast, only within one line-cycle. For the load step change from full load to no load, it is also shown in Figure 3.31. Also, the transient spike looks acceptable. The scope scale is 10 A/DIV for ac current waveform, 100 V/DIV for dc-link voltage waveform, 200 V/DIV for grid voltage waveform, and 10 A/DIV for dc load current.

![Image](image1.png)

Figure 3.30: No load to full load at grid-tied rectifier mode

![Image](image2.png)

Figure 3.31: Full load to no load at grid-tied rectifier mode

3.5.5. Grid-tied Charger/discharger Mode Test
Finally, the Grid-tied charger/discharger mode is done with the battery on the dc-side. Due to the power limitation of the battery, the test is finished under small power condition, which around 1 kW. Also, different power factor angle control is carried out on the ac side. It means by achieving the same active power delivery, the reactive power is regulated by different phase angle. In Figure 3.28 shows the transient response between charging mode to discharging mode. So, the battery current goes from positive to negative. In Figure 3.29, the power factor step response test is did showing the fast dynamic response. The scope scale is 10 A/DIV for ac current waveform, 100 V/DIV for dc-link voltage waveform, 100 V/DIV for grid voltage waveform, and 10 A/DIV for dc charging current.

![Figure 3.32: Unity power factor charging at grid-tied charger/discharger mode](image1)

![Figure 3.33: 60 degree power factor charging at grid-tied charger/discharger mode](image2)
Figure 3.34: Mode transition from charging mode to inverter mode

Figure 3.35: Mode transition from leading power factor inverter mode to unity power factor inverter mode
Chapter 4. Zero Steady-state Voltage Control at Stand-alone Mode with Large Load Variation

4.1. Existing Method

As discussed in Chapter 1, using multi-loop voltage control for a single-phase PWM inverter is more attractive for its design simplicity, ease of implementation and the predictability of stability. In this chapter, the main multi-loop control methods are investigated and compared. Based on the implementation method, the control schemes can be categorized into two types: stationary frame control and synchronous frame control.

4.2. Stationary Frame Control

4.2.1. Overview

Voltage regulation performance is highly dependent on the load conditions in single-phase inverters. This can be explained by looking at the following inductor current to voltage transfer function.

\[ G_{vq} = \frac{v_q}{i_L} = \frac{Z_{ac}}{sZ_{ac}C_{ac} + 1} \]  

where \( Z_{ac} \) is the load impedance and \( C \) is the filter capacitance. Under heavy load conditions, \( sZ_{ac}C_{ac} \ll 1 \) is valid below the outer loop crossover frequency. Thus (4.1) can be reduced to

\[ G_{vq} = \frac{v_q}{i_L} = Z_{ac} \]  

Furthermore, under heavy load conditions, the voltage loop gain varies with the load impedance, and as such, a heavy load leads to a low gain in the voltage loop, as shown in Figure 4.1. Hence, with a fixed voltage loop compensator, the heavier loads lead to larger steady-state errors.
4.2.2. Load Current Feedback Control and PR Control

The PI controller can provide good regulation for the dc voltage due to the infinite gain at the dc component. However, the PI controller has a steady-state error when regulating the 60 Hz sinusoidal voltage because of the finite gain at 60 Hz frequency. As shown in Figure 4.2, some papers have proposed a proportional gain plus load-current feedback to cancel out load variations and to handle large load variations [30-31]. The voltage loop diagram is shown in Figure 4.3.
This control scheme is easy to design and implement, and has a relatively good performance because the decoupling can make the system an ideal first-order system. The outer loop would become

$$G_{vi} = \frac{1}{sC_{ac}}$$

(4.3)

However, a proportional gain at 60 Hz doesn’t suffice to provide high gain, and hence a steady-state error remains. Although increasing the gain can achieve high gain at 60 Hz, it would decrease the phase margin resulting in a stability issue because of the delay. In addition, it needs an extra sensor, which adds to the hardware cost. In order to achieve a high loop-gain at 60 Hz, a PR regulator in both current and voltage loops has been proposed, as shown in Figure 4.4 [32-34].
The basic principle of the PR regulator is from the idea of the PI featuring infinite gain at the dc component. The basic form of the PR is shown below

\[
\{ P + R \} = C_{PR} = k_p + k_i \frac{2s}{s^2 + \omega^2}
\]

By implementing a resonant pole at fundamental frequency, an infinite gain is achieved at the fundamental frequency, thus providing zero steady-state error ac voltage control.

The above two control schemes, namely the load-current feedback and the PR regulator, can be combined in one controller. As shown in Figure 4.5, in order to investigate the PR plus load-current feedback control, a model is required. In the past, however, the effect of the sensor delay and digital delay has been neglected, leading to erroneous conclusions, as simply derived in (4.3).
Figure 4.6 shows the real outer voltage-loop diagram for a full model, and the transfer function has the following form,

\[ G_v = K_v \frac{E}{sC + \frac{1}{Z}(1 - BE)} \]  

(4.5)

where \( B \) is the sensor loop low pass filter, \( Z \) is the load, \( E \) is the inner current closed loop, and \( K_v \) is the gain of the PR controller.

To illustrate the benefits of using PR controllers for both current and voltage loops, the bode-plot of the current loop is shown in Figure 4.7 and 4.8. We can see the different loop gain at different load conditions. From the multi-loop control structure, the outer loop would only see the closed current loop. If we look at the closed current loop, we can see the PR can alleviate the gain at 60 Hz by only 4 dB. Thus adding a PR in the current loop won’t help too much for voltage regulation. The current loop can be designed by a PID compensator.
Figure 4.8: Closed loop gain of current loop

For comparison, the plots of voltage loop with and without PR are shown below in Figure 4.9.

Figure 4.9: Outer voltage loop of load current feedback with/without resonant controller

These plots show that a PR controller is not critical for the current loop, since the improvement of the loop gain at 60Hz in the current loop is much less than that of the voltage loop. Hence, the load current feedback plus PR control structure can be simplified to the structure shown in Figure 4.10.
In fact, an inner multiple poles and zeros current compensator and an outer PR-plus-load current feedback voltage controller can achieve good performance for resistive and first-order linear loads. Figure 4.11 shows that the load current feedback compensates the loop gain in the low frequency range, thus not proportional to the load impedance. The low frequency gain keeps almost constant and proportional to the load impedance without load current feedback.

Figure 4.11: Voltage loop frequency response of PR plus load current feedback and PR without load current feedback

**4.2.3. Stability for high-order Load**
If there are some other types of converter such as PFC connected on the ac side, there are EMI filters combined with some wire impedance connected between inverter output and PFCs. The loads will show up as a DM filter if PFCs are not running, as shown in Figure 4.12. Under some switching frequency of PFCs, the corner frequency of the DM filter may be around 10 kHz. So, for second-order linear loads, such as a filter load (inductor and capacitor in series), the PR plus load current feedback controller structure is subject to output resonance oscillation stability problems if there is not enough damping in the system, as shown in Figure 4.13, which is from Matlab Simulink simulation, while a PR controller without load current feedback still achieves stable regulation. The simulation results are obtained under one load case (100 mΩ resistor, 20 µF capacitor, and 100 µH inductor in series).

![Figure 4.12: DM filter load for inverter](image)
We can see that due to the existence of sensor filter delay and digital delay, the load current actually doesn’t effectively decouple the load, but adding another loop makes the control system more complicated. In fact, examining Figure 4.10, we see that the control of the inductor current with load current feedback is equivalent to controlling the output capacitor current [54], as shown in Figure 4.14.

Therefore, the difference between the controllers with and without load current feedback is the capacitor current loop (4.6) and the inductor current loop (4.7).

\[
H_{OL1} = H_i \frac{L_i}{d_{ab}} H_{delay} H_{filter} 
\]  

(4.6)
\[ H_{OL2} = H_i \frac{i_L}{d_{ab}} H_{\text{delay}} H_{\text{filter}} \]  

(4.7)

in which \( H_{\text{delay}} \) denotes the digital, computational delay; \( H_i \) represents the current loop compensator; and \( H_{\text{filter}} \) is the sensor filter.

The bode plots of both loops are shown in Fig. 4.15 as the 100 mΩ, 20 µF, and 100 µH in series filter load, which reveals the unstable resonance caused by the filter load in the capacitor current loop. However, in an inductor current loop, the resonance is well damped.

The loop difference can be investigated by looking at the current transfer functions. The inductor and capacitor control-to-current transfer functions are shown in (4.8) and (4.9).

\[ H_{iL} = \frac{i_L}{d_{ab}} = \frac{1 + sZ_{ac}C_{ac}}{s^2LC_{ac}Z_{ac} + sL + Z_{ac}} \]  

(4.8)

\[ H_{iC} = \frac{i_L}{d_{ab}} = \frac{sZ_{ac}C_{ac}}{s^2LC_{ac}Z_{ac} + sL + Z_{ac}} \]  

(4.9)

These two transfer functions have the same double poles and different zeros. Implementing the filter load in (4.10) into (4.8) and (4.9), the double of inductor and capacitor current loop are shown in (4.11) and (4.12).

\[ Z_{ac} = sL_1 + \frac{1}{sC_1} \]  

(4.10)

\[ \omega_{z1} = \sqrt{\frac{C_{ac} + C_1}{C_{ac}C_1L_1}} \]  

(4.11)
The double poles of both transfer functions are shown below

\[
\omega_{p1,p2} = \sqrt{\frac{(C_{ac} + kC_i + C_i) \pm \sqrt{C_{ac}^2 + [(1 + k)C_i]^2 + 2(1 - k)C_{ac}C_i}}{2C_{ac}C_i L_i}}
\]

\[
k = \sqrt{\frac{L_i}{L}}
\]

We assume the filter inductor \( L_i \) much smaller than the boost inductor \( L \), which is the normal case. Then, (4.13) approximates to

\[
\omega_{p1,p2} = \sqrt{\frac{(C_{ac} + kC_i + C_i) \pm \sqrt{C_{ac}^2 + [(1 - k)C_i]^2 + 2(1 - k)C_{ac}C_i}}{2C_{ac}C_i L_i}}
\]

Finally (4.14) gives the results,

\[
\omega_{p1} = \sqrt{\frac{C_{ac} + C_i}{C_{ac}C_i L_i}}, \quad \omega_{p2} = \sqrt{\frac{1}{C_{ac} L}}
\]

Equation (4.15) shows that \( \omega_{p2} \) is around the line filter resonance, and \( \omega_{p1} \) is caused by the filter load. It also shows that the double zero and double pole are located at the same frequency in the inductor current loop. Thus, the resonance pole is highly damped by the zero as shown in Figure 4.16, which requires a very small damping resistor.

![Bode Diagram](image-url)

**Figure 4.16:** Double poles and zeros of inductor and capacitor current loop

Based on the above analysis, for a first-order linear or non-linear load, the PR-plus-load current feedback presents better voltage regulation performance. However for higher-order loads, feeding back the load current may introduce high-frequency oscillations under small damping conditions; in this case the PR-without-load current feedback would be a better
choice.

4.3. Synchronous D-Q Rotating Frame Controller

4.3.1. Overview

DQ transformation is introduced in a three-phase system to project the system from stationary frame to synchronous rotating frame. The three-phase state variables are first transformed into a two-phase stationary coordinate, which is called the $\alpha$-$\beta$ frame. Then the DQ transformation is applied such that all variables are on the rotating frame. The rotating frame has the same angular frequency of the fundamental frequency of the converter. It is much easier to perform analysis and design the controllers for three-phase converters in a $d$-$q$ rotating frame because all time-varying state variables of the converter become dc time-invariant; hence only one operating point needs to be defined and considered for analysis. In order to establish a rotating frame, at least two independent phases are required; thus the concept is most often applied to three-phase but not to single-phase converters due to the limitation of only one available phase in the system.

In a $d$-$q$ rotating frame, the rotating vector in $\alpha$-$\beta$ stationary frame becomes constant vector due to the rotation of the reference plane itself. Figure 4.17 shows vector representations of stationary and rotating coordinates. Notice that angle $\theta$ is defined as

$$\theta = \int_{t_0}^{t} \omega(t) \, dt + \theta_{init}$$  \hspace{1cm} (4.16)

Where $\omega$ is the angular frequency in rad/sec, $\theta_{init}$ is the initial angle of the system, and $t$ is the time. Figure 4.3 shows vector $\tilde{x}$ which is an arbitrary phase-state variable that is projected into $\alpha$-$\beta$ stationary frame. Notice that $\tilde{x}$ can be decomposed into two component vectors, $\tilde{x}_\alpha$ and $\tilde{x}_\beta$. As vector $\tilde{x}$ rotates around the center relative to $\alpha$-$\beta$ plane, its components $\tilde{x}_\alpha$ and $\tilde{x}_\beta$ change respective to $\tilde{x}_\beta$ location and magnitude. Let us assume there is a rotating $d$-$q$ coordinate that rotates with the same angular frequency and direction as $\tilde{x}$, then the position $\tilde{x}$ relative to its components, $\tilde{x}_d$ and $\tilde{x}_q$ is the same regardless of time. It is clear that the $\tilde{x}_d$ and $\tilde{x}_q$ components are simply constant over the entire period or time and only depend on the magnitude of $\tilde{x}$ not its position in the stationary frame. Simple trigonometric properties and mathematics can be used to obtain both the D and Q matrices that describe the relationship between $\alpha$-$\beta$ and $d$-$q$ are given in (4.17) and (4.18). Notice that the matrices are non-singular and orthogonal; therefore $T^T = T^{-1}$ and $T^T T^{-1} = 1$ are true [12].
\[
\begin{bmatrix}
V_D \\
V_Q
\end{bmatrix} =
\begin{bmatrix}
\cos(\omega t) & \sin(\omega t) \\
-\sin(\omega t) & \cos(\omega t)
\end{bmatrix}
\begin{bmatrix}
V_\alpha \\
V_\beta
\end{bmatrix}
\]  
(4.17)

\[
\begin{bmatrix}
V_\alpha \\
V_\beta
\end{bmatrix} =
\begin{bmatrix}
\cos(\omega t) & -\sin(\omega t) \\
\sin(\omega t) & \cos(\omega t)
\end{bmatrix}
\begin{bmatrix}
V_D \\
V_Q
\end{bmatrix}
\]  
(4.18)

Recently, a synchronous $d$-$q$ frame controller has been proposed for single-phase converters [35-41]. By generating imaginary quadrature ($\beta$) components, all of the variables, including the voltage and current references, can be transformed into the synchronous $d$-$q$ frame, as shown in Fig. 3. With this, all time varying state and control variables become dc quantities, simplifying the converter design, which can now be treated as a dc-dc converter, and zero steady-state error is easily achievable. Figure 4.18 shows a standard $d$-$q$ controller where both the current and voltage loops are transformed into the $d$-$q$ frame, while Figure 4.19 shows an alternative implementation where only the voltage-loop is transformed into this rotating frame.
4.3.2. Relationship between Stationary Frame Control and Synchronous Frame Control

The equivalence of between d-q frame and stationary frame resonant controllers in a three-phase system was presented in [53]. The same principle can be applied to single-phase control systems. As we know, the current reference comes from the voltage loop d-q controller. Based on (4.18) and Figure 4.19, the expression is obtained below in (4.19).

\[ I_d(t) = I_d(t)\cos(\omega t) - I_q(t)\sin(\omega t) \]  

(4.19)
The $d$ and $q$ channel components comes from the DQ transformation in (4.20). Therefore the $d$ and $q$ channel component is available below.

$$\begin{align*}
v_d(t) &= v_\alpha(t)\cos(\omega_0 t) + v_\beta(t)\sin(\omega_0 t) \\
v_q(t) &= -v_\alpha(t)\sin(\omega_0 t) + v_\beta(t)\cos(\omega_0 t)
\end{align*}$$

$$\begin{align*}
v_d(s) &= \frac{1}{2}[v_\alpha(s + j\omega_0) + v_\alpha(s - j\omega_0)] - \frac{j}{2}[v_\beta(s - j\omega_0) - v_\beta(s + j\omega_0)] \\
v_q(s) &= \frac{j}{2}[v_\alpha(s - j\omega_0) - v_\alpha(s + j\omega_0)] + \frac{j}{2}[v_\beta(s + j\omega_0) + v_\beta(s - j\omega_0)]
\end{align*}$$

Plugging (4.20) into (4.19) gives

$$\begin{align*}
I_d(s) &= \frac{1}{2}[v_\alpha(s + j\omega_0)H_{dq}(s + j\omega_0) + v_\alpha(s - j\omega_0)H_{dq}(s - j\omega_0)] \\
&\quad + \frac{j}{2}[v_\beta(s - j\omega_0)H_{dq}(s - j\omega_0) - v_\beta(s + j\omega_0)H_{dq}(s + j\omega_0)]
\end{align*}$$

$$\begin{align*}
I_d(s) &= \frac{H_{dq}(s + j\omega_0)}{2}\left[v_\alpha(s) - jv_\beta(s)\right] + \frac{H_{dq}(s - j\omega_0)}{2}\left[v_\alpha(s) + jv_\beta(s)\right]
\end{align*}$$

$$\begin{align*}
I_d(s) &= \left[\frac{H_{dq}(s + j\omega_0)}{2}\left[1 - j\frac{v_\beta(s)}{v_\alpha(s)}\right] + \frac{H_{dq}(s - j\omega_0)}{2}\left[1 + j\frac{v_\beta(s)}{v_\alpha(s)}\right]\right]v_\alpha(s)
\end{align*}$$

The relationship between the voltage loop and current loop component is obtained in (4.21). Based on the definition, the relationship between the stationary frame and the synchronous frame is shown in (4.22).

$$\begin{align*}
H_{ab}(s) &= \left[\frac{H_{dq}(s + j\omega_0)}{2}\left[1 - j\frac{v_\beta(s)}{v_\alpha(s)}\right] + \frac{H_{dq}(s - j\omega_0)}{2}\left[1 + j\frac{v_\beta(s)}{v_\alpha(s)}\right]\right]
\end{align*}$$
Basically, in a single-phase system, the $\beta$ component is generated in accordance with the $\alpha$ component. Hence, the $\beta$ component is not independent. The relationship between the $\alpha$ and $\beta$ component is shown below in (4.12).

\[
\begin{align*}
\begin{cases}
 v_\alpha(t) = v \cos(\omega_o t) \\
v_\beta(t) = v \sin(\omega_o t)
\end{cases}
\Rightarrow - \frac{s}{\omega_o} v_\alpha(s) = v_\beta(s)
\end{align*}
\]  

Substituting (4.12) into (4.11) gives

\[
H_{ab}(s) = \left\{ \frac{H_{dq}(s + j \omega_o)}{2} \left[ 1 - \frac{s}{\omega_o} \right] + \frac{H_{dq}(s - j \omega_o)}{2} \left[ 1 + \frac{s}{\omega_o} \right] \right\}
\]  

If the compensator in a $d$-$q$ rotating frame is standard PI: $H_{dq}(s) = k_p + \frac{k_i}{s}$, the equivalent compensator in a stationary frame is

\[
H_{ab}(s) = (k_p + \frac{k_i}{s}) \left( \frac{1 + \frac{s}{\omega_o}}{2} \right) + (k_p + \frac{k_i}{s + \omega_o}) \left( \frac{1 - \frac{s}{\omega_o}}{2} \right)
\]

\[
\Rightarrow H_{ab}(s) = k_p + \frac{1}{2} \left( \frac{s + \omega_o}{s + \omega_o} \right) + \frac{1}{2} \left( \frac{s - \omega_o}{s - \omega_o} \right)
\]

\[
\Rightarrow H_{ab}(s) = k_p + \frac{k_i(1 + \frac{s}{\omega_o})(s - j \omega_o)}{s^2 + \omega_o^2} + \frac{k_i(1 - \frac{s}{\omega_o})(s + j \omega_o)}{s^2 + \omega_o^2}
\]

\[
\Rightarrow H_{ab}(s) = k_p + k_i \frac{2s}{s^2 + \omega_o^2}
\]

It is clear that the PR controller in a stationary frame is equivalent to the PI controller in $d$-$q$ rotating frame. In the sense of mathematics, the performance of a PI compensator in rotating frame is equal to that of a PR compensator in a stationary frame. In order to make a general conclusion, we assume the PID compensator in $d$-$q$ rotating frame is

\[
H_{dq}(s) = k_p + k_i \frac{1}{s} + \frac{k_1}{s + p_1} + \frac{k_2}{s + p_2} + \cdots + \frac{k_n}{s + p_n}
\]

Equation (4.22) can be split up as

\[
H_{dq}(s) = k_p + k_i \frac{1}{s + p} + \frac{k_1}{s + p_1} + \frac{k_2}{s + p_2} + \cdots + \frac{k_n}{s + p_n}
\]

Thus, we only need to explore the term $\frac{k}{s + p}$ to see how the PR controller would be in a
stationary frame. Plugging \( \frac{k}{s+p} \) into (4.13) gives

\[
H_{ab}(s) = \left( \frac{k}{s+p+j\omega_o} \right) \frac{1+j\frac{s}{\omega_o}}{2} + \left( \frac{k}{s+p-j\omega_o} \right) \frac{1-j\frac{s}{\omega_o}}{2}
\]

\[\Leftrightarrow H_{ab}(s) = \frac{k(1+j\frac{s}{\omega_o})(s+p-j\omega_o)}{2(s+p)^2+\omega_o^2} + \frac{1}{2} \frac{k(1-j\frac{s}{\omega_o})(s+p+j\omega_o)}{2(s+p)^2+\omega_o^2}
\]

(4.28)

\[\Leftrightarrow H_{ab}(s) = \frac{s+p+s}{(s+p)^2+\omega_o^2}
\]

\[\Leftrightarrow H_{ab}(s) = k \frac{s+p}{(s+p)^2+\omega_o^2} + k \frac{s}{(s+p)^2+\omega_o^2}
\]

We can see that in a stationary frame, one pole results in two terms. Generally, the pole is placed far behind the crossover frequency to attenuate the high-frequency components. In the current loop, the crossover frequency is normally behind the fundamental frequency. The following relationship is possible:

\[ p >> \omega_o \quad (4.29) \]

Equation (4.15) can be simplified as

\[
H_{ab}(s) = k \frac{s+p}{(s+p)^2+\omega_o^2} + k \frac{s}{(s+p)^2+\omega_o^2} \approx k \frac{1}{s+p} + k \frac{s}{(s+p)^2+\omega_o^2}
\]

(4.30)

Then, we can compare two expressions shown below

\[
H_{ab}(s) = k \frac{1}{s+p} + k \frac{s}{(s+p)^2+\omega_o^2}
\]

(4.31)

If the pole is comparatively large (which represents the normal case), the two expressions are the same in the frequency domain, like those shown in Figure 4.20. Therefore, we can use

\[
H_{ab}(s) = k \frac{1}{s+p} \quad \text{instead of } H_{ab}(s) = k \frac{s+p}{(s+p)^2+\omega_o^2} + k \frac{s}{(s+p)^2+\omega_o^2}.
\]
Then the relationship of PID compensator in a stationary frame and in a rotating frame is established as shown in (4.21).

\[
H_{dq}(s) = k_p + k_i \frac{1}{s} + \frac{(s + z_1)(s + z_2)\cdots(s + z_m)}{(s + p_1)(s + p_2)\cdots(s + p_n)} (n \geq m)
\]  

\[
H_{dq}(s) = k_p + k_i \frac{2s}{s^2 + \omega_o^2} + \frac{(s + z_1)(s + z_2)\cdots(s + z_m)}{(s + p_1)(s + p_2)\cdots(s + p_n)} (n \geq m)
\]  

Thus, if the current loop PID compensator is designed in \(d-q\) rotating frame, the equivalent compensator in the stationary frame is the PR plus a PID compensator. As discussed before, it is not necessary to put the PR controller into the current loop. Thus it is not necessary to implement a PID compensator in a \(d-q\) rotating frame in the current loop. In consequence, only the outer voltage-loop implementation in the \(d-q\) frame is the best option as shown in Figure 4.19.

**4.3.3. Unbalanced d-q Frame Control**

The advantages of single-phase \(d-q\) frame controls are straightforward compared with PR-based controls, since the PI compensator is much easier to design and implement. The main drawback of this approach is the need to generate the imaginary quadrature set of variables, referred to as \(\beta\)-axis components. Several methods have been proposed to do this. One solution is simply delay the \(\alpha\)-axis component one quarter cycle phase delay to generate the \(\beta\)-axis component. This solution is easy to implement, but introduces a phase delay, resulting in bad transient dynamics. Another approach is to differentiate \(\alpha\)-axis component to build another set of axis. However, this method is very sensitive to the noise from the sensor.
loop, amplifying the noise dramatically. Some papers propose an observer to construct the β-axis component. This approach can achieve a good result, but it is very complicated to design and implement. Hence none of these approaches represents a simple solution.

Looking back to Figure 4.17, we can see that the objective is to control α-axis component. The reason for the β-axis component is to generate a rotating vector and transfer it into a d-q frame. Alternatively, an equivalent possibility of generating two rotating vectors to eliminate the β-axis component is shown in Figure 4.21. Two rotating vectors with the half-norm of the single vector in Fig. 4 are generated in mirror with the α-axis. Therefore, the α-axis component projected by these two vectors is the same as that in Figure 4.17, but β-axis component is always zero. This means the effort to generate the β-axis component is omitted. When transferring these two vectors into the d-q frame, two frequency components show up; the dc component from the vector with the same rotating direction as d-q frame, and the $2\omega$ component from the vector with the opposite rotating direction as d-q frame.

![Figure 4.21: Stationary and rotating frame](image)

By forcing the β-axis components zero, the reference and actual voltage in d-q channels are shown in (4.33) and (4.34).

$$
\begin{bmatrix}
V_{D_{\text{ref}}} \\
V_{Q_{\text{ref}}}
\end{bmatrix}
= T \cdot \begin{bmatrix}
V \cos(\omega t + \phi) \\
0
\end{bmatrix}
= 0.5V \begin{bmatrix}
\cos \phi \\
\sin \phi
\end{bmatrix}
+ 0.5V \begin{bmatrix}
\sin(2\omega t + \phi) \\
\cos(2\omega t + \phi)
\end{bmatrix}
$$

(4.33)

$$
\begin{bmatrix}
V_d \\
V_q
\end{bmatrix}
= T \cdot \begin{bmatrix}
V \cos(\omega t + \phi)
\end{bmatrix}
= 0.5V \begin{bmatrix}
\cos(\omega t - \omega t + \phi_i) \\
\sin(\omega t - \omega t + \phi_i)
\end{bmatrix}
+ 0.5V \begin{bmatrix}
\sin(\omega t + \omega t + \phi) \\
\cos(\omega t + \omega t + \phi)
\end{bmatrix}
$$

(4.34)

Therefore the error in the d-q channels is

$$
\begin{bmatrix}
v_{D_{\text{error}}} \\
v_{Q_{\text{error}}}
\end{bmatrix}
= \begin{bmatrix}
0.5V \cos(\omega t - \omega t + \phi_i) - 0.5V \cos \phi \\
0.5V \sin(\omega t - \omega t + \phi_i) - 0.5V \sin \phi
\end{bmatrix}
+ \begin{bmatrix}
0.5V \sin(\omega t + \omega t + \phi) - 0.5V \sin(2\omega t + \phi) \\
0.5V \cos(\omega t + \omega t + \phi) - 0.5V \cos(2\omega t + \phi)
\end{bmatrix}
$$

(4.35)

Applying the PI compensator will eliminate the dc error, so
\[
\begin{align*}
0.5V_1 \cos(\omega t - \omega_1 t + \phi_1) - 0.5V \cos \phi &= 0 \\
0.5V_1 \sin(\omega t - \omega_1 t + \phi_1) - 0.5V \sin \phi &= 0 \\
\Rightarrow \quad \omega_1 &= \omega \\
\phi_1 &= \phi \\
V_i &= V
\end{align*}
\]

(4.36)

As soon as the dc error goes to zero, the \(2\omega\) frequency oscillation error automatically goes to zero.

\[
\begin{align*}
0.5V \sin(2\omega t + \phi) - 0.5V \sin(\omega t + \omega_1 t + \phi_1) &= 0 \\
0.5V \cos(2\omega t + \phi) - 0.5V \cos(\omega t + \omega_1 t + \phi_1) &= 0
\end{align*}
\]

(4.37)

Hence, in the mathematical sense, this control approach achieves zero steady-state error voltage regulation without generating the \(\beta\)-axis component. Actually, forcing \(v_\beta = 0\), and using a PI compensator in (4.22) yields

\[
H_{ab}(s) = k_p + k_i \frac{s}{s^2 + \omega_0^2}
\]

(4.38)

The above \(d-q\) frame controller does not need the generation of imaginary components and is still equivalent to a PR regulator in the stationary frame, thus it eliminates all the drawbacks of using the synchronous \(d-q\) frame approach. Further, this means that a simple PI controller can be used to achieve zero steady-state error. This implementation with \(v_\beta = 0\) can be referred then as an unbalanced \(d-q\) frame controller. Finally, the proposed control structure for single-phase PWM inverters is shown in Figure 4.22-23, where Figure 4.22 shows the cascaded current voltage loops implementation and Figure 4.23 the same scheme with the addition of the load-current feedback term.

![Figure 4.22: Unbalanced-DQ control without load current feedback](image-url)
4.4. Digital Control Implementation

According to the above discussion, PR is mathematically equivalent to single-phase \( d-q \) frame PI control. However, since it has a different form of compensator, the digital implementation would be different, which would affect the real control performance.

4.4.1. Single-phase frame PI control

The form of the PI and the digital form are shown below.

\[
C_{pi} = k_p + k_i \frac{1}{s} \tag{4.39}
\]

\[
C_{pi,d} = k_p + k_i(1 - z^{-1}) \tag{4.40}
\]

It has been shown that the digital form of PI is simple and easy to implement. Even if the DSP has a round-off/rounding error, it still achieves infinite gain at the dc component. The performance of digital control would be very close to ideal PI control.

4.4.2. PR control

The form of PR control is shown below.

\[
C_{pr} = k_p + 2k_i \frac{s}{s^2 + \omega_o^2} \tag{4.41}
\]

Before investigating the digital form, it is better to go over the general form of PR shown below.

\[
C_{pr} = k_p + k_i \frac{s}{(\frac{s}{\omega_o})^2 + k \frac{s}{\omega_o} + 1} \tag{4.42}
\]

The implementation of \( P \) and \( R \) can be done separately due to the linearity. Hence, it is useful to check the digital form of \( R \).

By implementing the bi-linear (Tustin) transformation in (4.32), the digital form would be
We see that by implementing the ideal \( R \) in (4.44), only the term \( b_2 \) has an implementation error. We may assume the error is equivalently from the denominator of \( b_2 \); then we have

\[
\Delta = \frac{m\Delta n}{n^2} = \frac{m\Delta n}{n(n + \Delta n)} \approx \frac{m\Delta n}{n^2}
\]  

(4.46)

Assuming the error from denominator is \( \Delta \) when implementing the digital form

\[
\Delta P_1 = \frac{m\Delta n}{n^2} = \frac{m}{n^2} (4\pi^2 + \Delta - 4\pi^2) \left( \frac{T_s}{T_f} \right)^2 = \frac{m}{n^2} \left( \frac{T_s}{T_f} \right)^2 \Delta
\]  

(4.47)

The error of implementing ideal \( R \) can be regarded as implementing digital form of (4.42) with a specific \( k \). So, the error would be from the parameter of \( k \)

\[
\Delta P_2 = \frac{m\Delta n}{n^2} = \frac{m}{n^2} \left( 4 + \frac{2k\omega_o T_s + \omega_o^2 T_s^2 - 4 + \omega_o^2 T_s^2}{4 + 2k\omega_o T_s + \omega_o^2 T_s^2} \right) = \frac{m}{n^2} 2k\omega_o T_s
\]  

(4.48)

Making (4.48) equal to (4.47) leads to

\[
k \propto \frac{T_s}{T_f} \Delta
\]  

(4.49)

Therefore, when we implement the digital form of ideal resonant controller, a small error results from the fact that we implement a general form of resonant controller with \( k \), which is proportional to \( T_s \) and inversely-proportional to \( T_f \). However, the gain at resonant frequency is highly related to parameter \( k \). As shown below, a smaller \( k \) can degrade the gain dramatically.
Figure 4.24: Relationship between gain and k

Therefore, although the PR can achieve the same performance as a single-phase $d$-$q$ frame PI controller, implementation error can result in a big impact to the real performance. The steady-state error would be bigger with bigger error.

All of the control schemes discussed so far can be summarized below.

<table>
<thead>
<tr>
<th></th>
<th>Transition response</th>
<th>Zero steady-state error</th>
<th>Load immunity</th>
<th>Load stability</th>
<th>Extra Hardware cost</th>
</tr>
</thead>
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<tr>
<td>Normal PID</td>
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<td>√</td>
<td>√</td>
<td></td>
<td>none</td>
</tr>
<tr>
<td>Load current feedback</td>
<td></td>
<td></td>
<td></td>
<td>High-order Load stability issue</td>
<td>current sensor</td>
</tr>
<tr>
<td>PR</td>
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<td>√</td>
<td>√</td>
<td></td>
<td>observer</td>
</tr>
<tr>
<td>PR + Load current feedback</td>
<td></td>
<td></td>
<td></td>
<td>High-order Load stability issue</td>
<td>current sensor</td>
</tr>
<tr>
<td>Capacitive current loop</td>
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<td>√</td>
<td>√</td>
<td></td>
<td>none</td>
</tr>
<tr>
<td>Standard single-phase DQ</td>
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<td>√</td>
<td></td>
<td>none</td>
</tr>
<tr>
<td>Single-phase DQ</td>
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<td>√</td>
<td>√</td>
<td></td>
<td>none</td>
</tr>
<tr>
<td>Single-phase DQ + load current feedback</td>
<td></td>
<td></td>
<td></td>
<td>High-order Load stability issue</td>
<td>current sensor</td>
</tr>
</tbody>
</table>
4.5. Experimental Evaluation

The PR, normal PID and unbalanced d-q frame control are evaluated using a 7 kW modified single-phase converter. The dc-link is connected with a constant dc source with 300 V. All control schemes are tested under no load, 1 kW resistive load, 1 kVar capacitive load, and 1 kW non-linear loads, and the results are plotted in Figure 4.25 to 4.36. The green waveform is the controlled ac voltage, and the blue color is the load current. The brown color is the voltage error. From the experimental results, the unbalanced d-q frame control presents the best steady-state performance. The PR control performance is limited by the digital implementation. The PID reveals the comparatively large steady-state voltage error.

4.5.1. Control Verification under No Load Condition

The three control methods are first tested under no load condition. All controllers present the stable performance. But the normal PID control shows the big voltage error compared with another two. Altogether, the voltage errors are not big.

Figure 4.25: Proposed single-phase d-q control at no load condition
4.5.2. Control Verification under 1 kW Load Condition

The three control methods are then conducted under 1 kW resistive load condition. Still, normal PID control shows the biggest voltage error. Also, the PR control shows some voltage error as well. Only single-phase \( d-q \) control presents the best result with much small voltage error.
Figure 4.28: Proposed single-phase $d$-$q$ control at 1 kW resistive load condition

Figure 4.29: Normal PID control at 1 kW resistive load condition
4.5.3. Control Verification under 1 kVar Load Condition

The three control methods are also done under 1 kVar capacitive load condition. Since there is the current phase shift, the control output should not be as good as pure resistive loads. The single-phase $d$-$q$ control still shows the best results.
4.5.4. Control Verification under nonlinear Load Condition

Finally, the three control methods are then verified under nonlinear load condition. Actually, the load is just the grid side transformer. Because of the saturation reason, the transformer presents the non-linear quality. Also there is the phase shift between current and voltage. Still, normal PID control shows the biggest voltage error. But the performance of single-phase d-q control drops down dramatically.
Figure 4.34: Proposed single-phase $d$-$q$ control at non-linear load condition

Figure 4.35: Normal PID control at non-linear load condition

Figure 4.36: PR control at non-linear load condition
The steady-state voltage errors of different controller under different loads are shown below in Table 4.2.

Table 4.2: Steady-state voltage error

<table>
<thead>
<tr>
<th></th>
<th>No load</th>
<th>1kW resistive load</th>
<th>1 kVar capacitive load</th>
<th>Non-linear load</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PID</strong></td>
<td>5 $V_{pk-pk}$</td>
<td>7.5 $V_{pk-pk}$</td>
<td>7 $V_{pk-pk}$</td>
<td>12 $V_{pk-pk}$</td>
</tr>
<tr>
<td><strong>PR</strong></td>
<td>1.5 $V_{pk-pk}$</td>
<td>4 $V_{pk-pk}$</td>
<td>3.5 $V_{pk-pk}$</td>
<td>5.5 $V_{pk-pk}$</td>
</tr>
<tr>
<td><strong>Single-phase d-q</strong></td>
<td>1 $V_{pk-pk}$</td>
<td>1 $V_{pk-pk}$</td>
<td>1 $V_{pk-pk}$</td>
<td>4 $V_{pk-pk}$</td>
</tr>
</tbody>
</table>

Actually we can see, although the PR control is equivalent to the single-phase $d$-$q$ control, the PR shows different performance with single-phase $d$-$q$ control just because of the digital implementation error. Single-phase $d$-$q$ control presents the best results compared with others, but the trade-off is the silicon cost for achieving the controller will be higher than others.
Chapter 5. SYSTEM LEVEL OPERATION

5.1. Single-Phase PLL

A critical aspect for all the modes of operation is the phase-lock-loop (PLL) system. In grid-tied mode, this component synchronizes the control system to the grid voltage which takes the AC voltage measurement from the VSC’s output and generates an estimate of the system frequency, $\omega_{\text{est}}$, and phase angle, $\theta_{\text{est}}$. As such, $\theta_{\text{est}}$ tracks the input angle, $\theta_{\text{in}}$. Depending on the type of PLL implemented, more information about the ac voltage can also be discerned from the PLL, such as the peak magnitude and RMS values.

![Figure 5.1: Basic PLL functional structure](image)

A PLL is composed of three basic elements, seen in Figure 5.1: the phase detector (PD), the loop filter (LF), and the voltage controlled oscillator (VCO). In the case of a digital implementation, the VCO becomes a digitally controller oscillator (DCO) and is a simple mathematical expression in the controller’s code [11].

5.1.1. Stationary Frame PLL and d-q based PLL

Sinusoidal-based PDs are essentially signal multipliers, and are popular in 1Φ systems. These PDs generate an error signal based upon the trigonometric relationship between the product of the system measurement and the output sinusoid of the DCO. This produces a signal for the LF to regulate; however, steady-state errors occur in this method [55, 56], thus causing the system frequency to have harmonic oscillations around the fundamental frequency. The multiplier function of the PD naturally generates a $2\omega$ ripple, seen in the second term of (4.1) as the PLL tracks and synchronizes with the input signal [11].

$$\sin(\omega_{\text{in}} t) \cos(\omega_{\text{ext}} t) = \frac{1}{2} \sin((\omega_{\text{in}} - \omega_{\text{ext}}) t) + \frac{1}{2} \sin((\omega_{\text{in}} + \omega_{\text{ext}}) t) \quad (5.1)$$

As the system reaches steady-state, $\omega_{\text{ext}}$, tracks and synchronizes with $\omega_{\text{in}}$, and the second term of (4.1), reaches $2\omega_{\text{in}}$. The size of the ripple depends upon two quantities, the bandwidth of the LF, and the input signal amplitude mismatch [57]. The first is easy to understand, in that the lower the bandwidth, the more attenuation there is at higher frequencies, but the relationship to the input signal amplitude mismatch is not as straightforward. The other notable feature is that though the ripple is reduced by lowering the bandwidth, there is a loss of phase-margin (PM) which translates into increased settling times.
For this type of PD, the input signal should ideally be at unity gain, thereby producing the trigonometric identity in (5.1). However, to achieve this, the ac voltage must be divided by the peak value, which in real systems is constantly changing around the nominal value. As such, the error voltage amplitude mismatch, \( A \) (which is also the unit value of the voltage), can be included in the equations, and thus this phenomenon can be quantified. For completeness, the equations show for when the grid and PLL are not synchronized, and a phase difference error term, \( \psi \), is present; seen in (5.2).

\[
V_{err} = A \sin(\theta + \psi) \cos(\theta) = \frac{1}{2} A \sin(2\theta + \psi) + \frac{1}{2} \sin(\psi)
\]  

(5.2)

It is seen that a DC term due to \( \psi \) is now present, and as the PLL synchronizes with the grid, this term goes to zero, and the error voltage is again left with a 2\( \omega \) ripple term; though now the effect of the amplitude mismatch on the ripple is clear.

To account for this double frequency term at steady-state, it is common to add an additional LPF before the LF for suppression of this added noise signal. The biggest side-effect is that the phase margin of the loop is reduced, increasing the tracking time and lowering the dynamics response.

Some papers [57-59] propose different types of single-phase PLL to address the problem. One type of single-phase PLL [57], as shown in Figure 5.2 is made by adding an additional trigonometric term loop to cancel the 2\( \omega \) ripple. This greatly reduces the steady-state error oscillation, but it cannot resolve the voltage amplitude mismatch. Another approach [57, 60] seen in Figure 5.3, is to introduce the \( d-q \) transformation in the PLL loop. This has the ability to detect the grid voltage amplitude, but it has an additional block to generate the \( \beta \)-axis component.

5.1.2. Unbalanced \( d-q \) based PLL
Using the same method of enforcing the $\beta$-axis component zero, the proposed $d$-$q$-based PLL system is shown in Figure 5.4. Accordingly, only the $d$-axis information is required, and $v_\beta$ is defined as zero to ensure a zero steady-state error for the grid phase angle tracking. The input reference signal is the grid voltage with phase angle $\theta$, and the output signal $\theta_1$, is later fed back to the $d$-$q$ transformation block.

![Figure 5.4: Unbalanced-DQ PLL Diagram](image)

Mirroring the controller case, the $d$-$q$ channel also has a $2\omega$ oscillating term. A low-pass filter can be used to filter this component and still detect the grid peak voltage as shown below.

$$V_{pk} = \sqrt{(2V_{d_{LPF}})^2 + (2V_{q_{LPF}})^2}$$  \hspace{1cm} (5.3)

This filter does not introduce any delays for the dc component, so the detected peak voltage is in phase with the grid voltage. Based on this, the PD output $V_{err}$ is given by

$$V_{err} = \frac{1}{2} \frac{V_{grid}}{V_{pk}} \sin(\theta - \theta_1) + \sqrt{\left(\frac{V_{grid}}{V_{pk}}\right)^2 + 1 - 2 \frac{V_{grid}}{V_{pk}} \cos(\theta - \theta_1) \cdot \sin(2\theta_1 + \phi)}$$  \hspace{1cm} (5.4)

$$\phi = \tan^{-1} \frac{A \sin(\theta - \theta_1)}{A \cos(\theta - \theta_1) - 1}$$  \hspace{1cm} (5.5)

A PI can then be used to eliminate the dc error, which in turn will force the $2\omega$ component error to zero when $V_{grid}/V_{pk}$ approaches unity, achieving the coveted zero steady-state error.

It is seen that as soon as the PLL synchronizes with the grid, the first term goes to zero, as well as the second term. This eliminates the $2\omega$ oscillation ripple automatically, thus achieving the zero steady-state error.

The simulation step response of the proposed PLL is shown below.

### 5.1.3. Simulation and Experimental Evaluation

A simulation is done performed using Matlab Simulink package, and the experiment is
carried out on the single-phase converter.

Figure 5.5: Frequency 2Hz step response

Figure 5.6: phase 30 degree step response

The proposed PLL addresses the voltage magnitude mismatch problem and eliminates the $2\omega$ oscillation steady-state error. It applies the $d$-$q$ transformation technique but omits the effort to generate the beta axis component. In the figures below, the brown color is the stationary frame PLL, and the green color is the proposed $d$-$q$ frame PLL.

Figure 5.7: Experimental evaluation of PLL operating at 60 Hz grid voltage: 2 Hz step PLL transient response (0.5 Hz/DIV)
Figure 5.8: Experimental evaluation of PLL operating at 60 Hz grid voltage: 290 degree step transient response (0.5 Hz/DIV)

5.2. Modes transition

The procedure for mode transition is shown in Figure 5.8. It can be seen that the grid-tied inverter mode is the base transfer state. Between any two modes of transfer, the system should first change to the grid-tied inverter mode to ensure a truly seamless transition, since the grid-tied inverter mode is the shared inner current loop common to all modes.

Figure 5.9: Procedure for transition between different modes

The modes transition procedure can be divided by two parts. One is the modes transition...
between different grid-connected modes. Another one is the modes transition between grid-tied modes and stand-alone mode. The MatLab Simulink simulation of the modes transition between different grid-tied modes is done and shown below in Figure 5.10 to 5.12. Green color waveform is grid voltage, and the blue color waveform is ac current.

The simulation verified the modes transition from grid-tied rectifier mode to grid-tied charger/discharger mode. The input grid rms voltage is 120V, and the dc-link voltage is regulated at 300V. Charging dc current is set at 37A. Figure 5.10 shows the simulation configuration; and Figure 5.11 shows the ac voltage $V_{ac}$ and current $I_{ac}$ waveform during the whole transition period. Figure 5.12 shows the mode transition from grid-tied rectifier mode to grid-tied inverter mode occurred at 0.2 s. Figure 5.13 shows the mode transition from grid-tied inverter mode to the grid-tied charger/discharger mode occurred at 0.25 s. The simulation results show the seamless modes transition due to the generic current loop.

![Figure 5.10: Simulation setup for modes transition](image)

![Figure 5.11: Modes transition from grid-tied rectifier mode to grid-tied charger/discharger mode](image)
Figure 5.12: Transition from grid-tied rectifier mode to grid-tied inverter mode at 0.202s

Figure 5.13: Transition from grid-tied inverter mode to grid-tied rectifier mode at 0.248s
Chapter 6. CONCLUSION AND FUTURE WORK

6.1. Conclusion

This thesis has presented the modeling methodology for single-phase full-bridge topology by applying small signal modeling, quasi-static modeling method. The complete control design procedure is given under different modes of operation for the single-phase energy systems application. The modeling and control design are verified by the experimental results under 7 kW power level tests, which presents comparatively good steady-state results as well as fast dynamics under load step change. This design procedure can be used for other single-phase application.

The stand-alone voltage mode control is further investigated. The objective is to achieve zero steady-state error voltage regulation with a fast transient response under large load variations. Two types of control are investigated, which are the stationary frame control and the synchronous frame control. In stationary frame control, the load current feedback, capacitive current loop, and PR control are studied for different types of load. Finally, the work shows that load current feedback plus PR control presents good steady-state performance as well as faster transient response. However, the tradeoff is this control may have stability issues under some high-order loads. Also, with synchronous frame control, the single-phase \(d-q\) rotating frame control presents zero steady-state error voltage regulation, but it takes much effort to generate \(\beta\)-axis component. The unbalanced \(d-q\) frame control can be applied to take over the standard \(d-q\) frame control with the same performance. It is demonstrated that the PR controller in stationary frame control is equivalent to PI controller in synchronous frame control. Experiments show that the single-phase \(d-q\) control improves averagely 70% of the steady-state performance compared with normal PID control under no load, 1kW resistive load, 1 kVar capacitive load, and non-linear load condition.

In the last part of this investigation, the single-phase phase-lock-loop (PLL) is analyzed, and the drawback of the traditional method is shown with the steady-state error. Some modified PLL is studied and compared. Then, a new type of PLL based on the unbalanced \(d-q\) frame control is presented, which provides zero steady-state regulation performance.

6.2. Future work

The modes transition procedure is proposed and some of the modes transition are simulated in the end. However, the experiment is not done to verify the method. Also, the procedure is valid only when the ac current is sinusoidal and in phase with the ac voltage both under grid-tied mode and stand-alone mode. If the load is a non-linear load at stand-alone mode and the current is not sinusoidal, some transient problems occur during the transition between stand-alone mode and grid-tied mode. The modes transition can be studied further.

Secondly, when doing the small-signal modeling for grid-tied modes, the grid is considered a strong source, and the dynamics of the grid are ignored. However, in many cases, the grid is a weak grid, and the dynamics will affect the control performance as well. This can
be the future work on modeling.

Thirdly, the islanding detection and resynchronization method is not discussed in this thesis, which would be a good research topic for the future.

In addition, paralleling the single-phase converter is a good way to improve the power rating and system reliability. Further work can be done to explore how paralleling control can be utilized with the previous method.

Last but not least, rotating vector control in three-phase systems introduces the space vector modulation (SVM). So, the SVM concept might be applicable to single-phase case, since we also have a similar rotating vector control. The difference is that SVM has six regions for the three-phase case, while it only has two regions in single-phase case. As such, we have similar zero, positive and negative vectors, which can be arranged to have different modulation scheme. Actually, unipolar modulation is one of the single-phase SVM schemes. So, the “single-phase SVM” can be probably studied to achieve different objectives, such as zero circulating current limiting when performing paralleling.
APPENDIX A HARDWARE IMPLEMENTATION

This section describes the hardware implementation of the proposed system. The hardware includes the power stage circuit, digital controller board, signal-conditioning and A/D sensing board, and the interface and hardware protection board.

Universal Controller and A/D Conversion Boards

Universal Controller

The digital controller board selected for the prototype is a universal Controller (UC), which is introduced briefly in this section. UC is a topology-free controller board which can implement high-level control for a wide range of power electronic converters and systems using both medium and high power. Figure A.1 shows the UC board including its Xilinx FPGA, Sharc DSP, and its communication ports such as I/O pins and fiber optic receiver/transmitters. The I/O pins are utilized to communicate with the A/Ds on the signal conditioning and sensing board and receive the digital sampled signals. They are also used to configure the A/D’s input pins for proper operation [61].

A/D Conversion Board

The A/D conversion board includes the sensing circuit, the signal conditioning circuit,
and the A/D conversion circuits as well as the over-limit protection circuit. Figure A.2 shows the board.

![A/D board, photo by author](image)

There are two AD7864 AD converters on the board. The AD7864 is a high-speed, low-power, 4-channel simultaneous-sampling 12-bit A/D converter that operates from a single 5V supply [62]. The board contains a 1.65us successive approximation ADC, four track/hold amplifiers, a 2.5V reference, an on-chip clock oscillator, signal conditioning circuitry, and a high speed parallel interface. The input signals on the four channels are sampled simultaneously, thus preserving the relative phase information of the signals on the four analog inputs. The part accepts analog input ranges of +/- 10 V. The time sequence of the signal conversion is shown in Figure A.3.
Before going to the AD7864, the input digital signal first goes through the low pass filter to attenuate the high frequency noise picked up through the environment. The design of the corner frequency of the low pass filter should consider the impact to the controller, since it would introduce phase lag into the data. Additionally, the corner frequency should be much higher than the control bandwidth and should achieve good noise attenuation. The designed corner frequency is 7.3 kHz. The filter configuration is selected as a Sallen-Key active low-pass filter as shown in Figure A.4.

![Sallen-Key low-pass filter configuration](image)

The corner frequency of this type of filter is

$$f = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

(7.1)

The values of the parameters are listed below.

$$\begin{align*}
R_1 &= 48.7 \text{k}\Omega \\
R_2 &= 48.7 \text{k}\Omega \\
C_1 &= 560 \text{ pF} \\
C_2 &= 560 \text{ pF}
\end{align*}$$

(7.2)

**TBWOODS OVERVIEW**

Instead of designing the power stage, we bought a commercial converter and modified it for our application. We finally choose a TBWood three-phase motor drive as our prototype.
power stage. TBWoods is affiliated with Vacon Holdings, Inc., which produces highly reliable high-power density motor drives.

**Functional Description of Drive system**

The motor drive we used is the E-TRAC X4 AC Drive. Figure A.5 shows the exterior.

![TBwoods X4 AC Drive](image)

Figure A.5: TBwoods X4 AC Drive, photo by author

The followings are the electrical specifications of this series’ products. More details can be checked in [63]

<table>
<thead>
<tr>
<th>Table A.1: Electrical Specification of X4 2025 Drive</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
</tr>
<tr>
<td>Line frequency</td>
</tr>
<tr>
<td>Source kVA(maximum)</td>
</tr>
<tr>
<td>DC bus voltage for:</td>
</tr>
<tr>
<td>Overvoltage trip</td>
</tr>
<tr>
<td>Dynamic brake activation</td>
</tr>
<tr>
<td>Normal under-voltage (UV)</td>
</tr>
<tr>
<td>trip</td>
</tr>
<tr>
<td>Overvoltage trip</td>
</tr>
<tr>
<td>Overvoltage trip</td>
</tr>
<tr>
<td>DC bus voltage for:</td>
</tr>
<tr>
<td>Overvoltage trip</td>
</tr>
<tr>
<td>Dynamic brake activation</td>
</tr>
<tr>
<td>Normal under-voltage (UV)</td>
</tr>
<tr>
<td>trip</td>
</tr>
<tr>
<td>Control system</td>
</tr>
<tr>
<td>Control system</td>
</tr>
<tr>
<td>Output Voltage</td>
</tr>
<tr>
<td>Overload capacity</td>
</tr>
<tr>
<td>Overload capacity</td>
</tr>
<tr>
<td>Frequency range</td>
</tr>
<tr>
<td>Frequency stability</td>
</tr>
<tr>
<td>Frequency Setting</td>
</tr>
</tbody>
</table>

The power stage configuration of the TBwoods motor drive is shown below in Figure A.6
TBwoods uses the back-back topology, which consists of a front-end SCR rectifier, a dc-link capacitor, a dynamic brake and a three-phase IGBT VSI as the output. For our application, we plan to use two phase-legs of the three-phase VSI to be the single-phase full-bridge power stage.

**Hardware Functions Used From Original System**

As shown in Figure A.6, we won’t use the front-end rectifier. We will keep the dc-link capacitor and dynamic brake for our application. We will only use two of the three phase-legs of the VSI as the power stage.

**Dc-link Capacitor and Dynamic Brake**

The dc-link capacitor consists of three electrolytic capacitors in parallel whose total value is around 7.4 mF. The original function of this capacitor is to decouple the front-end rectifier and three-phase VSI for stability as well as the ride-through capability. For our application, we use it for noise decoupling in the inverter mode as well as a voltage stabilizer at rectifier and charger/discharger modes.

The dynamic brake consists of one solid-state IGBT switch and one bleeder resistor. The IGBT is controlled by a controller. The original function of the brake is to provide a current loop when the in-rush current comes from the induction motor to prevent damage to the SCR rectifier for its non-regenerative essence. For our case, we use this to discharge the dc-link capacitor when the over-voltage fault condition occurs.

**Sensing and Measurement**

The TBwoods sends back the ac current, dc-link voltage to its own controller. We continue to use the sensing signal while adding a sensor loop for the ac voltage.

The original signal-conditioning and sensing circuit on the TBwoods power stage is shown below in Figure A.7 and Figure A.8.
The basic idea of these sensing circuits is to use the resistor divider, voltage following, and comparator to scale the signal down to the required range. The equation of the sensing circuit can be derived in using (7.3) and (7.4) provided that the turn ratio of the current transducer is known.

\[
I_o = 2.5 + 12.02 \times \left( \frac{I_{in}}{2000} \right)
\]  

\[
V_o = \frac{V_{dc}}{54.98} - 2.5
\]  

**Added Hardware Functions to Original System**
If we want to use the TBwoods to meet our requirements, we need to remove its original controller and insert ours. The critical issue is the signal interface and power/ground interface. In terms of the power stage structure, we can design an interface board to hook up a universal controller to the power stage circuit board.

**Gain and Offset Scaling of Sensed Measurements**

Since the sensing signal ranges around 2.5 V, it won’t be sufficient to achieve high resolution of the A/D conversion. We would like to fully use the input range of the AD7864. This means the output of the sensing circuit should be scaled up. We use op-amps to build the scaling circuit. Figure A.9 gives the circuitry configuration.

![Scaling circuit configuration](image)

Figure A.9: Scaling circuit configuration

The expression between the input and output is

\[
V_o' = \frac{R_2}{R_1}(V_o - \frac{R_1}{R_2} \times 3.3)
\]  

(7.5)

Therefore, we can tune the resistance to obtain the desired scaling factor and dc offset.

**Hardware protection circuit implementation**

Every converter should have protection. The basic protection function is to block the four channels’ switching signals if a fault condition occurs. One way to realize this is to put the fault detection and execution function into the digital controller as software protection. This method is straightforward and simple, and doesn’t carry extra hardware cost. However, the drawback to this method is the time delay. The block signal can be carried out one switching cycle (50 μs) after the fault condition occurs. This is normally not acceptable, since the IGBT would explode if in-rush or high fault current flowed through it more than 1 μs. Hence, hardware protection is needed. The state-of-the-art technology already combines some hardware protection into the IGBT module as a whole, such as de-saturation protection. With respect to the cost cut, the IGBT module that TBWoods uses doesn’t have de-saturation protection. Hence, extra hardware protection is required to design.

The protection consists of over voltage protection and over current protection. The basic principle behind this protection scheme is that when the ac current or dc voltage reaches a pre-defined level, the protection circuit generates a fault signal to block the switching signals. We set two levels for both voltage and current. The lower level is the cutter-current and
cutter-voltage level. When the voltage and current is beyond this level, the switching signal would be blocked. But if the voltage and current drop back to the normal rated value, the fault signal would be released, which means the converter still works. The higher level is the over-current and over-voltage level. When the current and voltage reach this level, the converter would be totally shut off, waiting a manual reset and restart. The cutter level should be added using the hysteresis function, which means the voltage and current must be slightly lower than the cutter level to release the fault signal. When the dc-link voltage reaches the cutter level, the fault signal would fire the dynamic break control signal to discharge the dc-link capacitor as well as blocking switching signals. A brief protection circuit is shown below in Figure A.10.

![Protection circuit configuration](image)

Figure A.10: Protection circuit configuration

The cutter and over level is selected based on the datasheet from TBWoods drive.

<table>
<thead>
<tr>
<th>Cutter-current level</th>
<th>Cutter-voltage level</th>
<th>Over-current level</th>
<th>Over-voltage level</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 A</td>
<td>380 V</td>
<td>60 A</td>
<td>400 V</td>
</tr>
</tbody>
</table>
USB interface Board

The USB interface board is used to connect the UC to a wireless device (presently a laptop PC) to communicate with higher-level controller using wireless communication. The USB interface board is shown in Figure A.12. This board allows the UC to be connected to any USB enabled device (proper coding for each application and device connected is needed), and components such as inexpensive network wireless cards can be added in the future.
with local PC via USB interface. The PC is responsible to transmit the data and commands back and forth between TBwoods and wireless router.

Figure A.13: High-level wireless communication, photo by author

Figure A.14 shows the real battery pack. Figure A.15 shows the charging profile. Blue and red color waveforms show the dc battery voltage and corresponding charging current respectively.

Figure A.14: Battery pack, photo by author
Figure A.16 shows the DSP code flow chart to achieve the control of bi-directional PWM converter for single-phase energy systems application.

Figure A.15: Charge Profile
DSP Code Reference

```c
#include <sysreg.h>
#include <def21160.h>
#include <math.h>
#include <signal.h>
#include <stdio.h>
#include <stdlib.h>
#include <21160.h>
#include "UControl.h"
#include "Parameters.h"
#include "functions.h"
void Ramp_vref(float);
void Input_filter(void);
void Vdc_PI_Comp(void);
void Iac_PI_Comp(void);
void De_sat(void);
void Ramp_iref(void);
//void maindd(void){while(1){}};
//Parameter array that interacts with USB
extern int g_nParamArray[15];
)/(SUMMARY)Write a value to the hex display. </SUMMARY>
inline void HexWrite( const unsigned int nVal ){
    * ( volatile UINT*)(0x0A000000) = nVal;
}
UINT g_nCurrPkt1Prev;
UINT g_nNextActivation;
/// <SUMMARY>Read data from FPGA memory</SUMMARY>
/// <REMARKS>This function is used to read data from the FPGA and includes the timing
delay necessary to prevent deadlock. <REMARKS>
/// <PARAM name="nAddr">This is the address of the FPGA memory location to read.</PARAM>
#pragma pure
unsigned int FPGARead( const unsigned int nAddr ){ 
    asm("nop;");
    volatile unsigned int* pInt = (unsigned int*)(nAddr);
    unsigned int nRet = 0;
    nRet = *pInt;
    asm("nop;");
    return nRet;
}
/// <SUMMARY>Write data to the FPGA</SUMMARY>
/// <PARAM name="nAddr">Target address to write to.</PARAM>
/// <PARAM name="nVal">Value to write to the address</PARAM>
void FPGAWrite( const unsigned int nAddr, const unsigned int nVal ){ 
    asm("nop;");
    volatile unsigned int* pInt = (unsigned int*)(nAddr);
    *pInt = nVal;
    asm("nop;");
}
/// <SUMMARY>Delay process used to wait in the DSP.</SUMMARY>
/// <PARAM name="nMaxCtr">This is a counter that indicates how many wait loops should execute.</PARAM>
#pragma const
void DelayProc(const unsigned int nMaxCtr){
    unsigned int n;
    for( n = 0; n < nMaxCtr; n++ ){ 
        asm("nop;");
        asm("nop;");
        asm("nop;");
    }
}
/// <SUMMARY>Write to USB device and do not assert ackstat. </SUMMARY>
void USBSWrite( const UINT nReg, const UINT nValue, const UINT nMarker ){
    UINT nOutVal = nMarker & 0xFFFF0000;
    UINT nCmd = (nReg << 3) & 0x0F; //mask address
    nCmd = nCmd | 0x02; //write
    nOutVal = nOutVal | (nCmd << 8 );
    FPGAWrite( 0x14000000, nOutVal );
}
/// <SUMMARY>Write to USB device and assert ackstat. </SUMMARY>
void USBSWriteAS( const UINT nReg, const UINT nValue, const UINT nMarker ){
    UINT nOutVal = nMarker & 0xFFFF0000;
    UINT nCmd = (nReg << 3) & 0x0F; //mask address
    nCmd = nCmd | 0x02; //write
    nCmd = nCmd | 0x01; //Enable ACKSTAT
    nOutVal = nOutVal | (nCmd << 8 );
    nOutVal = nOutVal | (nValue & 0xFF );
    FPGAWrite( 0x14000000, nOutVal );
}
```

-95-
void USBRead( const UINT nReg, const UINT nMarker )
{
    UINT nOutVal = nMarker & 0xFFFF0000;
    const UINT nCmd = ((nReg << 3)&0xF8); //mask address
    nOutVal = nOutVal | (nCmd << 8);
    FPGAWrite(0x14000000, nOutVal);
}

void USBReadAS( const UINT nReg, const UINT nMarker )
{
    UINT nOutVal = nMarker & 0xFFFF0000;
    UINT nCmd = ((nReg << 3)&0xF8); //mask address
    nCmd |= 0x01; //Enable ACKSTAT
    nOutVal = nOutVal | (nCmd << 8);
    FPGAWrite(0x14000000, nOutVal);
}

void mainUSB(void);
void UpdateUSBParameters()
{
g_nParamArray[0]=MODE_STATUS;
g_nParamArray[1]=*(int*)(&ACTIVE_POWER);
g_nParamArray[2]=*(int*)(&REACTIVE_POWER);
g_nParamArray[3]=CHARGE_STATUS;
MODE_DEMAND=g_nParamArray[4];
P_DEMAND=*(int*)(&g_nParamArray[5]);
Q_DEMAND=*(int*)(&g_nParamArray[6]);
VOLTAGE=g_nParamArray[7];
FREQ=g_nParamArray[8];
}

int main()
{
    sysreg_bit_set(sysreg_MODE2, IRQ0E); //enable /IRQ0
    sysreg_bit_clr(sysreg_MODE1, IRPTEN);
    
    ConfigurePWM();                 //send out the first data
    //   sysreg_bit_clr(sysreg_MODE1, IRPTEN); //enable global interrupt
    while(1)
    {
        asm("nop; ");
        asm("nop; ");
        asm("nop; ");
        //USB Main function
        mainUSB();
        //maindd();
    }
}

void ConfigurePWM()
{
    *g_cpwPer = bitPer; // Switching Period expressed in clock cycles Tsw/ 12.5ns
    *g_cpwDeadtime = 100; // Deadtime expressed in clock cycles Tsw/ 12.5ns
    *g_cpwPDeletion = 0.2*bitPer; //Pulse Deletion expressed in clock cycles 0/ 12.5ns
    *g_cpwMod_SEL = 1; // when 1 Unipolar, When 0 Bipolar
    *g_cpwCurr_Dir = 0; // Current Direction used for deadtime compensation
    *reset_ff = 1; // reset D flipflop
    *reset_ff2 = 1; // reset D flipflop
    *reset_ff3 = 1; // reset D flipflop
    // *HSFan = 0; //reset HSFan
    *g_cpwDeadCom = DTC_0m0ff; //reset deadtime compensation

    // AD data read out
    void ADScale()
    {
        float UL_Temp;
        float Vdc_Temp;
        float Vac_Temp;
        float HS_Temp;

        int ADC_CHA= *reg_ADC2CHA;
        int ADC_CHB= *reg_ADC1CHB;
        int ADC_CHC= *reg_ADC2CHC;
        int ADC_CHD= *reg_ADC1CHA;

        //converting 2’s compliments to float
if(ADC_CHA >= 0x800)  
{  
IL_Temp = (-(~(ADC_CHA-1) & 0xfff)+CHC1_CHA_OFFSET)/CHC1_CHA_SCALE;  
else  
IL_Temp = (ADC_CHA+CHC1_CHA_OFFSET)/CHC1_CHA_SCALE;  
}

if(ADC_CHB >= 0x800)  
{  
Vac_Temp = (-(~(ADC_CHB-1) & 0xfff)+CHC1_CHB_OFFSET)/CHC1_CHB_SCALE;  
else  
Vac_Temp = (ADC_CHB+CHC1_CHB_OFFSET)/CHC1_CHB_SCALE;  
}

if(ADC_CHC >= 0x800)  
{  
Vdc_Temp = (-(~(ADC_CHC-1) & 0xfff)+CHC2_CHA_OFFSET)/CHC2_CHA_SCALE;  
else  
Vdc_Temp = (ADC_CHC+CHC2_CHA_OFFSET)/CHC2_CHA_SCALE;  
}

if(ADC_CHD >= 0x800)  
{  
Charge_I = (-(~(ADC_CHD-1) & 0xfff)+CHC2_CHB_OFFSET)/CHC2_CHB_SCALE;  
else  
Charge_I = (ADC_CHD+CHC2_CHB_OFFSET)/CHC2_CHB_SCALE;  
}

Il = ( IL_Temp - 0.152463 ) * 21.2;  // Setting the polarity right
Vac = ( Vac_Temp + 0.009 )   * 22.9 *(1.0);
Vdc = ( Vdc_Temp + 8.0235 )  * 27.205;
Charge_I  = Charge_I   * (1000/328.0);
}

void irq0_handler(int useless)
{
  while(*reg_ADAV==0)
  asm("nop; ");
  ADScale();
  Open_Close_Sel=0;
  if (Open_Close_Sel==1)
  Openloop();
  else if (Open_Close_Sel==0)
  {  
  Closedloop();  
  Duty = (bitPer * 0.5) + (bitPer * 0.5) * Duty_ab;  //transfer to counter number
  // Duty=0;
  }
}

if(Iac>0)               //determine current direction
{Curr_Dir=1;  
  else if(Iac<=0)
  Curr_Dir=0;
}

SwPer=bitPer;    //12.5ns * #
DeadTime=160;
Pd=100;
Mod_Sel=1;  //0=bipolar, 1=unipolar
Curr_Dir=0;..............

if(InitTime>5e-3)               // wait for 5ms
{  
if(Mod_indexopen<0.7)
  Mod_indexopen+=0.01;  //increase Modindex
  else if(Mod_indexopen>0.7)
  InitTime=6e-3;  
}

if(Iac>0)               //determine current direction
{Curr_Dir=1;
  else if(Iac<=0):
  Curr_Dir=0;
  SwPer=bitPer;    //12.5ns * #
  DeadTime=160;
Pd=100;
  Mod_Sel=1;  //0=bipolar, 1=unipolar
  Curr_Dir=0;..............
}

if(Mod_indexopen<0.7)
  Mod_indexopen+=0.01;  //increase Modindex
  else if(Mod_indexopen>0.7)
  InitTime=6e-3;

if(Iac>0)               //determine current direction
{Curr_Dir=1;
  else if(Iac<=0):
  Curr_Dir=0;
  SwPer=bitPer;    //12.5ns * #
  DeadTime=160;
Pd=100;
  Mod_Sel=1;  //0=bipolar, 1=unipolar
  Curr_Dir=0;..............
}
Update Value
void Update()
{
    *g_cpwDuty   = Duty;    //Reference waveform
    *g_cpwPer   = SwPer;    //Switching period
    *g_cpwDeadtime  = DeadTime;   //Deadtime
    *g_cpwPD   = PD;    //Pulse Deletion
    *g_cpwMod_SEL  = Mod_Sel;
    *g_cpwCurr_Dir  = Curr_Dir;
    *g_cpwDeadCom   = DTC_OnOff;
}

Protection Block
void Protection()
{
    if(abs(Iac)>=150 || Vdc>=380 )
        *relay=0; // relay_control
    else if(abs(Iac)<=130 && Vdc<=350 )
        *relay=1;
    else if((abs(Iac)>130 && abs(Iac)<150) || (Vdc>350 && Vdc<380) )
        *relay=old_relay;
    else
        *relay=1;
    old_relay=*relay; //histersis
    if(*relay==0) fault=1;
    if(*relay==1 && fault==1) count++;
    if(*relay==0 && count>0) count=0;
    while(*relay==1 && count>=50 )
    {
        ff_state=0;
        fault=0;
        count=0;
        clear=1;
    }
    for(;clear==1;count++)
    while(clear==1 && count>=3)
    {
        ff_state=1;
        count=0;
        clear=0;
    }...

void Ramp_vref(float Vlimit)
{
    if(Vmag < Vlimit-0.02)
        Vmag += 0.01;
    else if(Vmag > Vlimit+0.02)
        Vmag -= 0.01;
    else
        Vmag = Vlimit;
}

void Ramp_iref()
{
    if(Imag < 1.98)
        Imag += 0.001;
    else
        Imag = 2.0;
}

void Vdc_PI_Comp()
{
    if (GRID_MODE == 0){
        //*********************current charge/discharge controller****************
        yv_iDC[3]=yv_iDC[2];
        yv_iDC[1]=yv_iDC[0];
        yv_iDC[2]=1.4721/2*Vac_err+yv_iDC[3];
        yv_iDC[0]=yv_iDC[2]*50e-6+(1-96.3*50e-6)*yv_iDC[1];
        yv[0] = yv_iDC[0];
    }
    else if (GRID_MODE == 1){
        //**************************AC voltage inverter test*************************
        yv_inv[2]=yv_inv[1];
        yv_inv[1]=yv_inv[0];
        xv_inv[2]=xv_inv[1];
        xv_inv[1]=xv_inv[0];
    }.
\[
xv_{\text{inv}[0]} = \text{Vac}_\text{err};
\]
\[
yv_{\text{inv}[0]} = 0.1 \times (xv_{\text{inv}[0]} - 0.8201 \times xv_{\text{inv}[1]} - 0.2953 \times yv_{\text{inv}[1]}); 
\]
\[
yv[0] = yv_{\text{inv}[0]};
\]

```c
else if (GRID_MODE == 2) {
    //****************************DC voltage rectifier test***************
    yv_rec[3] = yv_rec[2];
    yv_rec[1] = yv_rec[0];
    xv_rec[1] = xv_rec[0];
    xv_rec[0] = \text{Vac}_\text{err};
    yv_rec[2] = xv_rec[0] + (13.7 \times 50 \times 10^{-6} - 1) \times xv_rec[1] - (30.5 \times 50 \times 6 - 1) \times yv_rec[3];
    yv_rec[0] = 20 \times 50 \times 6 \times yv_rec[2] + yv_rec[1];
    yv[0] = yv_rec[0];
}
```

```c
} //****************************$

```c
void PLL()
{
    Err_PLL = (\text{Vac} / \text{Vnom}) \times \cos \theta - \sin \theta \times \cos \theta;
    //\text{Vnom} = 100 \text{ Vrms}
    //\text{Vnom1} = 120 \text{ Vrms}
    \text{Int}_{\text{Vac}} = \text{Int}_{\text{Vac PLL}} + K_i \times \text{Err}_{PLL} \times \text{Period};
    \text{Pro}_{\text{Vac PLL}} = K_p \times \text{Err}_{PLL};
    \omega = \text{Int}_{\text{Vac PLL}} + \text{Pro}_{\text{PLL}} + 2\pi \times \text{linefreq};
    //equivalent if/else statements for upper and lower frequency limits on PLL
    \omega = \begin{cases} 
    \omega \leq 2\pi \times \text{flimit higher} & ? \omega = (2\pi \times \text{flimit higher}) \; \text{if} \\
    \omega \geq 2\pi \times \text{flimit lower} & ? \omega = (2\pi \times \text{flimit lower}) \; \text{if}
    \end{cases};
    \theta = \theta + \omega \times \text{Period};
    \text{if} (\theta > 2\pi) \{ 
    \theta = \theta - 2\pi; 
    \text{else if} (\theta < 0.0) \{ 
    \theta = \theta + 2\pi;
    \}
    \cos \theta = \cosf(\theta);
    \sin \theta = \sinf(\theta);
}
```

```c
} //****************************$

```c
void Iac_PI_Comp()
{
    yc[3] = yc[2];
    yc[2] = yc[1];
    yc[1] = yc[0];
    xc[3] = xc[2];
    xc[2] = xc[1];
    xc[1] = xc[0];
    xc[0] = Iac_err;
    if (Vdc > 280)
        KK = 5 \times Vdc / 440;
    else if (Vdc < 280)
        KK = 5;
    yc[0] = 0.019842 \times KK \times (xc[0] - 0.1432 \times xc[1] - 0.824845 \times xc[2] + 0.3183543 \times xc[3]) - 0.5427 \times yc[1] - 0.9599 \times yc[2] + 0.5828 \times yc[3];
    \text{if} (yc[0] > 1)
        yc[0] = 1;
    \text{if} (yc[0] < -1)
        yc[0] = -1;
    \text{Duty}_{ab} = yc[0];
}
```

```c
} //****************************$

```c
void ChargeCurrentRef()
{ 
```
if (Vdc <= 306.0) {
    I_DCref = 6.0;
    Charge_flag = 0;
}
else if ((Vdc <= 308.0) && Charge_flag == 0 && StopCharge_flag == 0) {
    I_DCref = 6.0;
}
else if (Vdc <= 312.2 && Charge_flag1 == 0 && StopCharge_flag == 0) {
    Charge_flag = 1;
    I_DCref = 3.0;
    Charge_flag1 = 0;
}
else if ((Vdc <= 314.2) && Charge_flag1 == 0 && StopCharge_flag == 0) {
    I_DCref = 3.0;
}
else if (Vdc <= 322.2 && Charge_flag2 == 0 && StopCharge_flag == 0) {
    Charge_flag1 = 1;
    I_DCref = 2.5;
    Charge_flag2 = 0;
}
else if ((Vdc <= 316.0) && Charge_flag2 == 0 && StopCharge_flag == 0) {
    I_DCref = 2.5;
}
else if (Vdc <= 317.0) {
    Charge_flag2 = 1;
    I_DCref = 1.0;
    Charge_flag3 = 0;
}
else if ((Vdc <= 326.0) && Charge_flag3 == 0 && StopCharge_flag == 0) {
    I_DCref = 1.0;
}
else if (Vdc <= 327.0 && StopCharge_flag == 0) {
    Charge_flag3 = 1;
    I_DCref = 0.3;
    StopCharge_flag = 0;
}
else if ((Vdc < 328.0) && StopCharge_flag == 0) {
    I_DCref = 0.3;
}
else if ((Vdc <= 330.0)) {
    I_DCref = 0.0;
    StopCharge_flag = 1;
}
else {
    I_DCref = 0.0;
    StopCharge_flag = 1;
}
}

void StateOfCharge() {
    // SOC 0 - 60
    if (Charge_flag == 0) {
        CHARGE_STATUS = (Vdc*9/14)/330;
    }
    // SOC 61 - 70
    else if (Charge_flag == 1) {
        CHARGE_STATUS = 71;
    }
    // SOC 71 - 80
    else if (Charge_flag1 == 1) {
        CHARGE_STATUS = 81;
    }
    // SOC 81 - 90
    else if (Charge_flag2 == 1) {
        CHARGE_STATUS = 91;
    }
    // SOC 91 - 100
    else if (Charge_flag3 == 1) {
        CHARGE_STATUS = 99;
    }
}

// closed loop controller
void Closedloop() {
    I_DCref = 2.0;  // charging current reference
    GRID_MODE = 0;  // mode
    Ramp_vref(I_DCref);
    PLL();
    Vac_err = Vmag - Charge_I;  // outer loop error
    Vdc_PI_Comp();  // outer loop compensation
    Iac_ref1 = Iac_ref * sinf(theta + pi + 0*PF_Multiplier);
    Iac_err = Iac_ref1 - Iac;  // calculate Iac error
    Iac_PI_Comp();  // current compensation
    De_sat();  // saturation
}
[8] RENEWABLES 2007 GLOBAL STATUS REPORT
[22] Ying-Yu Tzou, etc. “High-performance Programmable AC power Source with Low


Loops Using State Variable Feedback for Single-phase Converter Systems” IEEE APEC09’