5. Active Conditioning for a Distributed Power System

5.1 The Concept of the DC Bus Conditioning

5.1.1 Introduction

In the process of the system integration, the greatest concern is the dc bus stability and system interaction. To ensure system stability, criteria need to be developed, and specifications have to be given to the “box” manufacturer. The minor loop gain concept – the ratio between the output impedance and the input impedance of the cascaded module—was introduced by Middlebrook in 1975 [F1]. This is a very conservative criterion that requires a total separation between the input and output impedance at an interface, which may cause too much penalty or be too costly in the implementation. The gain margin and phase margin (GMPM) criterion was proposed by F. C. Lee et. al. It was adopted in the power system of the space station program [F2-3,F6]. This criterion allows for the overlap between the input and output impedance, but with a forbidden region for phase and gain reservation. Assumptions have to be made before taking this concept down to the individual box level, which are unknown beforehand. Even with a well-defined criterion, a field design engineer may still face too many restrictions imposed by all the specifications in the practical design. For example, to design an input filter, all the constraints of filter damping, energy consumption, noise attenuation, output impedance, and input impedance conflict with each other. In most cases, it is difficult to adjust the parameter to meet all the requirements. One natural question is whether we can shape the input impedance of a regulated power converter.

There is nothing more desirable than a load converter behaving resistively to the dc bus in a full frequency range in the small signal sense. On the other hand, the large signal input current characteristics of a power converter are equally important. The source converter expects dc current from the loads. But unfortunately, in most applications, there exists reactive and dynamic
current on the dc bus because of pulsating loads, system transients, converters plugging in and off, possible system resonance, and so on. The large signal harmonic interaction related to the unbalanced load and the small signal impedance interaction and are discussed in Chapter 4.

This chapter proposes a dc bus conditioner for a distributed power system. The system consists of a source converter, a dc bus conditioner, and load converters. The load current on the dc bus can be divided into two categories: the dc component related to the active power, and the ac components representing the reactive power. The dc component, which encompasses a large percentage of the overall system power, is assigned to the source converter. The reactive power, which may take only a fraction of the total power, is assigned separately to the dc bus conditioner. Limited by a higher power rating, the source converter’s switching frequency is relatively low. The system bandwidth can cover only the lower frequency range, whereas the bus conditioner processes less power and switches at higher frequency, and therefore has higher system bandwidth to deal with high order system dynamics and high frequency components. The dc bus conditioner contributes to the dc system in several ways. First, it shunts the large signal harmonic current from the dc bus. This is done through extra energy storage. Whenever the ripple current is needed, it will circulate through the bus conditioner, not to the bus. Second, it improves the transient dynamic response of the system because of its higher system bandwidth. Third, it helps to maintain the bus stability. The small signal analysis shows that the bus conditioner can boost the input impedance of the regulated converter in the middle frequency range where the interaction normally happens. The concept of the bus conditioner is illustrated in Figure 5.1

### 5.1.2 The Circuit Structure for DC Bus Conditioner

There are two basic circuit topologies that can be used for the dc bus conditioner. One is the capacitor energy storage type. The other is the inductor energy storage type. The capacitor energy storage bus conditioner is shown in Figure 5.2. This is a boost-buck structure with an input inductor, a PEBB module, and an energy storage capacitor. In boost-mode operation, the bottom switch and top diode of the phase-leg are activated. The storage capacitor absorbs the energy from the dc bus. In buck mode operation, the top switch and bottom diode will be activated. The energy storage capacitor releases energy back to the bus. Its purpose is to shunt the ac current into a capacitor that is not connected directly to the bus, thus isolating the dc bus.
from the ripple current contamination. The energy storage capacitor can be small, because there is no other load on it and, therefore, it tolerates a higher voltage ripple.

The bus conditioner is essentially a current controlled current source. At the critical load points, it senses the load current. A band-pass filter is used to determine the frequency range in which it should respond. The lower end of the passing band will determine the maximum energy storage, because the low frequency current usually contains higher energy. Its higher end is limited by the current loop bandwidth, or, in other words, the switching frequency. The output of the bandpass filter is used as the reference signal for the current loop. The duty cycles are generated to control the current to the opposite polarity as the ac current on the dc bus. In system transients, the dc bus conditioner responds quickly to provide the transient energy momentarily. A very slow voltage loop is used to put extra control on the duty cycles to make up the system energy loss/gain in transients. This also maintains the energy level on the capacitor in system quiescent state. Its bandwidth is low enough not to disturb the operation of the current loop at transients.

5.2 Design and Control Considerations

5.2.1 Component Selection

The selection of the components in the bus conditioner depends on the application. The essential factors are power rating and switch frequency and system bandwidth requirements. The circuit topologies can be derived based on the basic configurations. For example, the voltage on the energy storage capacitor is higher than the dc bus voltage in order to be able to transfer energy back to the dc bus. If the dc bus voltage itself is very high, three-level circuit topology can be used, as shown later in Section 5.4.

The following shows the design considerations for the capacitor type bus conditioner.

Assume the DC bus voltage is $V_{dc}$; the circulating power between the bus conditioner and the dc bus is $P_o$, and the major concerned ac current is $F_{ac}$ in Hz.

The average current of the circulating power will be:

$$I_{avg} = \frac{P_o}{V_{dc}}$$  \hspace{1cm} (5-1)
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Figure 5.1 The concept of active bus conditioner
Figure 5.2 The capacitor type conditioner and its control function blocks
This current is equivalent to a sinusoidal current $I_{ac}$:

$$I_{avg} = \frac{1}{\pi} \int_{0}^{\pi} \sqrt{2} \sin(\omega_{ac}t) d\omega_{ac} = \frac{2\sqrt{2}}{\pi} I_{ac}$$

(5-2)

The value of $I_{ac}$ can be used as the reference of the current rating of the active devices plus other factors such as current ripple. The voltage rating selection of the active device is straightforward depending on the voltage level on the energy storage capacitor. The major design consideration of the active device is the thermal management associated with high switching frequency.

First of all, the maximum power dissipation capability of the circuit depends on the heat sink selection. If the temperature difference between the case of the active device and its junction temperature is $\Delta T_{cj}$:

$$\Delta T_{cj} = T_j - T_c$$

(5-3)

The maximum allowed power loss dissipation for the active device will be:

$$P_d = \frac{\Delta T_{cj}}{R_{th_{cj}}}$$

(5-4)

where $R_{th_{cj}}$ is the thermal resistance of the active device, which is a function of the die size and the packaging technology. At the desired switching frequency of $f_s$, the total power loss of the active device will be:

$$P_d = F(f_s) = (E_{on} + E_{off})f_s + P_c$$

(5-5)

If equation (5-5), $E_{on}$ and $E_{off}$ are the turn-on and the turn-off energy of the selected device at the normal operation condition. $P_c$ is the conduction loss of the device. They can be found in the device data sheet or the real device burn test. The device selection is a trial-and-error process. The thermal resistance, turn-on and turn-off energy, and conduction loss of the selected device have to meet the equation (5-5) at a given switching frequency, input and output voltage and current and other operation conditions.

Selection of the capacitor is a trade-off of maximum allowed voltage ripple and the capacitance. The larger the capacitance, the easier the control, the less voltage ripple in the system dynamics, and of course, the higher the cost.

The total charge that is going to be pumped into the capacitor in half ac current cycle is:
The voltage variation on the capacitor with this amount of charge is:

$$\Delta V_c = \frac{Q}{C} \quad (5-7)$$

There are two major ac current components going into or out of the capacitor. One is the harmonic current frequency on the dc bus, and the other is the switching frequency. The ESR of the capacitor is chosen to be very small in all the frequency ranges in order to reduce the power loss, which is a function of the square of the RMS current.

There are also two major considerations for inductor design. One is current ripple under the given switching frequency. The other is the delay effect between the real ac current and the inductor current. Under system transients, inductor current has to provide the desired current slew rate required by the load. The ripple current as a function of the switching frequency is:

$$\Delta i_c = \frac{V_{as}D}{LF_i \omega \sqrt{2}} \% \quad (5-8)$$

In Equation (5-8), the D is the duty cycle. If the voltage on the storage capacitor is two times higher than the dc bus voltage, the steady state duty cycle will be about fifty percent.

### 5.2.2 Modeling and Control of the DC Bus Conditioner

There are three basic function blocks in the control loop, the band pass filter, the high bandwidth current loop, and the low bandwidth voltage loop. The band pass filter provides the reference signal to the current loop.

#### 5.2.2.1 Design of the Band Pass Filter

The most important design criteria of the band pass filter are the cut-off frequency and the phase delay. An ideal filter would provide unity gain and zero phase delay in its passing band and much higher attenuation at the blocking band. A very convenient way to construct a band pass filter is to use two low pass filters with one at low cut-off frequency and one at high cut-off frequency and combine them at their output. Second order filters were used:
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\[ FL_1(s) = \frac{1}{\left(\frac{s}{w_1}\right)^2 + 2\zeta \frac{s}{w_1} + 1} \]  \hspace{1cm} (5-9)

Figure 5.3 Band bass filter design
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\[ FL_2(s) = \frac{1}{(\frac{s}{w_2})^2 + \xi_2 \frac{s}{w_2} + 1} \]  
(5-10)

\[ FL(s) = FL_1(s) - FL_2(s) \]  
(5-11)

The design example is shown in Figure 5.3. FL1(s) is the low pass filter with a 10 kHz cut-off frequency. FL2(s) is the one with a 10 Hz cut-off frequency. The combined filter shows a passing band from 100 Hz up to 4 kHz. Generally, a distribution system will have a characteristic frequency on which either the oscillation is most likely to happen or the load harmonics current exists. In Chapter 3, it was shown that the inverter load might bring \(2\omega\) frequency into the system. The band pass filter is designed to pick up this characteristic frequency in the distribution system with high fidelity, and let the bus conditioner produce a counter current to balance the oscillation or the harmonic current.

5.2.2.2 Derivation of the Plant Transfer Function

The average model of the half-bridge PEBB module derived in Chapter 3 can be used directly for the bus conditioner. The dc bus conditioner operates like a single-phase power factor correction circuit in a way that the inductor current is not constant like in a dc/dc converter. The small signal analysis method used for the PFC circuit design can be applied to the bus conditioner also. The system control block diagram is shown in Figure 5.4. The transfer functions from duty cycle to inductor current and from the duty cycle to capacitor voltage can be obtained based on the averaged PEBB model.

\[ F_i(s) = \frac{\dot{I}_L}{\dot{d}} = \frac{IL (s/wz + 1)}{D \alpha s^2 + bs + 1} \]  
(5-12)

\[ F_v(s) = \frac{\dot{V}_C}{\dot{d}} = \frac{R_iIL - D\dot{V}_C}{D^2} \left( \frac{s/wz1 + 1}{as^2 + bs + 1} \right) \]  
(5-13)

In equation (5-12) and (5-13)

\[ a = \frac{LC}{D^2} \quad \text{and} \quad b = \left( \frac{R_i}{D^2} + Rc \right)C \]

The duty cycle to the inductor current transfer function has a dc gain of IL/D, a zero at very low frequency which is not a concern for the current loop that is supposed to operate at high frequency only, and double poles at the LC resonant frequency. Actually, the bus conditioner
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resembles the audio amplifier; any ac current falling in its passing band will be reproduced counter-wise. As that of the linear amplifier, the dc bus capacitor and the energy storage capacitor can be treated as a short-circuit in high frequency small signal analysis. The high frequency characteristics of $F_i(s)$ can be approximated as:

$$\frac{IL}{d} \approx \frac{V_c}{sL}$$  \hspace{1cm} (5-14)

The duty cycle to capacitor voltage has a dc gain, two zeros at very high frequency, and two system double poles. The high frequency zero is not a concern for voltage loop design, because the voltage loop operates at very low frequency. The duty cycle to inductor current transfer function is shown in Figure 5.5. The duty cycle to capacitor voltage transfer function is shown in Figure 5.6. The high frequency zero effect can be seen in the phase of diagram of the Bode plot.

### 5.2.2.3 Design of the current and voltage loop controller

In the system control block diagram in Figure 5.4, there are two paths of signal flow. One is the low frequency path, which is the voltage loop. The other is the high frequency path, which is the current loop. The system can be analyzed separately. The procedure of control design is straightforward as long as the plant transfer function becomes known. From the control diagram, the transfer function from the inductor current reference to the real inductor current can be obtained:

$$\frac{\dot{IL}}{IL_{\text{ref}}} = -\frac{F_i(s)F_m}{1+Ti} (FL_2(s) - FL_1(s))$$  \hspace{1cm} (5-15)

In equation (5-15), $Ti$ is the current loop gain. And $Ci(s)$ is the current loop compensator.

$$Ti = Gi(s)RIHe(s)Ci(s)Fm$$  \hspace{1cm} (5-16)

Figure 5.7 shows the Bode plot of the transfer function from the reference signal to the inductor current with a proportional controller. The current loop together with the band pass filter constructs a good passing band from 100 Hz to 4 kHz. Within the passing band, the bus conditioner has a unity gain and phase of 180 degrees. It will produce the counter balance current to the dc bus.
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Figure 5.4 The control block diagram of the dc bus conditioner
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Figure 5.5 The Bode plot of the duty cycle to inductor current transfer function
Figure 5.6 The Bode plot of the duty cycle to capacitor voltage transfer function
A simple integrator with a low frequency pole, which attenuates the low frequency ripple voltage on the capacitor, can be used for the voltage loop. The voltage loop has two functions. One is to maintain a certain amount of energy storage on the capacitor, and the other is to buffer the high frequency current transient into low frequency dynamics. It has a very narrow bandwidth. The voltage loop gain is plotted in Figure 5.8.

### 5.2.2.4 The Inductor Type Circuit

The inductor energy storage type circuit is shown Figure 5.9. It is a bi-directional chopper with an energy storage inductor. The inductor is pre-charged with a certain amount of energy. If the on-times of the two active switches are equal to the on-times of the diodes, there will be no effective energy transfer between the inductor and the dc bus. If the on-time of the active switch is longer than the on-time of the diodes, the energy is transferred to the inductor and vice versa. By controlling the duty cycle, the ripple current is absorbed to the inductor, not the dc bus.

The control of the inductor type circuit is similar to that of the capacitor-type circuit. It has a high bandwidth current loop to track the ac current from the load and a slow current to regulate the average current, or the energy storage, of the inductor.

The voltage rating of the semiconductor device in a capacitor-type circuit is higher than that of the inductor type. The input current of the capacitor-type circuit is continuous because there is an inductor at the input side, whereas the input current of the inductor type circuit is pulsating. It has switching frequency ripple. An input filter is desirable to smooth the ripple current, but it may bring extra phase shift and degrade the performance of the bus conditioner. Another consideration is that a capacitor may have a higher energy density at high voltage than the inductor. For a given amount of the energy $E$, the relationships between the capacitance and inductance are given by:

$$E = \frac{1}{2} CV^2 = \frac{1}{2} LI^2$$  \hspace{1cm} (5-17)

In applications where the big inductor is available, the inductor type bus conditioner can be used. One of the big advantages of the inductor type circuit is that it is able to provide very high 
$\text{di/dt}$ slew rate compared to the capacitor type circuit.
Figure 5.7 The Bode plot of the transfer function from the load ac signal to the inductor current
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Figure 5.8 Bode plot of the voltage loop gain
Figure 5.9 The inductor type dc bus conditioner with its control blocks
There are three different operational modes of the circuit: the charge mode, the discharge mode, and the freewheeling mode. In the charge mode, all the active switches are on. The dc bus voltage is applied directly to the inductor. The inductor absorbs energy from the dc bus. In discharge mode, all the active switches are off, and the inductor current discharges from the diode branches to the dc bus. It releases energy back to the bus. In freewheeling mode, only one of the active switches is on, either the top or the bottom. The current circulates inside the circuit through one active device and one diode. There are losses produced by the voltage drop of the semiconductor devices and the conductors in freewheeling mode.

The large signal average model can be derived based on the charging duty cycle as shown in Figure 5.10. The small signal characteristics of the circuit can be obtained based on the average model.

Because the current generated by the bus conditioner is pulse-width-modulated, a PWM voltage waveform will be applied to the inductor. If the inductor is not large enough, a current ripple could be excited. This will affect the input current modulation in turn. In this case the inductor current ripple effect has to be compensated on-line, which is shown in Figure 5.11. The rule for the duty cycle compensation is:

$$D_e = \frac{I_{ref}}{I_{avg} + I_{ripple}}$$

(5-18)

$D_e$ is the effective duty cycle. Using the instantaneous inductor current to compensate the duty cycle is a viable approach to use small inductor and allow relative high current ripple on the inductor.

### 5.3 The Functions of the dc Bus Conditioner

The function of the bus conditioner is demonstrated through examples as shown in the following.
Figure 5.10 The average model of the inductor type current

Figure 5.11 Compensation of the duty cycle according to the current ripple
5.3.1 Providing the Harmonic Current of the Pulsating Load

The system connection diagram is shown in Figure 5.12. An inverter load draws $2\omega$ ripple current from the dc bus. The bus conditioner is connected at the input point of the inverter. In this system, the bus conditioner provides the ac harmonic current as required by the pulsating load. As shown in the waveform, when the pulsating current is injected into the system, the dc bus conditioner produces a current with opposite direction. The bus voltage still remains regulated by the rectifier. The three-phase PWM rectifier is not affected by the pulsating load, and the three-phase input current is immune from the distortion. The energy storage capacitor takes over the pulsating current; therefore, its voltage has the ripple content.

5.3.2 Buffering the System Dynamics

It was shown in Chapter 4 that the system dynamic response can become very oscillatory when the input and output impedance of rectifier and inverter load are very close to each other. The bus conditioner now is connected on the dc bus as shown in Figure 3.39. The source converter is the three-phase rectifier with an input of 480 V, and the dc bus voltage 800 V. The load is a four-leg inverter for secondary utility power supply. When a step load is applied at the output of the four-leg inverter, there will be current step change reflected to the dc bus. With the help of the dc bus conditioner, the very fast transient current is diverted to the energy storage capacitor. Therefore, the bus voltage does not change significantly, it dips only 4.6 V compared to 48 V before. In the transient process, the capacitor is discharged. The voltage loop of the bus conditioner slowly adds control on the duty cycle and charging the energy back to the capacitor.

5.3.3 Improving the Load Input Impedance / Source Output Impedance

The impedance measurement setup diagram is shown in Figure 5.14. A small signal current perturbation is applied onto the dc bus. While the bus voltage responds to the perturbation, the current is shared among different boxes. The source output impedance and load input impedance of the boxes on the dc bus are:

$$Z_s = \frac{V_s}{i_s}$$  (5-19)
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\[ Z_L = \frac{V_L}{I_L} \quad (5-20) \]

Because the bus conditioner is a current follower, the perturbation current going into the load will be replicated in its passing band.

\[ \hat{i}_{bc} \approx -\hat{i}_L \quad (5-21) \]

The equivalent load current including the bus conditioner will be:

\[ \hat{i}_{le} = \hat{i}_s + \hat{i}_L \approx 0 \quad (5-22) \]

Therefore, the combined input impedance becomes very high.

\[ Z_{le} = \frac{\hat{V}_L}{\hat{I}_{le}} \quad (5-23) \]

As shown in Figure 5.14, the equivalent input impedance looking into the shaded box is boosted up by over 30 dB in its active region compared to the impedance without the bus conditioner. The equivalent impedance still shows the regulated converter at a very low frequency with its phase starting at minus 180 degrees. Once inside the dc bus conditioner’s active range, the phase rises rapidly to zero. Meanwhile, it successfully accomplishes a wide separation with the output impedance of the input filter.

The dc bus conditioner can be treated as part of the source from the other point of view. The equivalent source impedance can be defined as the ratio between the bus voltage and the total current of source and the dc bus conditioner:

\[ Z_s = \frac{\hat{V}_s}{\hat{I}_s} = \frac{\hat{V}_s}{\hat{i}_s + \hat{i}_w} \]

The equivalent source impedance will be reduced in the active region of the bus conditioner.

5.4 Experiments

Because the voltage of the energy storage capacitor is higher than the dc bus voltage, with a 800 V dc bus system, a three-level circuit topology is used, as shown in Figure 5.15 (a). The hardware setup is shown in Figure 5.15 (b). A preliminary experiment was carried out on the hardware. Figures 5.16 and 5.17 show the inductor current reference signal and the produced inductor current at 120 Hz and 1 kHz. The switching frequency is 40 kHz.
Figure 5.12 The bus conditioner connected with pulsating load to provide the harmonic current
Figure 5.13 System transient performance, (a) system diagram and (b) comparison of the bus voltage
Figure 5.14 The impedance improvement with the bus conditioner, (a) Measurement setup, (b) The comparison of the impedance
Figure 5.15 A three-level structure for dc bus conditioner, (a) Circuit diagram, (b) The hardware setup
Figure 5.16 The reference signal and the inductor current at 120 Hz
Figure 5.17 The reference signal and the inductor current at 1 kHz