A Power Conditioning System for Superconductive Magnetic Energy Storage based on Multi-Level Voltage Source Converter

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A new power conditioning system (PCS) for superconductive magnetic energy storage (SMES) is developed and its prototype test system is built and tested. The PCS uses IGBTs for high-speed PWM operation and has a multi-level chopper-VSC structure. The prototype test system has three-level that can handle up to 250-kVA with a 1800-V DC link, a 200-A maximum load current, and a switching frequency reaching 20-kHz with the help of zero-current-transition (ZCT) soft-switching. This PCS has a great number of advantages over conventional ones in terms of size, speed, and cost.

Conventional PCSs use thyristors, due to the power capacity of the SMES system. The speed limit of the thyristor uses a six-pulse operation that generates a high harmonic. To reduce the harmonic, multiple PCSs are connected together with phase-matching transformers that need to be precise to be effective in reducing the harmonics. So, the system becomes large and expensive. In addition, the dynamic range of the PCSs are also limited by the six-pulse operation, because it limits the useful area of the PCS applications.

By employing a high-speed PWM, the new PCS can reduce the harmonics without using the transformers reducing size and cost, and has wide dynamic range. However, the speed of a switching device is generally inversely proportional to its power handling capacity.
Therefore, employing a multi-level structure is one method of extending the power-handling capability of the high-speed device. Switching loss is another factor that limits the speed of the switch, but it can be reduced by soft-switching techniques. The 20-kHz switching frequency can be obtained with the help of the ZCT soft-switching technique, which can reduce about 90% of switching losses from the IGBT during both turn-on and turn-off transients.

There are two different topologies of the PCS; the current source converter (CSC) type and the chopper and voltage source converter (VSC) type. In terms of the SMES system efficiency, the chopper-VSC type shows a less volt-ampere requirement of the power device. Therefore, the new PCS system has a chopper-VSC structure.

Since the chopper-VSC structure consists of multiple legs that can be modularized, a power electronics building block (PEBB) leg is a good choice; all of the system problems caused by the high frequency can be solved within the PEBB leg.

The VSC is built with three of the PEBB legs. Three-phase AC is implemented with a three-level space vector modulation (SVM) that can reduce the number of switching and harmonic contents from the output current. A closed-loop control system is also implemented for the VSC, and shows 600-Hz control bandwidth.

The multi-level structure used requires too many high-speed switches. However, not all of them are used at the same time during normal multi-level operation. A new multi-level topology is suggested that requires only two high-speed switches, regardless of the number of levels. Other switches can be replaced with slow-speed switches that can allow additional cost savings.
To my mother
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Chapter 1 Introduction

1.1 Background

Ever since superconductivity was discovered in 1911, it has drawn lot of attention due to its enormous impact on human life. This attention has led to a variety of applications, and many future possibilities for utilizing superconductivity in various areas have been predicted. Since superconductivity has zero resistance, it is natural that the technology has a number of applications in the electric power area. One of the most promising applications in this area is a type of energy storage called superconducting magnetic energy storage (SMES). The SMES is an inductor that can store large amount of electric energy in the form of magnetic flux by flowing DC current through its coil without experiencing losses. The SMES can be used efficiently in various electric-power applications such as utility load leveling. The SMES system can be used as an alternative for generating electricity by storing electricity during off-peak times and sending electricity back to the utility grid during peak load times. This directly improves the efficiency of existing power plants. Similarly, the SMES system is highly also useful for utilities that lack or have weak intertie. A good example is the utility grid in Alaska, where the load changes suddenly and abruptly but is isolated from the U.S. utility grid. To make the Alaskan utility grid stable, the utility grid must have sufficient power-plant standby to prepare for load changes. This is, however, a very expensive method of solving this problem. The SMES system can be an alternative. With the SMES system, the standby power plant can rest during low loads, and the SMES can be on standby for the load changes. When the load changes, the SMES system can immediately take over the load until the power plant starts up and can take the load over. By doing this, the SMES system not only can stabilize the utility grid without having performance degrade, but also can save operating costs. Other applications of the SMES include static volt-ampere-reactive (VAR) compensators, utility uninterruptable-power-supply (UPSs), voltage sag compensators, black starters, pulse power source, etc.

After its first discovery, it was 75 years before superconductivity was taken to the next stage. In late 1986, the IBM research center at Switzerland announced a second
superconductivity known as Type II superconductivity. Type II superconductivity can sustain its properties until 77°K, the boiling point of liquid nitrogen, resulting in tremendous cost savings. Type II superconductivity was named high-temperature-superconductivity (HTS), while earlier superconductivity, known as Type I superconductivity, was named as low-temperature-superconductivity (LTS). Ironically, HTS is no longer a conductor at room temperature; rather it is an insulator. When it is cooled down below critical temperature, Tc, it suddenly turns into a superconductor. When this discovery was announced, industries around the world quickly recognized the enormous potential of this new technology. Researchers throughout the world started a challenging, high-stakes race to develop this technology.

After the initial appearance of superconductivity in 1911, the first active research into the SMES system was not initiated until the early 1970s by the Department of Energy (DoE)[A1][A2]. The result of the research led to a test of a 30-MJ SMES coil with 10-MW power converter at Bonneville Power Administration (BPA) in Takoma Washington. The SMES system was designed and tested to dampen the power oscillation of the Pacific AC Intertie [A3]. SMES, the second stage of the research, was led by the Department of Defense (DoD) starting in 1987. The DoD chose the SMES as a potential candidate for a power source to provide the pulse power required for a ground-based defense system, and initiated a program to develop this technology. The first aim of this program, called engineering test model (ETM) program, was to develop a SMES system that could provide 400-MW pulse power for 100 seconds with a rising and falling time of one second. The system must also be able to provide 50-MW utility power for two to three hours for utility load leveling. The final aim was to develop a SMES system that scales ranges from 1000-MWh to 5500-MWh with a 1000-MW discharge capability. Unfortunately, this program was terminated in 1992 because of a congressional budget-cut. Recently, a SMES program focused on commercial use was initiated to stabilize utility lines in Alaska where the intertie proves difficult. DoD has also begun a new research program that investigates the benefits of using the SMES with carrier aircraft launching.
1.2 The Power Conditioning System

The SMES is an inductor and stores energy in the form of DC current, while most electric energy source/load requires voltage source type. To store and retrieve energy to and from the SMES, the PCS should provide proper voltage across the SMES. Therefore, a power conditioning system (PCS) is indispensable for the SMES in most of its applications, and plays a key role in the overall SMES system performance. The performance of the PCS depends on various qualities such as its structure and devices. There are three different topologies available for its structure. The first topology, introduced during early stages of the SMES development, is a six-pulse current source converter (CSC) type. The PCS used for the BPA test incorporated this type of topology with SCRs. The structure of this CSC type is shown in Figure 1-1. This CSC can control power flow by changing the firing angles between two of the SCR CSCs through two of the three-phase transformers. This method, however, causes a great deal of circulating current through the transformers, therefore requiring over-sized transformers. This method also has a limited range of reactive power control due to the firing angle limitation of the SCR. Two different suggestions for improvement were made during the ETM program. The DoD assigned the development of the PCS to two major electronics companies, General Electric Corporation (GE) and Westinghouse Corporation. Each company suggested its own method of improvement. General Electric suggested a hybrid CSC topology based on the six-pulse CSC technique. Westinghouse suggested a totally new concept of DC chopper followed by VSC typology [A10]. Figure 1-2 shows the hybrid CSC type and Figure 1-3 shows the chopper and VSC type. The hybrid CSC type is an improvement over the CSC type because two of the CSCs are connected before the transformers, reducing circulating current during the free-wheeling period, therefore requiring a smaller-sized transformer. In addition, the hybrid CSC designed for the ETM program used GTOs together with the SCRs to extend the control areas of the active and reactive powers.

The chopper-VSC type PCS suggested by Westinghouse uses a different method. In this method, the chopper translates the DC current from the SMES into a voltage source that can be used as the input for the VSC. The VSC uses four of six-pulse VSCs with a phase matching transformer. The advantages of this structure over the other CSC types are
smaller volt-ampere requirement for the switching device and reduced current harmonics on the three-phase utility side.

Figure 1-1. Block diagram of a CSC-type PCS used in the BPA test

Figure 1-2. Block diagram of multiple hybrid-CSC-type PCSs
1.3 Objective

The common denominators of the three different types of the PCS are thyristors, a six-pulse operation, and matching transformers. All of these factors are closely related to each other. The thyristors are necessary due to the power requirements of the PCS. There are not many switching devices that can handle the necessary amount of power for the SMES applications except the thyristors. However, the thyristors are not easy to control due to the nature of the regenerative process. Usually they need a reverse voltage across the switch to turn off. The six-pulse operation makes use of the line frequency to turn off the thyristors. The six-pulse operation introduces the DC current of the SMES into the utility, therefore enlarging the harmonic content. To reduce the harmonics, multiple six-pulse PCSs with different firing angles and matching transformers are needed. These transformers are expensive because they need to be matched each other to prevent any increase of harmonics an unbalanced transformer can cause. In addition to the cost, the transformer increases the size of the PCS making the design of the PCS difficult due to the larger parasitic. The six-pulse operation also limits the speed of the PCS. The BPA test results show that the dynamic range of the PCS is less than one hertz.
All of the above limitations are caused by the speed of available switching devices. When the speed of the switching device is enough for PWM operation of the PCS, the six-pulse operation can be replaced with the PWM. The PWM can reduce the harmonic content of the PCS and can remove the expensive and large transformer, resulting in size reductions and lowered costs. The increased switching speed also increases the speed of the PCS. The effect of the higher-speed PSCs is an improvement of the performance of the SMES system and an extension of its application areas. Therefore, the speed of the PCS is one of the most important factors in the usefulness of the SMES system.

The objective of this research is to discover how to increase the speed of the PCS and demonstrate the resulting method through an experimental system.

1.4 Approach

As mentioned before, the speed of the PCS is a key factor in reducing the system's size and cost and in increasing the system's speed to extend the range of application of the SMES system. The speed of the PCS is determined primarily by the speed of the switching devices. In addition, the switching device should also be able to handle the required power for the SMES system. Unfortunately, the speed of a switching device is usually inversely proportional to its power-handling capability. There are not many choices of switching devices that have both the speed for the PWM and the power for the SMES. One solution to this problem is using multiple structures that can extend the power rating of the system for the available devices. By using multiple devices and/or a multiple system, the overall power capacity of the system can be expanded. To increase the power capacity through multiplication, there are four different combinations for the multiple structure: series and parallel connections of devices and systems. Among these, either a series or a parallel connection of both devices and systems only extends the voltage or the current ratings of the whole system. These are not effective ways to extend the power rating. To extend both the voltage and current ratings of the whole system, which is most desirable, the combination used has to be a series connection of the device and a parallel connection of the system, or vice versa. The series connection of the system with the parallel connection of the device requires connections of the output of each system to the utility, which requires additional parts or equipment like a
transformer. In addition, the paralleling of devices usually requires a de-rating of device capacity, and some devices do not work well in parallel. On the other hand, the parallel system with series devices requires a method of voltage-sharing between devices. This method requires a smaller amount of de-rating of the power capacity of the system and the voltage capacity of the devices. Previous research [A17] shows this aspect clearly.

Previous research also shows that a multi-level structure with an IGBT is one of the best choices for the new PCS. The issue that follows is how to integrate the IGBT into the multi-level structure to get the maximum possible speed for the SMES PCS using available technologies. The approach to this problem can be divided into three parts: the device test; the leg design and test; and the system design and test. From the first step, the device test, various data of the IGBT relating to the switching operation can be obtained. Based on these data, the maximum switching frequency can be estimated, and alternative methods for increasing the maximum switching frequency can be reviewed. The results can also be used to determine the structure of the switch arrangement and its connection. The second step is the design and testing of the multi-level leg. Design considerations will include ways to reduce switching-related loss and voltage and current spikes for all ranges of operations. The third step is the construction and testing of the overall system.

1.5 Dissertation Outline

The research into the high-speed multi-level PCS can be outlined as follows.

Chapter 2 includes reviews of the present three power conditioning system techniques: six-pulse CSC; hybrid CSC; and chopper-VSC types. It also reviews the previous research results on new type of PWM multi-level structure using high-speed switches. This chapter includes information on the expected improvement of the size, the speed, and the cost of the new PCS over the conventional PCS, device selection, topology evaluation, and the structure of the prototype system. The detailed construction and test of the prototype system are discussed from Chapter 3 to Chapter 7.

In Chapter 3, surveys for soft-switching topologies that can extend the switching frequency of the switch are covered. Tests are performed under various operating conditions, such as using different gate drive resistors and device current levels. Based on
the test results, switching losses of the device during the turn-on and turn-off transitions are estimated. The results of the device test show the maximum possible switching frequency. To improve the speed further, a soft-switching topology is selected that is suitable for the high-speed PCS. By using proper soft-switching topology, the switching frequency can be extended higher. The device test is performed again using the soft-switching technique. Comparisons for the two switching methods are made.

Chapter 4 discusses the design of a three-level leg, which is a basic element of the high-speed PCS. This leg should operate efficiently in all of the possible operational modes of the PCS. Therefore, the leg should be designed for all of its operation modes. The leg is designed with the power electronic build block (PEBB) concept that enables modularization of the system. Various aspects of design, switching characteristics, and optimization of the PEBB leg are investigated.

Chapter 5 concentrates on a three-phase multi-level voltage source converter (VSC) using three of the PEBB legs. The three phases are implemented with a space-vector modulation (SVM) to reduce switching losses and to utilize given resources fully. The VSC operation is tested with an open loop, and power stage transfer functions are measured. This chapter also includes modeling of the VSC for both inverter and rectifier modes. Compensators are designed and tested with a closed loop to demonstrate the performance of the VSC.

Chapter 6 suggests an alternative for the multi-level topology that can reduce the number of high-speed switches. The present multi-level topology requires too many high-speed switches, which make the system expensive. The number of high-speed switches can be reduced by employing more slow-speed switches. This method will result in great savings on total system costs while maintaining the speed of the PCS as fast as the conventional one.

Conclusions are given in Chapter 7.
Chapter 2  Power Conditioning System Techniques

2.1  A Review of Present Power Conditioning Systems

2.1.1  The Six-Pulse Current Source Converter

The PCS used in the BPA test had two six-pulse CSCs with SCR. The two CSCs were connected in series at the DC side and connected to the SMES coil. The two outputs of each CSC were added together through two transformers. The system was able to control active and reactive power independently by using asymmetrical firing angles. However, the performance of the PCS was not satisfactory. The range of reactive power compensation was not wide enough and only suitable for the lagging current, which is not useful for the utility. The current waveforms of the output included a great deal of harmonics due to the six-pulse operation of each CSC. The dynamic range was about 0.4 seconds [A3]. Figure 2-1 shows an example of a six-pulse CSC using SCRs. Power flow of the system is determined by the firing angle of the SCR. Due to the firing capability of the SCR, the CSC topology can only be used in an approximately 5° to 140° period.

A couple of efforts were made to improve the six-pulse CSC using various methods, including changing the switching device from the SCR to a gate-turn-off thyristor (GTO) [A4][A5][A6]. The employment of the GTO provided leading current compensation; however, it introduced a voltage spike during turn-off, due to the leakage inductance of the transformer. This situation required the use of commutation capacitors that needed to be tuned to avoid an unnecessary fifth-order harmonic resonance between the capacitor and the leakage inductance of the transformer. With the GTO, the six-pulse bridge could be operated with pulse-width-modulation (PWM), reducing the harmonics. However, the GTO with the PWM generated too high switching loss. Therefore, efforts were made to reduce the loss using soft-switching techniques [A7].

By the nature of the current source, the current $I$ shown in Figure 2-1 should be continuous. Therefore, it needs closed paths. The closed path can be established by turning on either set of the top three switches, $S_1$, $S_3$, $S_5$ and the bottom three switches, $S_2$, $S_4$, $S_6$. 

...
$S_4$, $S_6$ together. However, the switch combinations should avoid shorting the three-phase line-to-line voltages. Therefore, only one of the top and bottom switches should be turned on at any given time.

The six-pulse operation of the CSC connects the DC current source to the AC lines during 60° periods for one pulse. Since the period is fixed, the total amount of apparent power cannot be controlled. To control the power in the BPA test, two SCR CSCs connected in series were used. The control of power can be achieved by placing the CSC such that each has a different firing angles. When GTOs were used instead, control of the power could be achieved by shorting one leg of the GTO within the 60° period, resulting in less connection time between the SMES coil current and the AC lines. This method is called partial-shorting control, and requires twice as many switching losses.
Figure 2-1. An example of a six-pulse CSC and its timing for six-pulse operation and the three-phase current
2.1.2 The Hybrid Current Source Converter

The PCS proposed by General Electric in the ETM program was a hybrid CSC. The difference between the six-pulse CSC used in the BPA test and the hybrid CSC was the connection method of the CSCs. The former used a series connection at both the input and output of the two CSCs, while the latter used a parallel connection. The series connection of the output was made through the transformer, while the parallel connection could be tied together in front of the transformer. Therefore, the parallel connection method could reduce the average current through the transformer and some of harmonics produced. This could save the power capacity of the transformer. However, the parallel connection did not promise current sharing of the two CSCs. It required two current-sharing inductors at both the input terminals of the CSC to prevent the appearance of a third harmonic across the SMES.

Figure 2-2 shows the detailed structure of the hybrid CSCs; the block diagram is already shown in Figure 1-2. To handle the high power, the PCS needs multiple hybrid CSCs with SCR and GTO. The CSC with SCR is used for lagging current and that with GTO is used for leading current. Generally, the power capacity of the GTO is inferior to that of the SCR. Therefore, a combination of one SCR CSC and two GTO CSCs are desirable for one PCS module.

When a system requires more than one six-pulse CSCs, the hybrid CSC is a better choice than two of the six-pulse CSCs in terms of controlling power. Suppose that two of the six-pulse CSCs are paralleled. Each CSC needs to short one leg to control the amount of power flowing. This result in double switching losses. Instead of partial shorting control, the two hybrid CSCs can be controlled with a phase-shifted six-pulse technique. By doing this, the power can be controlled without incurring additional switching losses. When the two CSCs are switched in-phase, the two CSCs dump out their maximum power to the output. When the output power needs to be controlled, the two CSCs can be fired with different angles. With the out-of-phase firing, the current I will flow from one of the top switches at CSC₁ to the bottom switch of the same leg at CSC₂, and vice versa. The transformer CST in Figure 2-2 is the current-sharing transformer that will split the SMES coil current equally into the two CSCs.
2.1.3 The Chopper-Voltage Source Converter

The chopper-VSC topology proposed by Westinghouse was totally different from the CSC topologies. It used a two-quadrant chopper and a VSC linked with a DC voltage. The chopper changes the DC current from the SMES coil to DC voltage, and a 24-pulse VSC changes the DC voltage into a three-phase AC current. Both the chopper and VSC need GTOs. For a 24-pulse VSC, four of the six-pulse VSCs were used, and the outputs were added together through a 24-pulse transformer to be connected to the utility. Control of the real and reactive powers were accomplished by controlling firing angles of the GTOs and the DC voltage that is determined by the duty ratio of the chopper. The angle and voltage differences between the utility line and the output of the VSC built current

Figure 2-2 Structure of a hybrid CSC
through the leakage inductance of the transformer that became the utility line current.

This topology has couple of advantages over the CSC topology. Since the SMES coil current flows only through the chopper, the current stress of the VSC can be reduced to a minimum, reducing the total device power rating of the system. The harmonics generated by the voltage and the current are filtered out by the leakage inductance of the transformer. The DC voltage can serve as a buffer between the utility and the SMES coil. When the utility is disturbed, over-voltage of the utility is changed into current by the leakage inductance of the transformer and charged into the DC link through the diodes of the VSC smoothing out the transient. This provides a good isolation of the SMES coil from the utility transients. The CSC topology directly exposes the SMES coil to the utility lines.

An example of the voltage-source approach is shown in Figure 1-3. The SMES coil current, which is a stiff current source, is changed into a voltage source with numbers of two quadrant choppers. At the output of the chopper, there are bulk capacitor banks followed by a 24-pulse voltage source converter interfacing with the AC power system through transformers. The DC link capacitor serves as a stiff but controllable DC voltage source. This configuration also significantly de-couples the SMES coil from the utility system and reduces the coil's exposure to disturbances on the utility system.

### 2.1.3.1 The Chopper

The role of the DC-DC chopper is to control the energy flow through the SMES coil. When the SMES needs to be charged, the chopper connects the DC link voltage to the SMES so that the current inside the SMES increases making power flow from the DC link to the SMES coil. When the SMES needs to be discharged, the chopper connects the opposite voltage. The rate of charge/discharge is controlled by the voltage magnitude of the SMES coil. In other words, the DC-DC chopper changes the constant DC link voltage into a variable voltage required by the SMES coil to make the desired energy flow.

Figure 2-3 shows a detailed configuration of the chopper. The suggested mode of operation for a chopper is as follows. As shown in Figure 2-3, the coil can be charged
when the two GTOs are fired simultaneously and the diodes become reverse-biased. When the two GTOs are turned off, the coil discharges and the diodes become forward-biased. The voltage across the coil is regulated by controlling the conduction time of the GTO over the switching cycle. At a duty cycle of 0.5, the SMES coil's average voltage and the VSC's average DC current are both zero, and no net power is transferred throughout one switching cycle. At a duty cycle larger than 0.5, the coil is charged; while at less than 0.5, the coil is discharged. Therefore, the control of charge/discharge is accomplished by controlling the duty cycle.

Another possible way of operation, which can reduce ripple and the amount of switching is as follows. During the off-time period, when the SMES coil keeps its energy, either one of the GTOs needs to be turned on to make a short current path. When only $GTO1$ is turned on, current $I$ flows through $D1$ and $GTO1$. During this time, the capacitor bank $C$ and the SMES coil are disconnected by the $GTO2$ and $D2$. When the SMES needs to be charged, both of the GTOs need to be turned on. By doing this, the capacitor voltage is applied to the SMES coil and charges it. When the SMES needs to be discharged, both of the GTOs need to be turned off. During this time, the current flows through the diodes, charging the capacitor.

![Figure 2-3. Structure of a two-quadrant chopper](image-url)
2.1.3.2 The Voltage Source Converter

The chopper is followed by the VSC to form a complete PCS. The VSC is composed of four six-pulse modules, making a 24-pulse VSC. The four modules are connected to each other through transformers, as shown in Figure 2-4. The primaries of the transformers are connected in series and tied to the utility. By doing this, the voltage rating of the six-pulse modules becomes a quarter of the line voltage.

The four six-pulse converter bridges and transformers constitute a single 24-pulse converter. By controlling the switching time such that the four six-pulse modules are phased 15° apart, a 24-pulse AC voltage waveform can be generated. The transformers are connected by standard Y-Y and Y-Δ connections to produce a 24-pulse waveform.
Figure 2-4. Structure of a quasi-24-pulse VSC
2.1.4 Limitations of Present Power Conditioning Systems

The present PCS topologies mentioned before are based on a six-pulse operation with thyristors. The six-pulse operation generates a great deal of harmonics by introducing DC voltage or current into the utility line. To reduce the harmonics, the utility line needs either a large filter or multiple six-pulse PCSs connected together with a phase shift between each of the six pulses. Another method requires phase matching transformers for each PCS. Figure 2-5 and Figure 2-6 show the matching transformer for each of the PCSs used to reduce the harmonics of its output current. The use of transformers does increase the size and the cost of the PCS.

Figure 2-5. The CSC with Y-Y and Y-Δ transformers achieving 12-pulse current
Those applications that the SMES PCS should oversee may need strict harmonic regulations and faster speed requirements. Figure 2-7 shows harmonic contents of the six-, twelve-, and twenty-four-pulses. The single six-pulse CSC has the largest harmonic content. The 12-pulse VSC can be created by using two six-pulse CSCs with a Y-Y and Y-Δ connected transformer. In this case, the 5th, the 7th, the 17th, and the 19th harmonics are reduced by introducing a 30° phase angle between the two six-pulse VSCs. By introducing four six-pulse VSCs with 15° between each, the 11th, and the 13th harmonics are additionally reduced. However, these values are the minimum values that can be obtained by mixing six-pulse VSCs. Additional reduction of the harmonics might be achieved by introducing more six-pulse VSCs. However, the method requires complicated and precise transformers to make it effective.
Figure 2-7. Amount of the harmonic contents of the 6-, 12-, and 24-pulse VSCs

In addition, the dynamic range of the PCS is limited by the switching frequency due to the use of thyristors with six-pulse operation.
Even though there are slight differences among them, the common disadvantages of the current PCS topologies can be summarized as follows:

1. Transformer requirements (large size and high cost)
2. high harmonics
3. slow dynamics

These are common problems of high-power applications that use thyristors. These problems can be solved by using PWMs with high-speed switches.

2.2 The Proposed Power Conditioning System

2.2.1 Issues of the Present Power Conditioning System

As mentioned in previous sections, the present PCSs that use thyristors contain high harmonics due to their six-pulse operation. In addition, the six-pulse operation limits the dynamic responses of the PCSs. To reduce harmonic contents, current PCSs use transformers employing different firing angles for each of the six-pulse units. Using the transformers not only increases the size of the system but also increases the cost because the transformers need to be matched precisely to make the multiple six-pulse operation effective in reducing the harmonics. This makes the transformers expensive. The six-pulse operation also limits the dynamic range of the total SMES system.

2.2.2 Expected Improvements

The present PCSs have high harmonics, slow dynamics, large sizes, and high costs. These are due to the six-pulse operation, which is necessitated by the speed limits of the thyristors. By employing high-speed switches such as an IGBT, which has an order of ten times faster than that of the thyristor, high-speed PWM operation becomes possible, and that leads to a significant reduction of the harmonics. By reducing the harmonics, the PCS no longer needs the transformer, since it fills the same function of reducing size and cost. In addition, the IGBT can expand the dynamic range of the PCS. Those improvements in the harmonics and the dynamic range, coupled with increased speed, could create an impressive PCS.
2.2.3 Device Selection

As mentioned above, the speed of the PCS is the essential point in improving performance and reducing size and cost. The speed of the PCS is mainly determined by the switching devices used. Therefore, selection of a high-speed switching device must be the first step. As demand increases and the technology improves, various types of high-power, high-speed devices such as IGBT, MOS controlled thyristor (MCT), static induction thyristor (SIT), and MOS controlled turn-off device (MTO), in addition to the GTO, have become available now. Among these, only the GTO and the IGBT have been widely accepted for high-power applications. Others are in the early stage of development and/or have found some limited applications.

Table 2-1 shows a comparison of these two types of devices in terms of various performance parameters for the currently available highest power rating devices. As shown in the table, the GTO has about six times the power rating than the IGBT. However, the IGBT is about six times faster than the GTO. All other aspects also favor of the IGBT.

<table>
<thead>
<tr>
<th></th>
<th>GTO 6000-V 4000-A</th>
<th>IGBT 3300-V 1200-A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conduction Voltage Drop</td>
<td>4.5-V</td>
<td>3.5 V</td>
</tr>
<tr>
<td>Turn-off Time</td>
<td>32-μS</td>
<td>3.6-μS</td>
</tr>
<tr>
<td>Turn-on Time</td>
<td>13-μS</td>
<td>3.5-μS</td>
</tr>
<tr>
<td>Gate Drive Peak Current Requirement</td>
<td>850-A</td>
<td>10-A</td>
</tr>
<tr>
<td>Snubber Circuit Requirement</td>
<td>Large</td>
<td>Small</td>
</tr>
<tr>
<td>Short Circuit Protection</td>
<td>Difficult</td>
<td>Easy</td>
</tr>
<tr>
<td>Derating Factor (Based on RBSOA)</td>
<td>0.4·Vce, 0.2·Ic</td>
<td>0.6·Vce, 0.2·Ic</td>
</tr>
</tbody>
</table>
2.2.4 System Topology Selection

2.2.4.1 Criteria

After finding a suitable device for the new PCS, the next step will be the selection of the system topology. Together with the device, the performance and cost of the new PCSs are related to the topology used. As mentioned in Section 2.1, there are two different approaches to the PCS topology: the CSC and the chopper-VSC. Even though the new PCS is supposed to use high-speed PWM, the fundamental operation principles should be the same as that of the present PCSs.

These two approaches are outlined in Figure 2-8. The CSC topology has three legs. Each of the legs has two switches and diodes connected in series. The VSC topology has a chopper in followed by a VSC and a DC link with a big capacitor bank in between. The chopper has two legs of switch and diode set, and the VSC has three legs of two series connected switches with anti-parallel diode. Both of the topologies require a inductor and a capacitor for filtering at the SMES side and three filter capacitors at the utility side. The VSC topology requires additional three filter inductors at the utility side.

When the two topologies are compared in terms of the number of power device required, the CSC topology needs six sets of switch and diode pair, while the VSC topology needs eight of them in addition of three more filter inductors at the utility side. Therefore, it seems natural that the CSC topology is better than the chopper-VSC topology. This idea is usually true for an application in which a current source is the main power source/sink.
However, the SMES coil current is not just a simple current source, because the SMES coil current is changed according to the energy stored in. The energy capacity of the coil needs to be made use of while considering the vast changes in current involved in its operation. The evaluation process of the topology should include all of these factors.

As mentioned in the introduction, the SMES is an inductor which stores energy in the form of current. The amounts of current increases as the SMES charges. The total amount of energy is $E = \frac{1}{2}LI^2$. Figure 2-9 shows the relationship between current and energy.

The shaded area is the amount of energy stored in the SMES. The area between $I_{\text{max}}$ and $I_{\text{min}}$ is the amount of energy that can be used. Therefore, the larger the difference, the more energy that can be used. When the $I_{\text{min}}$ is 30% of the $I_{\text{max}}$, 91% of the total energy...
stored in the SMES coil can be used.

Figure 2-9. Amounts of usable energy stored in the SMES

In a case like this, the system cost is not primarily determined by the component counts, but by the current, voltage, and thermal stresses of the total power devices. These factors are the most important aspects of the system for the high-power, high-speed PWM application where the semiconductor devices are very expensive compared to the other part of the system. So, a closer analysis is needed to evaluate the superiority of these two approaches. In this section, three of different comparisons are made of the total power device requirements, the device V-A ratings, the conduction losses, and the switching losses of these two approaches.

2.2.4.2 Estimation of Power Device Requirement

As mentioned before, the total amount of the power device requirement mostly determines overall cost of the system. The power device requirement is mainly determined by the power handling and thermal capacity requirements of the device. The power handling capacity corresponds to the volt-ampere requirement of the device, and the thermal capacity is determined by the conduction and switching losses. The
comparisons are made through estimated values of the total volt-ampere requirements, the conduction losses, and the switching losses. These values can be calculated with the expected values of voltage and current during normal operations of the each system.

The comparison is made under the condition that the current of the SMES coil can vary within \( I_{\text{max}} \sim I_{\text{min}} \), in which the required maximum power handling capability is \( S_{\text{max}} \), with the maximum active power \( P_{\text{max}} \) and maximum reactive power \( Q_{\text{max}} \). The PCS is assumed to be controlled with a PWM with a maximum DC link voltage/current utilization of 90%.

### 2.2.4.2.1 CSC Approach

In the CSC, the maximum AC RMS phase current at the lowest coil current is

\[
I_{\text{CSC}} = 0.90I_{\text{m}}\left(\frac{k}{\sqrt{2}}\right) = 0.64I_{\text{max}}/k.
\]

The RMS line voltage required is

\[
V_{\text{line}} = S_{\text{max}}/\left(\sqrt{3}I_{\text{CSC}}\right) = 0.91kS_{\text{max}}/I_{\text{max}}.
\]

The voltage rating of the switches and diodes should be higher than

\[
\sqrt{2}V_{\text{line}} = 1.28kS_{\text{max}}/I_{\text{max}}.
\]

The total device V-A rating of the CSC approach according to peak device voltage and current can be calculated as

\[
\text{VA}_{pk} = 6\cdot\sqrt{2}\cdot V_{\text{line}}\cdot I_{\text{max}} = 7.70kS_{\text{max}}.
\]

For the total conduction loss, the coil current is always conducted by two switches and two diodes. So the total conduction loss by all diodes and switches is

\[
P_{\text{con}} = 4V_{\text{on}}I_{\text{max}}.
\]

Again, considering the effect of voltage stress, the conduction loss function can be modified as
(2-6) \[ P_{1\text{con}} = 4V_{on}I_{\max} \sqrt{2V_{\text{line}}}/V_{dc} @ t = 4.62kV_{on}I_{\max} \frac{S_{\max}}{P_{\max}}. \]

The switching frequency of the CSC is assumed also to be \( f \) to achieve a control performance similar to that in the VSC approach. The total volt-ampere switched per second is

(2-7) \[ VA_{\text{sw}} = 2.7V_{\text{line}}I_{\max}f = 2.45kS_{\max}f. \]

2.2.4.2.2 VSC Approach

The DC link voltage in the VSC approach will be

(2-8) \[ V_{dc} = \frac{P_{\max}}{0.90*I_{\max}/k} = 1.11k\frac{P_{\max}}{I_{\max}}, \]

where \( k \) is the ratio of \( I_{\max}/I_{\min} \).

The phase current in the voltage source converter for a given apparent power \( S \) will be

(2-9) \[ I_{VSC} = \frac{|S|}{\sqrt{3*0.90V_{dc}/\sqrt{2}}} = 0.82I_{\max}S/(kP_{\max}). \]

Considering the maximum coil current, the total device V-A rating of the VSC approach according to peak device voltage and current will be

(2-10) \[ VA_{pk} = V_{dc} \times (2*I_{\max} + 6*\sqrt{2}*I_{VSC}) = +2.22kP_{\max} + 7.69S_{\max}. \]

In considering total conduction loss, the coil current is always conducted by two power devices in the boost chopper, which could be two diodes, two switches, or one switch plus one diode. On average, one diode and one switch are used to conduct the coil current. In the VSC, the average current in the worst case in both diodes and switches in one phase is less than 90% of phase RMS current. Assuming the conduction voltage drop for a diode and a switch is the same and equals \( V_{on} \), then the conduction loss of the total devices will be

(2-11) \[ P_{2\text{con}} = 2V_{on}I_{\max} + 3*0.90*V_{on}I_{VSI} = (2 + 2.20\frac{S_{\max}}{P_{\max}})V_{on}I_{\max}. \]

In the above equation, the effect of voltage stress is not considered. The total conduction
loss will be higher if the voltage stress mandates higher voltage rating switches or more switches in series. To consider this effect, the above equation can be modified according to the DC link voltage, which is proportional to the reciprocal of $k$:

$$P_{\text{con}} = k * P_{\text{con}} = (2k + 2.20 \frac{S_{\text{max}}}{I_{\text{max}}})V_{on} I_{\text{max}}.$$

This equation can reflect total conduction loss more accurately.

The switching loss is proportional to the voltage and current stress that a switch will see during switching action. Therefore, the total V-A switched per second that is proportional to the actual switching loss will be

$$V_{A_{\text{sw}}} = V_{dc} (I_{\text{max}} + 2.70I_{\text{VSC}}) f = (1.11kP_{\text{max}} + 2.45S_{\text{max}}) f,$$

where $f$ is the switching frequencies for both the chopper and VSC.

**2.2.4.3 Comparison**

The $V_{A_{pk}}$, which is the total volt-ampere requirement of the system is also closely related to the gate drive and snubber requirements, and $P_{\text{con}}$ directly reflects device conduction loss, and $V_{A_{sw}}$ is closely related to total switching loss. They are functions of $k$, the coil current range in which maximum power capability is to be kept. For an example system of $S_{\text{max}} = P_{\text{max}} = 100$-MW(MVA), these parameters are listed in Table 2-2 for a set of $k$.

From the table, the CSC approach is inferior to the VSC approach in every aspect except for $k=1$, where the maximum power is required only at maximum coil current. Other factors, such as the discrete device voltage and current ratings, and circuit design optimization, will play an important role regarding the selection of the CSC approach or the VSC approach. For $k=3$, which is assumed in the ETM program, the device VA rating of the CSC is roughly 50% higher than that of the VSC. Two important factors are not considered in Table 2-2: that the conduction voltage drop of a power device increases with the current; and that several choppers that can be interleaved to reduce switching frequency are required for a VSC. These two factors make the VSC approach even more favorable. Generally, the VSC approach will have a lower system energy loss and cost less than the CSC approach. In addition, more advanced techniques, such as multi-level converters and soft-switching topologies, are available for the VSC than the CSC.
Table 2-2. Comparison of the CSC and the VSC for the power semiconductor device requirements for a 100-MW PCS

<table>
<thead>
<tr>
<th>k</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>$VA_1_{pk}$</td>
<td>770 MW</td>
<td>1541 MW</td>
<td>2311 MW</td>
<td>3082 MW</td>
<td>3852 MW</td>
</tr>
<tr>
<td>$P_{1_{con}}$</td>
<td>$4.62V_{onI_{max}}$</td>
<td>$9.24V_{onI_{max}}$</td>
<td>$13.9V_{onI_{max}}$</td>
<td>$18.5V_{onI_{max}}$</td>
<td>$23.1V_{onI_{max}}$</td>
</tr>
<tr>
<td>$VA_1_{sw}$</td>
<td>$245f$ MW</td>
<td>$491f$ MW</td>
<td>$736f$ MW</td>
<td>$982f$ MW</td>
<td>$1227f$ MW</td>
</tr>
<tr>
<td>$VA_2_{pk}$</td>
<td>991 MW</td>
<td>1213 MW</td>
<td>1435 MW</td>
<td>1657 MW</td>
<td>1869 MW</td>
</tr>
<tr>
<td>$P_{2_{con}}$</td>
<td>$4.2V_{onI_{max}}$</td>
<td>$6.2V_{onI_{max}}$</td>
<td>$8.19V_{onI_{max}}$</td>
<td>$10.2V_{onI_{max}}$</td>
<td>$12.2V_{onI_{max}}$</td>
</tr>
<tr>
<td>$VA_2_{sw}$</td>
<td>$356f$ MW</td>
<td>$467f$ MW</td>
<td>$578f$ MW</td>
<td>$689f$ MW</td>
<td>$800f$ MW</td>
</tr>
</tbody>
</table>

Where

$VA_1=$ CSC-type PCSs;

$VA_2=$ VSC-type PCSs;

$k = \frac{I_{max}}{I_{min}} \cdot P_{max} \cdot Q_{max}$

$VA_{pk}=$ total device volt-ampere rating according to peak voltage and current stress;

$P_{con} =$ total device conduction loss; and

$VA_{sw}=$ total amount of volt-ampere related to the switching.

Figure 2-10 shows the linear interpolation of the peak volt-ampere requirements of the two approaches for $k$ from one to five. The chopper-VSC topology requires less volt-ampere capacity when the $k$ value is above 1.4. Together with the other two factors shown in Table 2-2, this shows that the chopper-VSC topology is more suitable for the new SMES PCS.
2.2.5 Operation Modes of Selected Topology

There are two different modes of operation for the SMES PCS. One is for charging of the SMES coil and the other is for discharging. Figure 2-11 shows the direction of power flow for the two modes. For both of the operation modes, the DC link is assumed to have a constant $V_{dc}$ as shown in Figure 2-11.

Figure 2-10. Total power rating requirements of the two different types of PCSs for 100-MVA
2.2.5.1 Charging Mode

The SMES coil can be charged by providing positive voltage $V_c$ across the filter capacitor $C$. This can be done by turn-on of the two chopper switches $S_{C1}$, and $S_{C2}$. When either one of the switches is turned off, $I_{SMES}$ will flow through the opposite diode of the same leg. This will cause freewheeling of $I_{SMES}$. By changing the duty ratio of the one switch, the average value of $V_c$ can be controlled. So, the amount of charging power can be controlled.

Since the DC link assumed as having constant voltage, the energy should come from the utility through VSC. For the charging, the VSC should be operated as a rectifier to get energy from the utility. The operation of the rectifier is the same as the normal three-phase rectifier. For the rectifier, the high-speed PWM operation can make the rectifier as a power factor corrected (PFC) one. In the case of PFC rectifier, the directions of the three-phase currents $I_A$, $I_B$, and $I_C$ should be the same as those of the three-phase voltage $V_A$, $V_B$, and $V_C$.

2.2.5.2 Discharging Mode

The discharging of the SMES requires the reverse process of the PCS. The SMES coil can be discharged by providing negative voltage $V_c$ across the filter capacitor $C$. This can
be done by turn-off of the two chopper switches. When either one of the switches is turned on, $I_{SMES}$ will flow through the switch causing freewheeling of $I_{SMES}$. By changing the duty ratio of the one switch, the average value of $Vc$ can be controlled. So, the amount of discharging power can be controlled.

During discharging mode, the energy should flow to the utility through VSC. For the discharging, the VSC should be operated as a VSI to provide energy to the utility. The operation of the VSI is the same as the normal three-phase VSI. The same as the rectifier, the high-speed PWM operation can make the output current of the VSI synchronized with the utility voltage. Therefore, the directions of the three-phase currents $I_A$, $I_B$, and $I_C$ should be the opposite as those of the three-phase voltage $V_A$, $V_B$, and $V_C$.

### 2.2.6 Multi-Level Structure

The next step for the new PCS is to build the selected topology with the selected device. However, the voltage ratings of the IGBT are still not high enough for the utility. An alternative to this barrier is using multiple of the devices connected in series. However, when the device becomes faster, it is more difficult to make the series-connected switches synchronize during switching. The IGBTs, which have about a 0.5~3-$\mu$S switching time, need a special method of voltage sharing when they are connected in series.

A topology which can guarantee voltage sharing is the multi-level topology. The multi-level topology divides the DC link voltage into multiple small-voltage links. The divided voltage source can be used to clamp voltage stress across the switches. One multi-level topology which is popularly used is the neutral-point-clamp (NPC) type [B1]. Figure 2-12 shows a leg of the NPC type multi-level topology, equivalent circuit, and possible output voltage for both two- and three-level topologies. The NPC-type three-level leg consists of four switches connected in series, two clamping diodes, and two capacitors to divide the input voltage source $V_s$. 

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Compared to a conventional two-level topology, the multi-level topology has following advantages:

1/nth of the DC-bus voltage across the switches;

reduced total-harmonic-distortion (THD) at the output waveforms for the same switching frequency;

1/nth of the switching loss for the same switching frequency; and

reduced current ripple at the filter inductor.

The disadvantages include difficulty of control, the necessity of clamping diodes, a divided input source, and a charge balance of midpoints.
2.2.7 Power Electronics Building Block

2.2.7.1 Purpose

The multi-level leg shown in Figure 2-12(b) can be a basic switching leg. The leg has three the DC link connections and an output terminal. The DC link are usually connected to bulk capacitor to make the voltage stable. Therefore, the voltage across the DC link can be assumed as fixed. The other connection to the leg is the output terminal that usually connected to an inductor that makes current from the terminal stable, too. With these two facts, the leg can accommodate all of problems associated with high-speed switching like voltage and current spike, parasitic, thermal, shoot-through, etc., and can be optimized to solve the problems. This concept is called as power electronics building block (PEBB) and the leg can be called as a PEBB leg.

Since the external connections to the PEBB leg are not involved in the high-speed switching, the overall system can be built easily by integrating the legs. All of high-speed switching related issues are dealt with the PEBB legs. The new PCS can be built with five of the PEBB legs, three of the PEBB legs are for VSC and two of them are for the chopper.

2.2.7.2 Operation Modes

Same as the two-level legs, the three-level legs also can be used for a rectifier for charging and a VSI for discharging by operating each of its legs as desired. Figure 2-13 shows the two operation modes of discharging and charging of the PEBB leg assuming the output line is connected to a constant current source. For the discharging mode, energy flows out from the DC link capacitors, $C_{S1}$ and $C_{S2}$, to the current source $I$. Energy flows into them during the charging mode. As shown in Figure 2-13, the difference between the two modes is the switch used for the PWM. The leg can be operated as an inverter by using $S1$ or $S4$, with $S2$ or $S3$ kept turned on. Using the PWM of $S2$ or $S3$ while $S1$ and $S4$ kept turned off, the leg can be a rectifier. The selection of the switch depends on the direction of the current.
2.2.8 Multi-Level Chopper and Voltage Source Converter

Compared to the traditional two-level chopper, the multi-level chopper can reduce switching loss and the size of the filter inductor significantly, in addition to reducing the voltage stress on the switches. Since the SMES coil current is fixed in one direction, a three-level chopper can be implemented by eliminating the components for the other direction of the current from the three-level leg, as shown in Figure 2-12. Two of the simplified PEBB legs are needed for the chopper, as shown in Figure 2-14.
Figure 2-14. A three-level two-quadrant chopper

Three of the PEBB legs shown in Figure 2-12(b) can be used to build a three-level VSC, as shown in Figure 2-15.

Figure 2-15. A three-level three-phase VSI

By combining the DC link of the three-level chopper and the VSI as shown above, the three-level PCS can be designed as shown in Figure 2-16.
2.2.9 The Prototype System

The concept of the next-generation PCS based on the chopper-VSC topology shown in Figure 2-16 can be verified by an experimental test system with a scaled-down capacity. The size of the test system is determined by feasible test environments and the availability of switching devices that can handle reasonable amounts of power. The maximum DC link voltage of the test system is set by the practically available DC power supply, which is 1000-V 100-A. By connecting the two power supplies in series and having a 10% margin of voltage, DC-link voltage is set to 1800-V. The switching device is selected as 1200-V 400-A IGBT counting derating. The maximum output current of each leg is set as 200-A. With the DC link voltage and maximum output current, the three-phase output of the VSC can have about 1000-Vpeak and 200-Apeak, that result in the maximum output of the system at 250-kVA.
2.3 Conclusion

Conventional PCSs have three different topologies: CSC; hybrid-CSC; and chopper-VSC. All of them use thyristors with six-pulse operation. The six-pulse operation is determined by the speed limitation of the thyristors, which also leads to high harmonic distortion. To reduce the harmonics, multiple PCSs are connected together with phase-shift techniques through transformers and different firing angles. The transformers increase the size and cost of the PCS. The six-pulse operation also limits the dynamic range of the PCS. All of these disadvantages are caused by the speed limitations of the switch. Generally, high-speed switches have a lower power capacity. To extend the power capacity of the high-speed switch, multiple switches connected in series are needed. As the switching speed increased, the series connection of the switching devices requires a method of voltage sharing among the devices. A multi-level topology is selected that make sure the voltage sharing during switching transients.

A new type of PCS that employs a high-speed switch with multi-level topology is suggested. Among various type of switching devices, the IGBT is proven to have the most desirable characteristics for the high-power, high-speed PCS. The multi-level structure can extend the voltage limit of the IGBT, resulting in extended power handling capacity of the total system. This topology allows the connection of multiple IGBTs in series, and uses clamping diodes to provide voltage-sharing between switches.

For the topology of the new PCS, two different converters, the CSC and the chopper-VSC, are evaluated. Due to the nature of the changing current of the SMES in wide range, it turns out that the chopper-VSC structure is the better choice in terms of power handling requirements of the total system devices. The test system of the new PCS employs an IGBT with a three-level chopper-VSC structure, and has a 250-kVA power capacity, a 1800-V DC link voltage, and a 200-A peak load current capacity.
Chapter 3  Evaluation of the Soft-Switching Techniques

The switching device is the most fundamental part of the system. Therefore, the experimental system design starts with device test. The purpose of this test is to obtain the switching characteristics of the device, such as voltage and current waveforms and switching losses during transients. The results of the test can be used to design the gate drive, heat sink, etc.

3.1 The Device Test with Hard-Switching

The current and voltage ratings of the maximum operating point of the experimental system become 900-V 200-A when the output becomes 250-kW. The IGBT selected is 1200-V 400-A, CM400HA-24H and the diode is an ultra-fast recovery type RM400HA-24S. Both are from the Powerex Corporation.

A test setup was built to measure the full stress of the voltage and current test, as shown in Figure 3-1. Since the circuit does not have a sufficient method of reset for the inductor $L$ – reset is accomplished by wire resistance and forward voltage drop of the diode $D$ – the duty ratio of the main switch $S$ needs to be very small. The pulses used for the test were four 20-kHz pulses per a 100-msec period. The length of the pulse is set to increase the current through the inductor $L$ at about 50-A per pulse making 200-A at the fourth pulse. Figure 3-2 shows the measured switching voltage and current waveforms and their loss measurements, $E_s$. The current spike during turn-on and the voltage spike during turn-off are about 150-A and 300-V respectively. The current spike during turn-on comes from the diode reverse recovery and leads to switching loss. The voltage spike during turn-off leaves no margin for the switch, which is unsafe.

The loss measurement $E_s$ is made with the oscilloscope using following function:

\[
(3-1) \quad E_s(t_i) = \sum_i V_s(i) \cdot I_s(i) \cdot \Delta t ,
\]

where $i$ is the sampling number and $\Delta t$ is the length of the sampling time. This is an approximated value of the integral of the product of the voltage and current of the switch.
The unit of the $E_s$ is the joule. Figure 3-3 shows measured switching losses for turn-on and turn-off for different load currents. These values, together with the conduction loss of the IGBT, can be used to estimate the total loss.

Figure 3-1. Loss-less test setup

Figure 3-2. Voltage and current waveforms of the switching test and measurement of the switching losses
3.2 Loss Estimation

Together with conduction loss – which can be easily estimated by the rated on-drop across the switch and average value of estimated current – the switching losses measured above lead to the estimation of losses for the switch. According to the data sheet, the typical value of the on drop voltage for the selected device is 2.5-V for the IGBT and 2-V for the freewheeling diode. With a maximum current of 200-A, which is set by the
design, the conduction loss of the switch can reach 250-W when the duty ratio is 0.5.

The total thermal resistance from the junction to the heat sink can be added into

\[ R_{th \, junction \, to \, case} + R_{th \, contact} + R_{th \, heat \, sink} = 0.04 + 0.04 + 0.18 = 0.26 \, ^\circ C/W \]

The heat sink assumed here is a liquid-cooled one, and the best practical product commercially available. With these thermal resistance and maximum losses, the temperature differences from junction to heat sink can reach maximum 65°C. Assuming the ambient temperature is 20°C, the junction temperature margin for the switching loss becomes about 65°C, which can lead to maximum switching frequency of 2.8-kHz.

The switch test results can be summarized as follows:

the voltage and current spikes are too large causing high loss and making the system unreliable; and

the switching frequency is limited by the thermal constraint and cannot be high enough for the new SMES PCS.

3.3 Soft-Switching Techniques

The device test showed that the switch has large voltage and current spikes. The spikes not only cause the system to be unreliable but also limit switching frequency, which eventually leads to slow dynamics of the PCS and high cost both of which contradict the objectives of the new PCS. One solution for these problems can be soft-switching, which may reduce the spikes and losses. A desirable soft-switching topology for this application should help both the turn-on and the turn-off of the switches.

3.3.1 Selection of Soft-Switching Techniques

Many soft-switching topologies were developed for various applications. Most of them have either ZVT or ZCT functions. To achieve ZVT of the main switch, G. Hua, and et al.[C1] used another small converter that had the same number of components as the main converter. This topology could make a complete ZVT of the main switch. However, both the main and auxiliary switches needed to be turned offing hard fashion. This topology used an additional capacitor to reduce turn-off loss in the main switch, which
created additional circulating energy.

The ZCT function of the soft-switching topologies is more important than ZVT for the converters that use IGBTs. G. Hua, and et al. extended the ZVT topology into ZCT by adding a series capacitor with the auxiliary inductor, forming a resonant tank [C4]. Figure 3-4 shows a basic boost converter with the ZCT circuit and its key waveforms. In this technique, a resonance is created by activating the auxiliary switch just before turn-off the main switch. By doing this, a complete ZCT of the main switch is achieved. In addition, the auxiliary switch also has a ZCT due to the resonance action. However, it needs a hard turn-on of the main switch, and some of the duty cycle is lost by the resonance.
Figure 3-4. Circuit diagram of Hua’s ZCT topology and its key waveforms
The loss measurements shown in Figure 3-3 show that both the turn-on and turn-off transitions need help. Therefore, the soft-switching topology for this application should have both ZVT and ZCT functions together. Since the power level is so high and the current is too large, the auxiliary switch also needs to be soft-switched. However, few soft-switching topologies were reported that can make all switches be soft-switched. Therefore, the selection has to be made based on which topology can give the best results.

One soft-switching topology that has both ZVT and ZCT functions is suggested in Appendix A. Figure 3-5 shows a basic boost converter with the soft-switching circuit and its key waveforms. This topology utilizes part of the main inductor to get the power source for soft-switching. By doing this, the topology does not have any resonance action that will save duty cycle loss. However, it could not make the auxiliary switch soft-switched.
Figure 3-5. Circuit diagram of a ZVT and ZCT topology and its key waveforms
H. Mao, and et al. [C5] modified [C4] by exchanging the auxiliary switch and the auxiliary diode for each other and activating the auxiliary switch twice for each transition of the main switch. By doing this, the topology makes both the main and the auxiliary switch ZCT, and reduces large amounts of the main diode current before turn-on the main switch that will reduce large amounts of turn-on loss. However, this topology needs a resonance action for each transition, which will increase duty cycle loss. Figure 3-9 shows the basic boost converter circuit and key waveforms of the topology.
Figure 3-6. An example of a boost converter comprised of Mao’s ZCT topology and its key waveforms
Table 3-1 shows a brief comparison of the three topologies in terms of the switching conditions of the main switch, auxiliary switch, etc. The ZVT and ZCT topology has a complete ZVT function, while Mao’s ZCT has only part of the ZVT function, and Hua’s ZCT does not have any ZVT function at all. However, in terms of the soft-switching of the auxiliary switch, Mao’s and Hua’s ZCT have a complete ZCT, which the ZVT and ZCT topology does not have. Since the SMES PCS needs a high current operation ability, the biggest concern is the turn-off of all its switches. Therefore, Mao’s ZCT topology is selected as the soft-switching topology for the SMES PCS.

Table 3-1. Comparison of the two soft-switching topologies

<table>
<thead>
<tr>
<th></th>
<th>Hua’s ZCT</th>
<th>ZVT and ZCT</th>
<th>Mao’s ZCT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Main switch</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn on</td>
<td>Hard</td>
<td>ZVT</td>
<td>Reduced reverse</td>
</tr>
<tr>
<td>Turn off</td>
<td>ZCT</td>
<td>ZCT</td>
<td>ZCT</td>
</tr>
<tr>
<td><strong>Auxiliary switch</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn off</td>
<td>ZCT</td>
<td>Hard</td>
<td>ZCT</td>
</tr>
<tr>
<td><strong>Circulating Energy</strong></td>
<td>Set to max. load</td>
<td>Depends on load</td>
<td>Set to max. load</td>
</tr>
<tr>
<td><strong>Number of Extra Components</strong></td>
<td>4</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td><strong>Duty cycle loss</strong></td>
<td>Fixed</td>
<td>Depends on load</td>
<td>Fixed</td>
</tr>
</tbody>
</table>

3.3.2 Operations of the Selected Zero Current Transition Topology

Sample boost converter of the ZCT topology selected in the previous section is shown in Figure 3-6. This topology not only provides for the ZCT operation of the main switch but also helps reduce the main diode current significantly by turn-on the auxiliary switch before the main switch is turned on. Figure 3-7 shows detailed turn-on stages, and Figure 3-8 shows detailed turn-off stages. Detailed operation stages of the circuit are explained below.
3.3.2.1 Turn-On

At \( t_0 \), shown in Figure 3-6, the auxiliary switch is turned on, starting a resonance. The resonance current increases the current through the \( D \) and charges the resonant tank capacitor.

At \( t_1 \), the current is reduced back to zero and starts to draw out current from the \( D \). The \( S_x \) can be turned off after this point with zero current.

At \( t_2 \), the \( S \) is turned on when the current through the \( D \) reduced to minimum. From this point, the \( i_x \) is reduced rapidly by the \( V_o \). This condition continues until the anti-parallel diode of the \( S_x \) recovers.

During \( t_3 \) to \( t_4 \), the resonant tank current caused by the reverse recovery is reduced to zero.

At \( t_4 \), the turn-on process finishes and the PWM turn-on period continues until \( t_5 \).

![Diagram of turn-on process](image-url)

Figure 3-7. Operating stages for the turn-on of the selected soft-switching topology
3.3.2.2 Turn-Off

At $t_5$, shown in Figure 3-8, the auxiliary switch is turned on, starting a resonance. The resonance current increases the current through the $S$ and charges the resonant tank capacitor.

At $t_6$, the current is reduced back to zero and starts to draw out current from the $S$. The $Sx$ can be turned off after this point with zero current.

At $t_7$, the current through the $S$ is reduced to zero. The switch current becomes negative after this point until $t_8$. During this time, the $S$ can be turned off with zero current.

At $t_8$, the load current becomes the resonant current until the D is biased forward at $t_9$.

During $t_9$ to $t_{10}$, the resonant tank current is reduced to zero.

At $t_{10}$, the turn-off process finishes.

More details of the circuit operation can be found in [C5].
Figure 3-8. Operating stages for the turn-off of the selected soft-switching topology

3.4 Design of Soft-Switching Parameters

Mao’s ZCT topology needs an auxiliary switch, a diode, and two resonant components. An IGBT module, CM150Y-24H, that has a 150-A, 1200-V capacity, is selected as the auxiliary switch and diode, based on the maximum and average current capacity. The values of the resonance components, $Lx$ and $Cx$, can be estimated using the soft-switching requirements. The key factors for the design are the maximum load current and
the turn-off time of the main switch. These two parameters can be used to estimate the characteristic impedance and the period of the resonant tank using the following relationship:

\[ T_{\text{off}} = T_0 \cos^{-1}(m)/\pi, \]

where \( m = ll_{pk} \), \( T_0 = 2\pi \sqrt{LC} \). \( I_{pk} \) is the resonance peak of \( Ix \) during turn-off. The \( I_{pk} \) can be approximately estimated as:

\[ I_{pk} = V_0/Z_0, \]

where \( Z_0 = (Lx/Cx)^{1/2} \).

Since the resonance parameters are fixed, the change of load current can affect the operating point. This can be compensated for by proper selection of the delay time between the auxiliary switch and the main switch gate signals.

For the design, the maximum current was given as 200-A, and the maximum turn-off time obtained from the device test was 1-μsec. The estimated values of the \( Lx \), \( Cx \), and \( m \) were 2-μH, 0.2-μF, and 1.5 each. Together with the auxiliary switch, the estimated values were implemented into the device test setup and tuned. Various operating points were tried to achieve the optimum operating conditions. Tested current levels and resonance times were 50-A, 100-A, 150-A, 200-A, and 4-μs, 5-μs, 6-μs. The turn-on delay \( T_{\text{d, on}} \) was about 200-ns longer than half of the resonance periods, and the turn-off delay \( T_{\text{d, off}} \) was 1.4 to 1.9 times of the resonance periods. Selected parameters shown in Figure 3-9 for the best result are as follows:

- Peak Current ratio \( Ip/I_0 \): 1.3 ~ 1.8 : 1.5;
- Resonant Time \( T_r \): 4-6-μsec : 4-μsec;
- Delay Time \( T_{\text{d, on}} \): 1.4 ~ 1.9 (of \( 1/2T_r \)) : 1.5 + 200-ns;
- Delay Time \( T_{\text{d, off}} \): 1.4 ~ 1.9 (of \( 1/2T_r \)) : 1.5.
Figure 3-9. A soft-switching test circuit of the selected topology and definitions of the parameters
3.5 Device Test with Soft-Switching

Figure 3-10 shows the measured voltage and current waveforms with hard- and soft-switching. Figure 3-11 shows their loss measurement comparison. The current spike during turn-on and the voltage spike during turn-off are reduced to 0-A and 100-V each. Even though the topology cannot reduce the diode current to zero during the turn-on of the main switch, the loss is reduced significantly. The voltage spike during turn-off leaves large margin for the main switch, which is another advantage of soft-switching. Compared to the test of hard-switching, the amount of loss saved by soft-switching is about 90% of its total loss for the 200-A case.
Figure 3-10. Comparison of the voltage and current waveforms

(a) Hard-switching

(b) Soft-switching
Figure 3-11. Comparison of the switching losses

Es (mJ)

Hard-switching

- Total
- Turn-off
- Turn-on

Soft-switching

- Total
- Turn-on
- Turn-off
3.6 Switching Frequency

As mentioned in Chapter 1, the switching frequency is one of the biggest concerns for the SMES PCS. The higher the frequency, the better. However, the device test results and the loss estimation show that the value cannot be extended much. With the help of the ZCT soft-switching, the frequency can be extended about ten times higher than that of the hard-switching case, in terms of the switching loss aspect. In addition, the soft-switching topology needs two resonance actions to complete the soft-switching. Each of those requires about two to three microseconds, and total of five microseconds per switching cycle. This is the duty cycle loss. Generally the duty cycle loss should not exceed 10% of the duty, in order to utilize the system efficiently. Considering this factor, the switching frequency is set to 20-kHz for the SMES PCS test system.

With the selected switching frequency, the bandwidth of the low-pass filter can be determined as needing to be one-tenth of the switching frequency to suppress switching ripple sufficiently. The size of the inductance of the filter is determined by the amount of output current ripple. The reasonable value of the current ripple is about 10% to 20% of the maximum currents. Therefore, the value of the inductance becomes about 0.6-mH, allowing a 30-A_{p-p} ripple. The output capacitor is set to 10-μF, which will make a double pole at 2-kHz.

3.7 Conclusion

The device is tested using the hard-switching. The test results show that the hard-switching method has large current and voltage spikes that will reduce system reliability. This method also has high switching losses that cannot allow high switching frequency. A solution for these problems is to use a soft-switching technique. Among various types of soft-switching topologies, the topology that can achieve zero current for all of its switches is selected. A device test with the soft-switching circuit shows a large reduction of the voltage and current spikes, and about a 90% reduction of switching losses enabling the switching frequency to reach up to 20-kHz. With the selected switching frequency, the bandwidth of the low-pass filter can be extended to 2-kHz.
Chapter 4  The Power Electronics Building Block

4.1  Soft-Switching of the Power Electronics Building Block

4.1.1  Soft-Switching for the Power Electronics Building Block

The soft-switching topology selected in Section 3.3 needs to be implemented into the PEBB leg. For implementation, the soft-switching topology needs to be identified in terms of the PWM switching cell concept. Figure 4-1 shows the selected soft-switching topology implementation on sample boost converter. The topology can be implemented in other converters by identifying circuit configurations with PWM switching cells. Figure 4-2 shows the selected soft-switching topology implemented in the PWM switching cell.

Implementation of the soft-switching circuit on the PEBB leg requires an identification of the PWM switching cells in the PEBB leg for each of the operation modes. Figure 4-3 and Figure 4-4 show the PWM cell identifications of the PEBB leg and their soft-switching implementations in terms of the PWM switching cell configurations for the discharging mode and the charging mode. As shown in Figure 4-3 (a) and (c) and Figure 4-4 (a) and (c), both of the operation modes share a common terminal, C, of the PWM switching cell. For the active, A, and the passive, P, terminals of the two operation modes, if the $S_a$ and the $S_b$ shown in Figure 4-3 are kept turned on, then the active and passive terminals can be opposite each other. The reason the $S_a$ and the $S_b$ can be kept turned on is as follows. In Figure 4-3 (c) and Figure 4-4 (c), when the $S$ is turned on, the $D$ can block the input voltage, instead of the $D$ and the $D_a$ for the positive modes, and the $D$ and the $D_b$ for the negative modes. This can make the implementation of the soft-switching circuit simpler, because the soft-switching components for both of the operation modes can be shared. When an IGBT module is used as the auxiliary switch and diode pair, the anti-parallel diode can be used as the auxiliary diode of the other mode. By doing this, the resonance tank can also be shared. Figure 4-3 (b) and (d) and Figure 4-4 (b) and (d) show the corresponding soft-switching implementations in the
PEBB leg for each of the operation modes.

Figure 4-5 shows the finalized soft-switching implementation for the PEBB leg, and Figure 4-9 shows its hardware implementations.

![Figure 4-1. Sample boost converter using a selected soft-switching topology](image)

![Figure 4-2. Soft-switching circuit implementation on the PWM switching cell](image)

(a) Without soft-switching
(b) With soft-switching
Figure 4-3. Identification of the PWM switching cell for the positive operating modes and its soft-switching implementation
Figure 4-4. Identification of the PWM switching cell for the negative operating modes and its soft-switching implementation
4.1.2 Soft-Switching for the Chopper

The three-level chopper leg design and implementation are discussed in other work. Details can be found in [B25]. In this work, the soft-switching operation of the chopper is discussed.

Figure 4-6 shows the three-level chopper. The chopper can be implemented with two PEBB legs which are fully tested with part of the switches removed from the positive and negative sides. According to Figure 4-3 (a), (b), (g), and (h), the soft-switching circuit for the $S_1$ and the $S_2$ can be implemented as shown in Figure 4-7 (a).

When Figure 4-7 (a) is compared to the PEBBp leg shown in Figure 4-6, it is found that one more switch, $S_3$, is needed. The switch will provide current paths for the soft-switching of the $S_2$. However, using two auxiliary switches for the soft-switching of one main switch is not desirable. In addition, the anti-parallel diode of the switch $S_3$ should have the same current capacity as that of the $D_2$. In this case, the chopper soft-switching topology can be improved by removing the $S_3$ from the circuit and connecting the resonant tank directly to the output line of the chopper as shown in Figure 4-7. The
change in the resonant tank connection does not change the soft-switching operation except in the transient of the PWM main switch between the $S_2$ and the $S_1$ for charges/discharges of the resonance capacitor. For the PEBBn leg shown in Figure 4-6, the same principle can be applied. Figure 4-8 shows the soft-switching implementation for the PEBBn leg.

![Figure 4-6. The three-level two-quadrant chopper](image)
Figure 4-7. The PEBBp leg soft-switching configurations for the three-level two-quadrant chopper
4.1.3 Hardware Construction

The PEBB leg defined above has the same structure as the three-level leg shown in Figure 2-12(b), in that is composed of four main switches connected in series with two clamping diodes between them. In addition, the soft-switching topology selected needs to be implemented into the PEBB leg. By doing this, all of the high-speed three-level PWM switching operations can be accommodated within one leg. The external connections to/from the leg are three-level DC link inputs and an output.

Figure 4-9 shows complete hardware implementation of the PEBB leg. The main switches, $S_1$ to $S_4$ and the clamping diodes, $D_p$ and $D_n$, are placed according to the circuit diagram. The switches and diodes are arranged as closely as possible to reduce parasitic inductance. Even though the soft-switching circuit helps switching transients, the two auxiliary circuits for the soft-switching are place each side, because the connection to the soft-switching circuit also involves resonant tank that smooths out the fast switching transient.

For the cooling of the devices, a 24”x12” water-cooled heat sink is used. The heat sink
has a total thermal resistance of 0.009°C/W. The equivalent thermal resistance for one main IGBT is 0.18°C/W. The value is the same as that for the loss calculation in Section 3.2. The heat sink is cooled with a water-chiller that has a 2.4-kW cooling capacity. Assuming overall efficiency of the PEBB leg at 97%, the capacity of the chiller is closely matched to the loss of the PEBB leg for a full power test.

Figure 4-9. Complete hardware implementation of the PEBB leg with the soft-switching circuit
4.1.4 Experimental Verification

4.1.4.1 Power Stage Test Setup

The purpose of the PEBB is to accommodate all of the high-speed switching-related needs into one leg. Therefore, the PEBB leg should cover all of the possible operational conditions. As mentioned in Section 2.2.5, there are two different modes of operation: the charging mode and the discharging mode. During the discharging mode, the leg provides power to output, and the charging mode receives. Each of the modes has positive and negative operations. The PEBB leg should cover all of them up to full power without having any constraints.

Each mode of operations of the PEBB leg can be achieved as shown in Figure 4-10(a)-(d). In the positive discharging mode, the PWM operation is performed with the $S_1$ and the $D_p$ while the $S_2$ is continuously turned on, as shown in Figure 4-10(a). In the negative charging mode, the operation is performed with the $S_2$ and the anti-parallel diodes of the $S_3$ and the $S_4$. In the opposite of these modes, the operation is performed with the $S_4$ and the $D_n$ with the $S_3$ turned on, and the $S_3$ and the anti-parallel diode of the $S_1$ and the $S_3$.

The operational mode test of the PEBB leg was performed as follows. The positive input was energized by a 900-V power supply, and the filter inductor was used as a reactive load. The operation of the PEBB leg started in the positive discharging mode. In the PWM operation of the $S_1$ and the $D_p$, while the $S_2$ is turned on, the load inductor was charged. During the turn-on period of the PWM, the positive input voltage charged the load inductor. When the inductor current reached the specified value of 200-A, the PWM was changed into the negative charging mode by changing PWM operation of the $S_3$, the $D_n$, the $DS_1$, and the $DS_2$ which generated negative output voltage. In the negative charging mode, the energy stored in the inductor was transferred into the negative side of the input capacitor, building negative voltage. The opposite modes of them were the same, except in the change of the polarity of the current and the voltage. Through this operation, the PEBB leg could be tested at full power in all of possible modes of operations.
Figure 4-10. Operational modes of the PEBB leg (soft-switching circuit is not shown for simplicity)
4.1.4.2 Controller

The controller is implemented with a digital signal processor (DSP) and eraseable programmable logic device (EPLD). The EPLD is to generate gate drive pulses for both main switches and auxiliary switches. The DSP provides duty ratio information to the EPLD. The DSP is connected to a personal computer emulator that can monitor the status of the DSP and change parameters. The links from the EPLD to the switches are consisted with fiber optic cable to isolate and reduce noise interference between the power stage and the controller. Detailed control circuit implementation and gate drive signal generation is described in Appendix B.

4.1.4.3 Discharging Mode

The implementation of the soft-switching circuit for the discharging mode is quite similar to that of the basic boost converter. Therefore, the soft-switching operations are nearly the same for the two. Figure 4-11 shows the turn-on voltage and current waveform comparison for the hard- and soft-switching operations with different current levels. Even though the hard-switching tests are not explained before, which will be explained in 4.3, the results are referred in here. As mentioned in Section 3.3.2.2, the soft-switching operation draws out part of the current from the diode $D_p$ before the main switch turns on, resulting in less reverse recovery. The gate drive resistance for the turn-on does not influence the reverse recovery current of the diode, as it does in the hard-switching case.

As shown in Figure 4-12, the turn-off of the soft-switching operation also shows similar waveforms to that of the basic boost converter. The waveforms are well-matched. In addition, voltage spikes during the turn-off periods decreased to within 120-V, while those of the hard-switching cases remain at 200-V. As opposed to the hard-switching case, the voltage spikes are not proportional to the amount of current in the soft-switching case.
Figure 4-11. Comparison of hard- and soft-switching voltage and current waveforms during turn-on of the discharging mode
Figure 4-12. Comparison hard- and soft-switching voltage and current waveforms during turn-off of the discharging mode
4.1.4.4 Charging Mode

Different from the case of discharging mode, soft-switching circuit implementations of the charging mode are not very similar to the basic boost converter, and the soft-switching operations are different. Figure 4-13 shows the same comparison as for the discharging mode. The turn-on waveforms do not show any significant difference. However, the turn-off waveforms look quite different from that of the discharging mode and the basic boost converter case.

![Comparison hard- and soft-switching voltage and current waveforms during turn-on of the charging mode](image)

Figure 4-13. Comparison hard- and soft-switching voltage and current waveforms during turn-on of the charging mode
Figure 4-14 shows turn-off waveforms which are quite different from those shown in Figure 4-12. Ideally, the switch current waveforms should have the same shape as those of the discharging mode. However, the current does not follow the resonance of the auxiliary circuit because of the parasitic inductance throughout the clamping diodes, $D_p$ and $D_n$, and the two middle switches, $S_2$ and $S_3$. During the start of the resonance, the switch current moves as it is supposed to, but just after the peak of the resonance, the current does not reduce at the resonant tank. After the resonant current reaches its peak, the current is supposed to be reduced by reverse bias of the inductor. However, the diode $D_p$ becomes biased forward by the voltage induced by the stray inductance of the $S$, the $S_a$, and the $D_n$, and lets the current freewheel. Figure 4-15 shows the current waveforms of the $D_p$ and the $S$. The path of the freewheeling current comes from the clamping diodes, $D_p$, and $D_n$, and the $S$, and the $S_a$. This freewheeling current continues until the $S$ is turned off. At the turn-off of the $S$, the freewheeling current causes a voltage spike until the auxiliary inductor current reaches to the load current. After that, the voltage across the $S$ returns to zero. This state continues until the resonant tank current is reduced to less than the load current and the $D$ starts to be turned on. So, the actual voltage is not increased immediately after the $S$ is turned off. This results in a small loss compared to similar processes in hard-switching operation.
Figure 4-14. Comparison hard- and soft-switching voltage and current waveforms during turn-off of the charging mode
Figure 4-15. The switch (top) and the clamping diode (bottom) current waveforms during the charging mode of soft-switching operation.
Figure 4-16. Parasitic inductance throughout the main switches and the clamping diodes.

Figure 4-17 shows simulated waveforms of the switch and the diode currents and the switch voltage. Figure 4-18 shows detailed operation stages of the turn-off process. Following is a detailed description of the process.

(a) $t_0$-$t_1$:

When the auxiliary switch $S_x$ turns on at $t_0$, the auxiliary circuit resonance starts and the resonant current reaches its maximum value at $t_1$.

(b) $t_1$-$t_2$:

After the resonant current reaches its maximum value at $t_1$, the current starts to decrease due to the resonant action. In the meantime, there are voltage drops in the loop of the resonant path. The voltage across the parasitic inductance of the $S_a$, the $S$, and the $D_n$ let the $D_p$ be biased forward, resulting in a freewheeling of the current through the $S_a$, the $S$, the $D_n$, and the $D_p$. The resonant current path is formed by the forward biased $D_p$.

(c) $t_2$-$t_3$:

The freewheeling current is interrupted by the turn-off of the $S$ at $t_2$. The freewheeling current charges up the parasitic capacitance of the $S$ until the auxiliary current takes up
the load current.

(d) t3-t4:
After the resonant current reaches the load current, the voltage across the S returns to zero. However, the resonant action continues, and the resonant current freewheels until the current is larger than the load current.

(e) t4-t5:
At t4, the resonant current reaches an equal balance with the load current and reduces further. The remaining part of the load current flows through the $D$.

(f) t5:
At t5, the resonance is finished and the PWM turn-off period starts.
Figure 4-17. Simulation results of the charging mode soft-switching turn-off operation.
Figure 4-18. The sequence of the turn-off process of the soft-switching operation for the charging mode
4.2 AC Operation

4.2.1 The Duty Cycle Limitation of Soft-Switching

The soft-switching topology selected utilizes the resonance action between an inductor and a capacitor. To make the soft-switching effective, the resonance has to be finished within the switching cycle and it takes time to be completed. The minimum time required the PEBB leg to finish the soft-switching operation as designed in Section 3.4 is about 10-μsec. During this time, the duty ratio of the main switch can not be changed. If the duty ratio is less than that, the soft-switching action can not be completed, resulting in ineffective at all eventually. Figure 4-19 shows the resonant tank current and voltage together with the main switch current. During the turn-on of the main switch, one resonance action has to be completed. The $T_{on1}$ is the time required for the resonant tank building current, and the $T_{on2}$ is the time to finish the resonance, and to prepare for the turn-off. The time $T_{off2}$ is to draw out current from the main switch, and the $T_{off1}$ is for the next cycle. The time $T_{on2} + T_{off2}$ is the minimum time required for the soft-switching operation and the duty ratio can not be smaller than that.

In addition, there is maximum duty ratio limitation. The main switch should not be turned off more than $T_{on1} + T_{off1}$. 


4.2.2 Experimental Results

The next experiment of the PEBB legs involves AC operation. The purpose is to see the PEBB leg operations under variable duty cycle with the soft-switching technique. In this test, the PEBB leg receives gate signals that can produce sinusoidal output voltage. Since the soft-switching operation has duty ratio limitation, which is about 10-\(\mu\)sec, the duty ratio less than that cannot be applied. By using the neutral point as the reference for the output, the PEBB leg can generate bipolar output voltages. Figure 4-20 shows the sinusoidal test setup with the resistor load. Figure 4-21 shows the output voltage and current waveforms of the PEBB leg with the soft-switching operation. Due to the duty cycle limitation in the soft-switching operation, the PWM signals around the zero crossing, which is smaller than 10-\(\mu\)sec, cannot be applied, resulting in a distorted output current around the zero crossing. An alternative method for this distortion can be hard-switching operation during the small PWM duty periods.
4.3 Hard-Switching of the Power Electronics Building Block

As seen in the output current waveform of the PEBB leg with soft-switching operation, the distortion caused by the duty ratio limitation is severe around the zero-crossing of the sinusoidal waveform, and can expect a large amount of harmonic. This directly contradicts the purpose of the new PCS. Since the distortion is caused by the duty ratio limitation of the soft-switching operation, an alternative solution can be the use of the
hard-switching operation during the zero-crossing period. This method can easily be implemented by removing the soft-switching gate drive pulses from the control circuit.

4.3.1 Hard-Switching Test with Two Operation Modes

The hard-switching operation tests for the two different modes of operation, the charging operation and the discharging operation, of the PEBB leg are performed the same way at the soft-switching operation case. Figure 4-22 shows the turn-on and the turn-off voltage and current waveforms of the discharging modem, and Figure 4-23 shows the same for the charging mode, with four different load current values with maximum DC link voltage.

![Switch voltage and current waveforms of the discharging mode](image)

Figure 4-22. Switch voltage and current waveforms of the discharging mode
Different from the soft-switching operation cases, the voltage and current spikes during the switching operations are very severe and need to be taken care of. The spikes will influence the system reliability, the losses, and the EMI. The higher the spikes, the more losses and EMI and the less reliability. The objectives of the hard-switching test are to see the switching behaviors with different circuit parameters and to reduce the voltage and current spikes and switching losses during the transitions. The tests are performed by various circuit parameters such as gate drive resistance, parasitic capacitance, the DC link capacitor, the snubber, in corporation of a different switch, etc. Details of the test results are discussed in Appendix A except for the gate drive resistance and the parasitic inductor effect, which are mentioned in the following sections.
4.3.2 The Effect of Gate Drive Resistance

Usually a higher-speed gate drive makes switching faster, resulting in less switching loss. However, faster switching leads to higher $di/dt$, which leads to higher voltage spikes. The speed of the gate drive can be controlled by the gate drive resistors. The gate drive resistors are divided into two different categories: turn-on and turn-off. In this experiment, several different values of the gate drive resistors are used to find the best value and compromise between speed and spike occurrences.

During turn-on, the lower the value, the higher the current spikes, but less loss occurs. Different values are used, from zero ohm to ten ohm. For very small values for the gate resistor, the current spikes become so large that they induce large amounts noise to the gate drive circuit, creating a mal-trigger, as shown in Figure 4-25. This noise is mainly caused by the capacitive turn-on of the switch. The minimum acceptable value for the turn-on gate resistor is 4.7-$\Omega$, at which the voltage stress is about 1000-V. Figure 4-24(a) and (b) show two different values of turn-on resistor cases, which are 3.9-$\Omega$ and 5.1-$\Omega$, respectively. The voltage spike of the diode in the case shown in Figure 4-24(a) is about 120-V higher than that of the case shown in Figure 4-24(b). Reverse recovery current difference is also about 60-A for both cases.

Contrarily, during turn-off, the voltage spikes and loss are not changed much by reducing the gate resistor value. The minimum value tried is zero-ohm.
Figure 4-24. Voltage and current waveforms of the main switch with two different values of turn-on gate resistance for the discharging mode.

(a) $R_{\text{on}} = 3.9 \, \Omega$ case

(b) $R_{\text{on}} = 5.1 \, \Omega$ case

Figure 4-25. Noise introduced into the gate drive signal with $R_{\text{on}} = 2 \, \Omega$
4.3.3 The Effect of Parasitic Inductance

Another important factor in spike occurrence is parasitic inductance. For a given $di/dt$, the voltage spike is proportional to the inductance. The $di/dt$ itself also depends on the inductance. The voltage and current spikes during switch transients primarily depend on parasitic inductance. During turn-on of the switch, the diode associated with the switch needs to be turned off. During reverse recovery of the diode, the reverse current flows through the diode until the diode is recovered. For this period, the current spike is inversely proportional to the parasitic inductance. The objective of the parasitic study is to identify the difference of the parasitic and its effects for the two operational modes of the PEBB leg.

The parasitic inductance of the switching path strongly depends on the area of current change. It is clear that the discharging mode operation has a smaller current changing area than that of the charging mode.

Figure 4-26 shows the area difference of the two modes and their physical areas. The area $A$ is for the discharging mode case and the area $B$ is for the charging mode case.

The voltage and the current spikes for the two modes are quite different. Figure 4-27 shows the voltage and current waveforms of the $S1$, for discharging mode, and the $S3$, for charging mode for the turn-off transients up to a 200-A switching current. The voltage spike at the $S1$ is about 180-V, resulting in a voltage stress of 1080-V across the switch. At the $S3$, the spike is about 270-V, leaving a margin of 30-V under the allowed maximum voltage stress of the switch. The cases of the $S2$ and the $S4$ are quite similar to those of the $S3$ and the $S1$. 
Figure 4-26. Area of current change (shaded area)
The voltage spikes are very important for the safe operation of the PEBB leg. The voltage spike depends on the $di/dt$ during the transients and the parasitic associated with it. During turn-on of the main switch, the $di/dt$ is caused by the reverse recovery of the diode and can be controlled by the gate drive resistor. During turn-off, on the contrary, it is not effectively controlled by the gate resistor and depends primarily on the parasitic for control. The parasitic capacitance is determined by the structure inside of the device and makes the spike worse as it increases. Parasitic inductance, however, is determined by the arrangement of the devices. Therefore, the voltage spikes can be minimized by reducing
parasitic inductance as much as possible.

Consequently, parasitic inductance has to be reduced to as low as possible using the control of spikes through the gate drive resistor. The selected value of the gate resistor for turn-on is $4.7\,\Omega$, and that for turn-off is zero.
4.4 Laminated Bus

The parasitic inductance can be effectively reduced by using a laminated DC link bus. A laminated bus consists of three layers copper plates. The layers are insulated with mylar laminate sheets on both sides of the bus. The sheet has a 3000-V insulation capacity. With both side of the bus plate insulated, the insulator has more than a 6000-V insulation capacity.

Figure 4-28 shows the PEBB leg with the laminated bus. The bus has three layers. The top layer is the $P$ side of the input source. The medium layer is the $O$ side, and the bottom layer is the $N$ side. The switch arrangement of the PEBB leg with the laminated bus is the same as that without the laminated bus, except for the clamping diode $D_p$. The diode is placed in back to make space for the high-frequency capacitors that are placed parallel with the DC link capacitors $C_p$ and $C_n$, promoting the effectiveness of the laminated bus.

The test results show that the output voltage waveforms are nearly the same as that without laminated bus, but the voltage and current spikes of the main switches during switching transients, as expected, are greatly reduced. From Figure 4-29 to Figure 4-32 show the voltage spike of the $S_1$ and the $S_3$ during turn-on and turn-off with and without laminated bus for hard- and soft-switching.
Figure 4-28. The soft-switching PEBB leg without and with the laminated bus
Figure 4-29. Switch voltage spikes during turn-on and turn-off of the discharging mode for the hard-switching operation with and without the laminated bus.
Figure 4-30. Switch voltage spikes during turn-on and turn-off of the charging mode for the hard-switching operation with and without the laminated bus.
Figure 4-31. Switch voltage spikes during turn-on and turn-off of the discharging mode for the soft-switching operation with and without the laminated bus
Figure 4-32. Switch voltage spikes during turn-on and turn-off of the charging mode for the soft-switching operation with and without the laminated bus

4.5 AC Operation with a Mixture of Hard-Switching and Soft-Switching Operations

The next test of the PEBB legs is the mixture of the hard-switching operation and the soft-switching operation. Figure 4-33(a) shows the output voltage and current waveforms with the soft-switching operation only. Due to the duty ratio limitation of the soft-switching operation, the PWM signals around the zero crossing, which is smaller than 10-μsec, can not be applied, resulting distorted output current around the zero crossing. This distortion can be avoided by applying the hard-switching operation during the small
PWM duty periods around the zero-crossing, as shown in Figure 4-33(b).

Efficiencies were measured with the two switching operations, hard-switching and soft-switching, with 40-kW of sinusoidal AC output power. Efficiency measured with the hard-switching operation was 95.12%, and that with the soft-switching operation was 95.95%. Improvement is 0.83%.

(a) With the soft-switching operation only

(b) With the soft-switching and the hard-switching operations together

Figure 4-33. Output voltage and current waveforms of the AC sinusoidal output test
4.6 Conclusion

In this chapter, a PEBB-based three-level leg is designed and tested. The issues of the PEBB leg design include implementation of the soft-switching technique, reduction of voltage spikes with hard-switching, and results of a mixture of hard-switching and soft-switching techniques.

The soft-switching circuits for each of the switches on the PEBB leg are designed and tested. For the discharging mode, the circuit configuration and its operations are nearly the same as those of the basic boost converter case. However, those of the charging mode are different, due to the presence of the neutral point clamping diode, which forms a freewheeling path that prevents the current dropping from the main switch. Even though the ZCT cannot be achieved during the turn-off of the main switch, the voltage across the switch can be maintained at a low point until the resonance finishes, except during a short period when the anti-parallel diode of the opposite side main switch is turned on. This results in nearly the same effectiveness as a complete ZCT on the main switch.

A new soft-switching circuit for the chopper leg is suggested that can have one auxiliary switch per one main switch. Direct modification of the PEBB leg with the soft-switching technique requires two auxiliary switches for the inner main switch. This new method can remove the extra auxiliary switch by moving the connection of the resonant tank directly to the output.

Due to the duty cycle limitation of the soft-switching technique, the small duty cycle portion of the PWM cannot operate with the soft-switching technique. This part can operate using the hard-switching technique. With the hard-switching technique, the voltage spikes during the charging mode become much higher than that during the discharging mode. This is caused by the parasitic inductance associated with each the operation modes. The parasitic inductance can be reduced effectively by using a laminated bus. With the laminated bus, one third of the voltage spikes during the charging mode is reduced. Smooth sinusoidal output is obtained with the PEBB leg by using both soft- and hard-switching technique.
Chapter 5  The Voltage Source Converter

With the completed PEBB leg, the new PCS can be built by using the PEBB legs. The chopper can be built using two of them, and VSC can be built using three of them. Since all of the high-speed switching related issues are solved at the PEBB leg, the system can be built assembling the PEBB legs, and the system-related issues are only for low-speed input and output. In this chapter, the issues on the VSC are focused. The VSC can be built using three PEBB legs. To get the desired output voltage and/or current from the VSC, appropriate modulation method and a controller to get the desired output are needed. To design the controller, the power stage transfer function should be known and the state variables need to be measured. The transfer function can be obtained using modeling of the power stage and can be verified by comparing to the measured values. The state variables can be measured by sensors.

5.1 Space Vector Modulation

Among various three-phase modulation schemes, the space vector modulation (SVM) method is the state-of-the-art modulation method used for this work. Three-phase PWM signal generation is based on the SVM and implemented with an electrically programmable logic device (EPLD) and a digital signal processor (DSP).

5.1.1 Switch Combination

There are $2^{12}$ possible switching states for the three-level VSI shown in Figure 5-23. However, the switch combinations of $S_{i1}$ and $S_{i4}$, where $i \in \{1,2,3\}$, while $S_{i2}$ and $S_{i3}$ are turned off do not have any meaning, since they do not generate any output nor provide any current paths. However, turning on the switch combinations that turn on any three consecutive switches of one leg at the same time will cause a shoot-through of either of the input voltage sources. Turning on all four switches of one leg will result in a shoot-through of both input sources. Even though the switches are not consecutive, turn-on any combination of three switches causes over-voltage on the remaining switch. The only possible switch combinations are any two adjacent switches in a leg, as shown in Figure
Therefore, a leg can have three possible switch combinations, \( S_p \), \( S_o \), and \( S_n \) and these switches can be represented as one three-pole bi-directional switch, as shown in Figure 5-1 (d). When the switches \( S_1 \) and \( S_2 \) are turned on, the switch is connected to \( S_p \). The output voltage \( V_{out} \) becomes \( V_p \). When the switches \( S_2 \) and \( S_3 \) or \( S_3 \) and \( S_4 \) are turned on, they become \( S_o \) or \( S_n \), and \( V_o \) or \( V_n \).

With this switch representation, the three-phase three-level VSI shown in Figure 5-23 can be represented as in Figure 5-2. Since a PEBB leg can have three different voltage outputs, the total number of possible switch connections for the three-phase VSI is \( 3^3 \) which is 27. Each of the switch combinations has its own output voltage and can be mapped into a three-phase line-to-line voltage vector space as a vector. Therefore, there are 27 possible vectors for the three-level three-phase VSC, and these vectors need to be identified. For example, if \( S_a \) connects to \( p \), \( S_b \) connects to \( o \), and \( S_c \) connects to \( n \), then this switch combination can be expressed \( pon \). The three-phase line-to-line voltages of the \( pon \) switch combination becomes \( V_{ab} = \frac{1}{2}Vs \), \( V_{bc} = \frac{1}{2}Vs \), and \( V_{ca} = -Vs \).

![Figure 5-1. Three possible switch combinations of the PEBB leg](image-url)
5.1.2 Vector Representation

Each of the vectors can be classified into one of four different vector groups according to its size: large, medium, small, and zero. The large vectors are the vectors that all of the three switches are connected to either $V_p$ or $V_n$, as shown in Figure 5-3(a), except in the case when all of them are connected to the same point. There are only six large vectors: $pnn$, $ppn$, $npn$, $npp$, $nnp$, and $pnp$. The medium vectors are the ones that have only one phase connected at $V_o$, and the other two switches connected to $V_p$ and $V_n$, as shown in Figure 5-3 (b). These are also six medium vectors: $pon$, $opn$, $npo$, $nop$, $onp$, and $pno$. The small vectors are those vectors that have two switches connected to the same point; the remaining one is connected to another adjacent point as shown in Figure 5-4. There are twelve small vectors: $ppo$, $oon$, $opo$, $non$, $opp$, $noo$, $oop$, $nno$, $pop$, $ono$, $poo$, and $onn$. The zero vectors are the vectors that have all three switches connected to one same point: $ppp$, $ooo$, and $nnn$. The zero vectors do not have any output voltage. Figure 5-5 shows 19 of the possible vectors and 27 switch combinations.
Figure 5-3. One set of large and medium vectors
Figure 5-4. One set of small vectors, *poo* and *onn*. 
5.1.3 Synthesis of Rotating Vector

The three-phase output of the VSC can be represented with a phasor that is a rotating vector, and synthesized with combinations of the vectors within a switching cycle. However, not all of the combinations have the same results. Harmonic distortions of the output voltage, amounts of ripple of the output current, and the number of switching will be strongly dependent on the method of modulation. Among those modulations that can generate the same three-phase output, one of the simplest and most efficient methods that can generate small current ripples and small harmonic distortions on the output is one that...
uses the combinations of the nearest vectors. Implementation of the nearest vector modulation method can be explained as follows.

The vectors shown in Figure 5-5 can be divided into six equal triangle sections. Each triangle section has two large vectors and two small vectors at its end and a medium vector between them, as shown in Figure 5-6.

The magnitude of the large vectors, in terms of the input voltage, is $\frac{2V_i}{\sqrt{3}}$. That of the small vectors is half of that figure. The magnitude of the medium vector is equal to $V_i$, which is the same as the radius of a circle inscribed into the large hexagon shown in Figure 5-5. Therefore, the maximum amplitude of undistorted output line voltage is $V_i$. The desired output line-to-line voltage vector in steady-state can be represented as:

\[ V = dm V_i e^{j\omega t}, \]

where $dm$ is the modulation index with a range of $0 \leq dm \leq 1$, and $\omega$ is the angle velocity of the output voltage. Therefore, the output voltage $V$ can be controlled over one switching cycle period by using the PWM of the switching vectors. Due to the large number of vectors, there is some freedom when selecting the vectors. This freedom can be used to reduce the number of switching actions and harmonic contents in the output and/or to compensate the midpoint charge to keep the midpoint potential within given limit. The harmonics can be minimized, if the switching vectors nearest to the reference vectors are selected for the PWM, because the vectors have only a minimum voltage difference.

There are six large triangles in the hexagon, as shown in Figure 5-5. For any $dm$ and $\omega$ values, the reference vector can be found inside one of the large triangles. Due to circular symmetry, operation and duty cycle calculations can be explained by using only one of the triangles, as shown in Figure 5-6.
Figure 5-6. Synthesis of the rotating phasor with the combination of adjacent vectors for \( \Delta_1 \)

To synthesize the three-phase output voltages, the phasor, which is the rotating vector \( \mathbf{v} \) as shown in Figure 5-6, needs to be identified. The length of each vector that can synthesize the phasor \( \mathbf{v} \) when it is located in \( \Delta_1 \) region can be expressed as follows:

\[
\begin{align*}
d_m \cdot e^{j\theta} &= V_s \cdot d_{Vs1} + V_m e^{j\frac{\pi}{6}} \cdot d_{Vm} + V_L \cdot d_{VL1}, \\
d_{Vs1} + d_{Vm} + d_{VL1} &= 1
\end{align*}
\]

and the solution becomes:
\[ d_{v_{s1}} = -\{\sqrt{3} \cos(\theta) + \sin(\theta)\} \cdot dm + 2 \]
\[ d_{v_m} = 2 \sin(\theta) \cdot dm \]
\[ d_{v_{L1}} = \{\sqrt{3} \cos(\theta) - \sin(\theta)\} \cdot dm - 1 \]

where \( dm = |\mathbf{v}| \), and \( \theta \) = the angle between \( \mathbf{v} \) and \( \mathbf{V}_{LI} \). The lengths correspond to the duty ratio of each vector.

Figure 5-7. Synthesis of the rotating phasor with the combination of adjacent vectors for \( \Delta_2 \).

When the phasor is located in \( \Delta_2 \) region, it can be expressed as follows:
\begin{align*}
(5-4) \quad d_m \cdot e^{j\theta} &= V_{s1} \cdot d_{v_{s1}} + V_{s2} \cdot e^{j\frac{\pi}{3}} \cdot d_{v_{s2}} + V_m \cdot e^{j\frac{\pi}{6}} \cdot d_{v_m}; \\
& \quad d_{v_{s1}} + d_{v_{s2}} + d_{v_m} = 1;
\end{align*}

and the solution becomes

\begin{align*}
(5-5) \quad d_{v_{s1}} &= -2 \cdot d_m \cdot \sin(\theta) + 1 \\
& \quad d_{v_{s2}} = \{\sin(\theta) - \sqrt{3} \cos(\theta)\} \cdot d_m + 1 \\
& \quad d_{v_m} = \{\sin(\theta) + \sqrt{3} \cos(\theta)\} \cdot d_m - 1.
\end{align*}

The region \(\Delta_3\) is a mirror of \(\Delta_1\) with respect to \(V_m\), so the duty ratios can be obtained by replacing the angle \(\theta\) with \(-\theta + \pi/3\), and \(V_{s1}\) and \(V_{L1}\) with \(V_{s2}\) and \(V_{L2}\) in equation (5-3).

![Figure 5-8. Synthesis of the rotating phasor with the combination of adjacent vectors for \(\Delta_3\)](image-url)
When it is located in $\Delta_4$ region, it can be expressed as follows:

\[
(5-6) \quad d_m \cdot e^{j\theta} = V_{s1} \cdot d_{v_{s1}} + V_{s2} \cdot e^{j\pi/3} \cdot d_{v_{s2}}; \\
 d_{v_{s1}} + d_{v_{s2}} + d_{v_c} = 1;
\]

and the solution becomes

\[
(5-7) \quad d_{v_{s1}} = -\{\sin(\theta) - \sqrt{3}\cos(\theta)\} \cdot dm \\
 d_{v_{s2}} = 2 \cdot dm \cdot \sin(\theta) \\
 d_{v_c} = -\{\sin(\theta) + \sqrt{3}\cos(\theta)\} \cdot dm + 1.
\]

Examples of one switching cycle implementation of the vectors obtained with the
The equations above are shown in Figure 5-10 (a) to (d) for $\Delta t$ to $\Delta t$.

### 5.1.4 Extraction of the Three-Phase Duty Cycle

In Figure 5-10 (a), the $poo$ vector, instead of $onn$, is selected as the $d_{vsi}$. By doing this, the phase $A$ can be connected to the $p$ input during the whole switching period. This will result in a smaller switching loss when the phase $A$ flows a large current, which is the usual case for a resistive load. The duty ratios for the phase $B$ and $C$ legs can be expressed as $d_{bi}$ and $d_{ci}$, where $i \in \{p,o,n\}$. 
Figure 5-10. Outputs of each phase during one switching cycle for each triangle

(a) For $dm = 0.8$, $\theta = 15^\circ$ in $\Delta_1$

(b) For $dm = 0.8$, $\theta = 25^\circ$ $\Delta_2$
Figure 5-10. (Continued) Outputs of each phase during one switching cycle for each triangle
When the duty ratio $dm$ is one, the phasor $\mathbf{v}$ passes through the outermost triangles. For the full power test of the three-phase VSC, the $dm$ is set to one, and the EPLD and DSP are designed according to the necessary parameters. Details of the design of the EPLD and the programming of the DSP are described in Appendix B.

5.2 Modeling

A computer model for the VSC is needed to predict system behavior and to design the compensation for the controller. The VSC can be used as a PFC rectifier when it receives power from the utility line. When the VSC returns energy back to the utility, the VSC acts as a VSI. In this section, the circuit models for the VSI and the rectifier will be discussed.

The procedure for modeling starts with a switch model for each application. As mentioned before, the three-level VSI topology can be represented with three-pole switches as shown in Figure 5-2. A topological difference between the VSI and the rectifier include the location of the power source and load. The rectifier has a three-phase voltage source and DC load instead of the $R_{VSI}$ and $V_s$ shown in Figure 5-12. The switch models are followed by average models. The models can be further simplified into large and small signal models by using coordinate transformation.

5.2.1 Switch Model

The three-level VSI topology can be represented with three pole switches as shown in Figure 5-11. The rectifier has a three-phase voltage source and a DC load instead of the $R_{VSI}$ and $V_s$ shown in Figure 5-12.
The switches shown in Figure 5-11 can be represented with a switch function defined as follows:

\[
(5-8) \quad \sum_{j \in \{p,o,n\}} S_{ij} = 1, \\
\]

where 
\[
S_{ij} = \begin{cases} 
1, & \text{if } i \text{ connected to } j, \quad i \in \{a,b,c\}, \text{ and } j \in \{p,o,n\} \\
0, & \text{else}
\end{cases}
\]

With the definition of equation (5-8), the three-phase output voltages and the two input
currents of the converter shown in Figure 5-11, using KVL and KCL for the given input voltages and the load currents, can be represented as follows:

\[(5-9) \quad v_A = S \cdot v_g, \quad i_g = S^T \cdot i_A,\]

where

\[
\begin{bmatrix}
v_{ab} \\
v_{bc} \\
v_{ca}
\end{bmatrix}, \quad \begin{bmatrix}
i_{ab} \\
i_{bc} \\
i_{ca}
\end{bmatrix} = \frac{1}{3} \begin{bmatrix}
i_a - i_b \\
i_b - i_c \\
i_c - i_a
\end{bmatrix}, \quad v_g = \begin{bmatrix} v_{po} \\ v_{no} \end{bmatrix}, \quad i_g = \begin{bmatrix} i_p \\ i_n \end{bmatrix}, \quad \text{and} \quad S =
\begin{bmatrix}
S_{ap} - S_{bp} & S_{an} - S_{bn} \\
S_{bp} - S_{cp} & S_{bn} - S_{cn} \\
S_{cp} - S_{ap} & S_{cn} - S_{an}
\end{bmatrix}.
\]

For the switch function vector \( S \), there are two methods of identification depending on the reference point of the input source. The reference point of the matrix \( S \) used above is the midpoint of the input source, which is the ‘o’ point. This point is good for the three-level topology.

The switch function vector \( S \) can be averaged over one switching cycle and replaced by the duty ratio vector as follows

\[(5-10) \quad d = \begin{bmatrix}
d_{ap} - d_{bp} & d_{an} - d_{bn} \\
d_{bp} - d_{cp} & d_{bn} - d_{cn} \\
d_{cp} - d_{ap} & d_{cn} - d_{an}
\end{bmatrix} = \begin{bmatrix} d_{abp} & d_{abn} \\ d_{bcp} & d_{bcn} \\ d_{cap} & d_{can} \end{bmatrix}.
\]

By replacing \( S \) with \( d \) in equation (5-10), equation (5-9) becomes

\[(5-11) \quad v_A = d \cdot v_g, \quad i_g = d^T \cdot i_A.
\]

With equation (5-11), the large signal state-space model of the VSI becomes

\[(5-12) \quad \frac{d}{dt} i_A = \frac{1}{3L} (d \cdot v_g - v_o),\]

\[(5-13) \quad \frac{d}{dt} v_o = \frac{3}{C} (i_A - \frac{1}{3R_{vsi}} v_o), \quad \text{and}
\]
(5-14) \[ \frac{d}{dt} v_g = \frac{1}{C_s} (i_{sdc} - d^T i_A), \]

where \( v_o = \begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} \), and \( i_{sdc} = \begin{bmatrix} i_{sdc} \\ -i_{sdc} \end{bmatrix} \).

The model of the rectifier becomes

(5-15) \[ \frac{d}{dt} i_A = \frac{1}{3L} (v_g - d \cdot v_{DC}), \]

and

(5-16) \[ \frac{d}{dt} v_{DC} = \frac{1}{C_s} (d^T i_A - i_{R_{dc}}). \]

where \( v_g = \begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} \), \( v_{DC} = \begin{bmatrix} v_{po} \\ v_{no} \end{bmatrix} \), \( i_{R_{dc}} = \begin{bmatrix} v_p - v_n \\ R_{DC} \\ v_p - v_n \end{bmatrix} \), \( C_s = C_{sp} = C_{sn} \), and \( R_{DC} = \) DC load of the rectifier.

Figure 5-13 shows the circuit model of the three-phase VSI, and Figure 5-14 shows that of the rectifier.
Figure 5-13. An average model of the three-level VSI

Figure 5-14. An averaged model of the three-level rectifier
5.2.2 Coordinate Transformation

Due to the VSI and rectifier deal with the three-phase AC source and load, equations from (5-12) to (5-16) are time-varying even in the steady state. For the modeling and control design of the AC system, rotating coordinates are much useful than stationary ones. A typical approach for the balanced three-phase VSI and rectifier modeling is a d-q transformation by using an orthonormal matrix as follows:

\[
T = \begin{bmatrix}
\cos(\omega t + \theta) & \cos\left(\frac{\omega t + \theta - 2\pi}{3}\right) & \cos\left(\frac{\omega t + \theta - 4\pi}{3}\right) \\
-\sin(\omega t + \theta) & -\sin\left(\frac{\omega t + \theta - 2\pi}{3}\right) & -\sin\left(\frac{\omega t + \theta - 4\pi}{3}\right) \\
\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}}
\end{bmatrix},
\]

where \( \omega \) = the angular speed of the rotating d-q frame, which equals to the converter output frequency, and \( \theta \) = relative angle of the d-q frame and the reference of the rotating vectors.

With the orthonormal matrix, the three-phase AC variables

\( x_3 = [x_1, x_2, x_3]^T \)

(5-18) can be transformed and inversely transformed into the rotating d-q variables as follows:

\( x_r = [x_d, x_q, x_0]^T = T \cdot x_3 \), and

\( x_3 = T^T \cdot x_r \).

(5-20) The derivative becomes

\[
\frac{d}{dt} x_3 = \frac{d}{dt} T \cdot x_r + T \cdot \frac{d}{dt} x_r.
\]

(5-21) The transformed state space model becomes

\[
\frac{d}{dt} x_r = T \cdot \frac{d}{dt} x_3 + T \cdot \frac{d}{dt} T \cdot x_r,
\]

(5-22) where
By applying the d-q transformation to the three-phase voltage and current variables, following equations are obtained:

\[\begin{align*}
\mathbf{v}_r &= T \cdot \mathbf{v}_\Delta, \quad \mathbf{i}_r = T \cdot \mathbf{i}_\Delta, \quad \mathbf{d}_r = T \cdot \mathbf{d}, \quad \mathbf{d}_r^T = d^T \cdot T^T; \\
\mathbf{v}_r &= \mathbf{d}_r \cdot \mathbf{v}_g, \quad \mathbf{i}_g = d^T \cdot \mathbf{i}_r,
\end{align*}\]

where \(\mathbf{v}_r = \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix}, \quad \mathbf{i}_r = \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix}, \quad \mathbf{d}_r = \begin{bmatrix} d_{dp} & d_{dn} \\ d_{qp} & d_{qn} \\ d_{0p} & d_{0n} \end{bmatrix}.\)

### 5.2.3 The Large Signal Model

By applying the equation (5-21) to the equations from (5-12) to (5-16), large-signal state-space models for the VSI and rectifier becomes

\[\begin{align*}
\frac{d}{dt} \mathbf{i}_r &= \frac{1}{3L} (\mathbf{d}_r \cdot \mathbf{v}_g - \mathbf{v}_{or}) - T \cdot \frac{d}{dt} T^T \cdot \mathbf{i}_r, \\
\frac{d}{dt} \mathbf{v}_{or} &= \frac{3}{C} (\mathbf{i}_r - \frac{1}{3R_{vi}} \cdot \mathbf{v}_{or}) - T \cdot \frac{d}{dt} T^T \cdot \mathbf{v}_{or}, \quad \text{and} \\
\frac{d}{dt} \mathbf{v}_g &= \frac{1}{C_s} (i_{sde} - \mathbf{d}_r^T \cdot \mathbf{i}_r),
\end{align*}\]

where \(\mathbf{v}_{or} = T \cdot \mathbf{v}_o = [v_{od}, v_{oq}, v_{oo}]^T.\)

The transformed model of the rectifier becomes

\[\begin{align*}
\frac{d}{dt} \mathbf{i}_r &= \frac{1}{3L} (\mathbf{v}_{gr} - \mathbf{d}_r \cdot \mathbf{v}_{DC}) - T \cdot \frac{d}{dt} T^T \cdot \mathbf{i}_r, \quad \text{and} \\
\frac{d}{dt} \mathbf{v}_{DC} &= \frac{1}{C_s} (\mathbf{d}_r^T \cdot \mathbf{i}_r - i_{Rdc}).
\end{align*}\]

Figure 5-15 and Figure 5-16 show an average d-q models based on this transformation.
Figure 5-15. An average d-q model of the three-level VSI

Figure 5-16. An average d-q model of the three-level rectifier
The state variables can be replaced with the steady-state ones with upper case letters. By choosing all of the derivatives of the state variables in the equations from (5-26) to (5-30) as zero, the steady state equations for the VSI can be obtained as follows:

\[(5-31) \quad D_{rdi} = \frac{V_{ord} \cdot R_{VSI} - \omega_r \cdot L \cdot V_{orq} - \omega_r^2 \cdot L \cdot V_{ord} \cdot C \cdot R_{VSI}}{V_{gi} \cdot R_{VSI}};\]

\[(5-32) \quad D_{rqi} = \frac{V_{orq} \cdot R_{VSI} + \omega_r \cdot L \cdot V_{ord} - \omega_r^2 \cdot L \cdot V_{orq} \cdot C \cdot R_{VSI}}{V_{gi} \cdot R_{VSI}};\]

\[(5-33) \quad I_{rd} = \frac{1}{3 \cdot R_{VSI}} (V_{ord} - \omega_r \cdot V_{orq} \cdot C \cdot R_{VSI});\]

\[(5-34) \quad I_{rq} = \frac{1}{3 \cdot R_{VSI}} (V_{orq} + \omega_r \cdot V_{ord} \cdot C \cdot R_{VSI});\]

\[(5-35) \quad I_{sdc} = \frac{V_{ord}^2 + V_{orq}^2}{3 \cdot V_{gp} \cdot R_{VSI}} = -\frac{V_{ord}^2 + V_{orq}^2}{3 \cdot V_{gn} \cdot R_{VSI}},\]

where \(i \in \{p,n\}\).

Followings are the equations for the rectifier with the additional conditions of \(I_{rqi} = 0\) and \(V_{DC} = 2 \cdot I_{Rdc} \cdot R_{DC}:

\[(5-36) \quad D_{rdi} = \frac{V_{ord}}{V_{DCi}};\]

\[(5-37) \quad D_{rqi} = \frac{2 \cdot V_{ord} \cdot R_{DC} \cdot V_{orq} - 3 \cdot \omega_r \cdot L \cdot V_{DCi}^2}{2 \cdot V_{DCi} \cdot V_{ord} \cdot R_{DC}};\]

\[(5-38) \quad I_{rdi} = \frac{V_{DCi}^2}{2 \cdot V_{ord} \cdot R_{DC}},\]

where \(V_{DCp} = V_p\), and \(V_{DCn} = V_n\).
5.2.4 The Small-Signal Model

The small signal models of the VSI can be derived by the perturbations and linearizations of the variables for the large-signal models at a given steady-state operating point. The small-signal model can be derived with the perturbation of those variables as follows:

\[(5-39) \ x = X + \tilde{x},\]

where \(X\) denotes the steady state value and \(\tilde{x}\) denotes the perturbation. In addition to the perturbation, the linear approximation can be achieved by ignoring the non-linear terms as follows:

\[(5-40) \ xy = (X + \tilde{x})(Y + \tilde{y}) \approx XY + X\tilde{y} + Y\tilde{x}.\]

Figure 5-17 and Figure 5-18 show the small-signal models of the VSI and rectifier. Equations (5-41) and (5-42) show the small-signal state-space model.

Figure 5-17. An average small signal d-q model for the three-level VSI
Figure 5-18. An averaged small signal d-q model for the three-level rectifier
\[
\begin{bmatrix}
\frac{V_p}{3L} & \frac{V_n}{3L} & 0 & 0 & 0 \\
0 & 0 & \frac{V_p}{3L} & \frac{V_n}{3L} & 0 \\
0 & 0 & 0 & 0 & 0 \\
-\frac{I_d}{Cs} & 0 & -\frac{I_d}{Cs} & 0 & 1 \\
0 & -\frac{I_d}{Cs} & 0 & -\frac{I_q}{Cs} & -1 \\
\end{bmatrix}
+ 
\begin{bmatrix}
\tilde{d}_{dp} \\
\tilde{d}_{dn} \\
\tilde{d}_{ap} \\
\tilde{d}_{aq} \\
\tilde{i}_{ad} \\
\end{bmatrix}
\]

\[
(5.42) 
\frac{d}{dt} \begin{bmatrix}
\tilde{i}_d \\
\tilde{i}_q \\
\tilde{v}_p \\
\tilde{v}_n \\
\end{bmatrix} = 
\begin{bmatrix}
0 & \omega_r & -\frac{D_{dp}}{3L} & -\frac{D_{dn}}{3L} \\
-\omega_r & 0 & -\frac{D_{ap}}{3L} & -\frac{D_{aq}}{3L} \\
\frac{D_{dp}}{Cs} & \frac{D_{ap}}{Cs} & 1 & 1 \\
\frac{D_{dn}}{Cs} & \frac{D_{aq}}{Cs} & CR_{VSI} & CR_{VSI} \end{bmatrix}
\begin{bmatrix}
\tilde{i}_d \\
\tilde{i}_q \\
\tilde{v}_p \\
\tilde{v}_n \\
\end{bmatrix}
\]

5.2.5 Power Stage Transfer Functions

The transfer functions of the VSI are obtained by the simulation of the circuit, as shown in Figure 5-17, and simulation of the rectifier as from Figure 5-18. The parameters used for the VSI are as follows:

D channel output voltage \(V_d\) \(1100\text{-V};\)

Q channel output voltage \(V_q\) \(0\text{-V};\)

\(\omega\) \(2\pi \cdot 60;\)
\[ R_{\text{VSI}} = 7.3-\Omega; \]
\[ L = 600-\text{uH}; \]
\[ C = 10-\text{uF}; \]
\[ V_g = 1800-\text{V}; \]
\[ C_p = 1200-\text{uF}; \text{ and} \]
\[ C_n = 1200-\text{uF}. \]

The parameters used for the rectifier are as follows:

\[ V_{od} = 480-\text{V}; \]
\[ V_{oj} = 0-\text{V}; \]
\[ V_{DCI} = 1800-\text{V}; \text{ and} \]
\[ R_{\text{DC}} = 13-\Omega. \]

The simulations are done with two different values of the positive and the negative duty ratios, \( D_{(dq)\text{p}}, \) and \( D_{(dq)\text{n}}. \) The difference of the two values results in the current flow through the midpoint. The \( pnn \) vector component, which is not connected to the midpoint, does not show any difference between the two duty ratios. In this case, the two values can be \( D_{(dq)\text{p}} = -D_{(dq)\text{n}}. \) The capacitors \( C_p \) and \( C_n \) do not affect to the circuit. Therefore, the input source can be replaced with a voltage source. The transfer functions of the three-level VSI and rectifier do not show any difference from those of two-level VSIs and rectifiers. However, the medium vector, \( pon, \) and the small vector, \( poo, \) flow current through the midpoint. In the worst case, the two values can be \( D_{(dq)\text{p}} = D_{(dq)\text{n}}, \) and the capacitors \( C_p \) and \( C_n \) can be added together without any input source.

The calculated values of the operating points of the equations from (5-31) to (5-38) are as follows:

\[ D_d = 1, D_q = 0.031, I_{rd} = 82-\text{A}, I_{r}\bar{q} = 0.679, \text{ for the VSI; and} \]
\[ D_d = 0.267, D_q = -0.069, I_{di} = 183.576, \text{ for the rectifier.} \]

Figure 5-19 shows the simulated transfer functions of the three-level VSI and rectifiers with the input voltage source, and Figure 5-20 shows those of the VSI with the two
capacitors, $C_p$ and $C_n$. The gain and phase of the two cases change the transfer functions in frequency less than 30-Hz.

Figure 5-19. The voltage transfer functions of the three-level VSI with the input voltage source.
Figure 5-20. The voltage transfer functions of the three-level VSI with the capacitor input

(a) $V_{d/dd}$

(b) $V_{g/dd}$
5.3 Closed-Loop Control

The system dynamic range that actually determines the speed of the PCS is determined by the loop gain of its controller. The wider the gain, the faster the speed of the PCS. However, the maximum limit of the dynamic range is limited by its switching frequency and should be sufficiently less than that to eliminate switching noise from the power stage. In this section, the ability of the closed-loop controller to make the PCS system stable is investigated.

Figure 5-21 shows the block diagram of the control loop for the VSC. The loop consists of sensors, a controller, and a power stage through the SVM. The command for the loop is given through the reference input. The controller should be able to control the PCS in various operating conditions and during required functions. Basic functions of the PCS include the charging and discharging of the SMES coil. To charge/discharge the SMES coil, the VSC should be able to receive/provide energy from/to utility line. When the SMES coil needs to be charged, the VSC needs to be a rectifier. The rectifier should be able to operate with power factor correction (PFC). When the SMES coil needs to be discharged, on the other hand, the VSC needs to be an utility inverter that provides energy back to the utility. The PCS can also be used as a stand-alone system when the load is separated from the utility. In this case, the VSC needs to provide a desired voltage to the load. The power stage of the VSC developed in this research can do all of the above functions. Different roles of the VSC can be accomplished by changing the configuration and parameters of the controller. When the VSC is used as a rectifier, the control object is the three-phase line currents that need to be synchronized with the three-phase voltage. For the utility inverter the control object is also the line current. The difference between this mode and the rectifier mode is the direction of the input currents, which are opposite to each other. For the VSI, the control object is the output voltage. In this case, the controller should not do anything for the current except limit its value within the maximum allowed for safe operation to protect the VSC from damage.
In this section, each of the items within the control loop - sensors, controller, and power stage transfer function - are explained, except the SVM shown in Figure 5-21 which is already explained in Section 5.1.

### 5.4 Controller

A controller that can be used for the VSI, rectifier, and utility inverter has the structure shown in Figure 5-22. The controller is designed and implemented by other works. In this section, the structure of proportional and integral (PI) type compensator is briefly reviewed.

The controller has three functions, DQ transformation, compensation, and inverse DQ transformation. The sensed three-phase AC voltage and current information are transformed into the DQ coordinate. The DQ signals are subtracted from the reference values that make error signals. Objective of the compensator is to get desired loop gain.
characteristics that determines the speed of the VSC. Desired loop gain characteristic for VSC needs to have pole at origin for tight regulation of output for given reference signals. The presence of double pole at the transfer function requires one zero compensator at the same frequency. To get the desired characteristics, the compensator should have one integrator and one proportional gain buffer as shown in Figure 5-22. The value $K_p$ is for proportional gain and $K_i$ is for integral gain. The controller is implemented with 32-bit digital signal processor (DSP).

Figure 5-22. Block diagram of control loop
5.5  Experiment

5.5.1  System Integration

Five PEBB legs are built and each of them is tested successfully. Two of the legs are used to build the chopper in other work, and three of them are used for voltage source converter (VSC), as shown in Figure 5-23. The chopper and VSC are installed in a double-bay frame to make a complete SMES-PCS test system. Installation includes all required plumbing for water-cooling. Figure 5-24 shows a constructed power stage of the SMES PCS proof-of-concept test system. The left side of the rack contains the VSC and the right side is the chopper. System-level tests are performed with this system.

Three of the PEBB legs are connected to each other in a side-by-side configuration through the DC link. Since the PEBB legs are fully tested individually, the test of the three-phase VSC can concentrate on testing the three-phase modulation. According to the applications of the SMES PCS, the VSC can be used as a voltage source inverter (VSI), a rectifier, and a utility inverter. For example, when the PCS is used as a black starter, it needs to be a VSI. When the PCS charges the SMES coil, it needs to be a rectifier. When the PCS needs to return the stored energy in the SMES coil back to the utility, it needs to be a utility inverter. The difference between the VSI and the utility inverter is that the VSI needs to control the output voltage while the utility inverter needs to control current. All three functions of the VSC are based on a three-phase operation. In this chapter, details of the three-phase operation are discussed.
Figure 5-23. The three-level three-phase VSI

Figure 5-24. The complete power stage of the three-level SMES PCS test system
5.5.2 Three-Phase Open Loop Test

5.5.2.1 Three-Phase Output

The first test of the three-phase VSC is performed with an open loop. The purpose of the open-loop test is to verify the operation of the SVM. Therefore, the VSC is tested by operating as a VSI with the SVM. Figure 5-25 shows the test setup. Two 900-V DC power supplies are connected in series to provide positive and negative voltage. The midpoint of the power supplies connected in is also connected to the midpoint of the three-level inverter. The output of the VSC is connected to a three-phase Y connected resistor load bank. The digital logic and DSP are programmed to generate the desired SVM. The gate drive signals are provided through optical links to each of the main and the auxiliary switches. Figure 5-26 shows the three-phase output phase voltage waveforms $V_{AN}$, $V_{BN}$, and $V_{CN}$. The voltage waveforms are nearly the same as that of the phase currents in this case, because of the small load resistance compared to the impedance of the filter capacitors. Glitches are noticed at the zero crossing of a phase current. The glitches are caused by the current shift of the filter inductor that makes lagging current. Figure 5-27 shows three-phase line-to-line output waveforms. White dotted lines are placed there deliberately to show the average values of each voltage. Each of the waveforms shows five levels of voltage, as expected.
Figure 5-25. Test setup for the three-phase VSC
Figure 5-26. Three-phase output phase voltage $V_{AN}$, $V_{BN}$, and $V_{CN}$

Figure 5-27. Three-phase output line-to-line voltage $V_{ab}$, $V_{bc}$, and $V_{ca}$
5.5.2.2 Efficiency Measurement

Efficiencies are measured throughout power ranges of 20-kW up to 98-kW using soft-switching techniques due to the limitations of the input power source, and up to 60-kW using hard-switching techniques due to safety reasons. Figure 5-28 shows the measurements using soft- and hard-switching techniques. The measurements show that the efficiency improvements are negligible and efficiency fails with soft-switching operation. This can be explained as follows.

For low power, the circulating energy of the resonance action for the soft-switching operation that is tuned for the maximum power level increases loss. Higher efficiency, around the 40-kW area shown in Figure 5-28, could be caused by this effect.

For high power, a three-phase SVM operation eliminates the switching of the highest current leg for a 60°-120° area. The average value of the current in this area is half of the whole current. The remaining phase current which is switched provides the other half of the value. The two halves of the switching portions are added together. Therefore, the amount of the switching loss of the three-phase SVM is the same as that of single phase operation. However, the conduction loss of the three-phase SVM is three times larger than that. Another aspect of the soft-switching technique is that the resonant peak current is proportional to the DC link voltage and is designed for 900-V. However, in this test, the maximum DC link voltage on one side is 500-V, reducing the peak resonant current to about 56%. This leads to a lower maximum load current that can be soft-switched. All of these could be the causes of the lower efficiency difference around the 60-kW area.
5.5.2.3 Harmonics Measurement

Figure 5-29 shows the measurements of the harmonic contents of the output voltage and current. All of the harmonics are within 1.1%. Total harmonic distortions measured are 1.3% for $V_{ab}$ and $I_b$, and 1.5% for $V_{ac}$ and $I_c$. Figure 5-30 shows expected improvements of the harmonic content on the three-level PWM VSI output, compared to that of the systems using thyristors based on six-pulse operations.
Figure 5-29. Harmonics measurement results
Figure 5-30. Comparison of the harmonics with the system based on six-pulse operations
5.5.3 Sensors

Sensors are needed to get voltage and current information from the power stage. Since the VSC has to deal with so high a voltage and current, the sensors have to provide sufficient isolation between the power stage and controller. In addition to that, the sensor should provide highly accurate data paths from the power stage to the controller, while simultaneously isolating noise from the power stage. These two conditions somehow contradict each other. Therefore, compromises have to be made.

The inverter needs five voltage sensors for three AC and two DC voltages. The voltage sensors are supplemented with a hole-effect voltage sensor that provides galvanic isolation. The isolation is provided by a transformer that has sensing winding at the primary side and compensation winding at the secondary side. To enable a voltage to be measured, a current proportional to the measured voltage must be collected through an external resistor connected in series with the primary circuit of the sensor. Figure 5-31 shows the circuit diagram of the voltage sensor.

![Figure 5-31. Voltage sensing circuit](image)

The VSC needs two current sensors for AC currents. The operation principle is nearly the same as that of the voltage sensor except on the primary side. The current to be sensed needs to be provided through a hole on the sensor. Figure 5-32 shows the circuit diagram of the current sensor.
The sensors not only pick up measurements but also the noise of the power stage. To eliminate the noise and get the desired data, the sensing circuits must filter noise. Generally, low-pass filters are used to eliminate any noise which has much higher frequency than that of the measured signal. Usually, the low-pass filter with/without a common mode (CM) choke is implemented with capacitors at various points of the sensor circuit, as shown in Figure 5-31. However, the capacitor at the sensor circuit changes the transfer function of the sensor. Therefore, careful use of the capacitor is recommended.

The transfer function of the original sensor is nearly flat from 10-Hz to 10-kHz except for a 7dB peak around 20-kHz. When the CM choke is inserted between the voltage sensor and series resistor, a peak near 18-kHz ( +8 dB, -70°) is noticed. When a 43-kΩ resistor is used for the \( R_a \), the gain becomes flat until 10-kHz with -38° phase shift. When an 820-pF capacitor is used as the \( C_I \), a peak shows up at 9-kHz (+4.2dB -47°). When the resistor is reduced further, the gain and phase slopes become more flat. When 0.1-μF is used as \( C_o \), the gain becomes flat until 10-kHz, but the phase becomes -45°. When \( Ra = 43\text{-}k\Omega \), \( C_I = 820\text{-}pF \), and \( Co = 0.1\text{-}μF \), the gain has a peak at 8.3-kHz (+3.8dB -90°).

Figure 5-33 shows the gain and phase angles of the voltage sensor in various \( Ra \) and \( Rb \) cases, and with/without \( Co \) cases.
Figure 5-33. Gain and phase plots of the voltage sensor with different R and C values

Following are the conditions for the gain phase measurement.

G₀: Original Configuration

G₁: \( C₀ \ 0.1\mu F \)

G₂: \( Rₐ \ 100-KΩ \)

G₃: \( Rₐ \ 100-KΩ \) with \( C₀ \ 0.1\mu F \)
$G_4$: $R_a$ 10-KΩ

$G_5$: $R_b$ 10-KΩ

$G_6$: $R_b$ 1-KΩ

$G_7$: $R_a$ 1-KΩ

As shown in the graph, the $G_3$ case shows the best result, and the sensor low-pass filter is finalized with the values.

The transfer function of the current sensor is difficult to measure, due to lack of the excitation method of the input current. However, 0.1-$\mu$F of $C_o$ is helpful, as in the voltage sensor.

Figure 5-34 and Figure 5-35 show AC voltage waveforms measured directly by a scope and a voltage sensor. Considering the voltage scale of the scope, sensed voltage shows a high S/N ratio.
Figure 5-34. An output voltage waveform measured with a scope

Figure 5-35. An output waveform measured with the voltage sensor
5.5.4 The Transfer Function Measurements

The control loop of the VSC includes various functions such as DQ transformation and SVM. This means that the transfer function obtained with the modeling of the power stage is not sufficient. Correct transfer function of the system is essential for the design of the compensator. Therefore, the transfer function needs to be measured with the actual system. Measurement of the transfer functions is done with an impedance analyzer. A signal output from the impedance analyzer is used as a perturbation for the controller. Figure 5-36 shows the measurement setup. There are two signal inputs on the analyzer. One is a reference signal input, and the other is a measurement signal input. The two signals are compared to measure the difference in terms of magnitude and phase. Therefore, the two input points are determined according to the transfer function measured.

A duty ratio input perturbed with the output from the analyzer is added to a pre-set duty value, and this perturbed duty value is changed into the three-phase SVM duty ratios by an inverse DQ and fed into the VSC switches. The reactions of the power stage for the SVM are picked up by sensors. The output voltages and currents from the sensors are fed into the ADC channels. The data from the ADC channels are changed back to the DQ coordinate, and compared with the pre-set values. In this way, the measured data includes all other factors such as sensors, ADC, DAC, etc. The ADC chip has 20-MSPS and it is designed to operate continuously by itself. However, the data from the ADC are latched into the EPLD every 20-kHz, resulting in a sampling delay. Figure 5-37 shows a measured $V_{d}/d_{d}$ transfer function of the VSI. The shape of the transfer function is not much different from that of the simulated one, but the phase delay shows large differences.
Figure 5-36. Measurement setup for the transfer function

Figure 5-37. The measured VSI transfer function of $V_d/d_d$
5.5.5 The Closed-Loop Test

The VSC is completed by closing the control loop. With the controller, the VSC can be used as an inverter, a rectifier, and an utility inverter. Figure 5-38 shows the loop gain, $T_{V_{d}}$, of the inverter. The loop gain shows a crossover frequency of 600-Hz, with 8-dB of gain margin and 60° of phase margin. Figure 5-39 shows the step response. The waveform shows the step change of the duty ratio from 0.7 to 0.9. Thanks to the high-switching frequency and wide bandwidth of the control loop, the inverter can respond within 400-μsec for the step change of the command.
Figure 5-38. A measured loop gain $T_{v_d}$ of the VSI

Figure 5-39. Measured step response of the VSI with the loop gain
5.6 Conclusion

The power stage of the three-level chopper-VSC type SMES PCS is built with five PEBB legs. This research concentrates on implementation and testing of the three-phase VSC. The three-phase AC is implemented with a three-level SVM that has large, medium, and small vectors. A SVM algorithm that can reduce the number of switching actions and output current ripples is selected and implemented.

The efficiency measurement does not show large improvement using soft-switching techniques compared to the AC test result of the PEBB leg. This is due to the switching loss portion of the three-phase SVM on the VSC becoming smaller than that of a one phase AC on a PEBB leg. The harmonic distortion improvement shows around one percent.

Closed-loop control of the VSC is implemented with DQ transformation, a PI controller, and an inverse DQ transformation followed by a SVM, power stage, and sensors. Computer models of the power stage are developed for two different applications, the VSI and the rectifier. The transfer function of the VSI is compared with the measurement. The two agree on magnitude but not on phase, due to the delay introduced by measurements.

Measurements of voltages and currents are made with isolated hall effect sensors. Efforts are made to prevent noise being introduced into the controller.

The compensator for the three-phase VSI is implemented with the PI controller. The closed-loop gain measurement of the VSI shows –20dB/dec with a crossover frequency of 600-Hz, with 8-dB of gain margin and 60° of phase margin, which makes a step response time of 400-μsec from the step change of the command to the output voltage.
Chapter 6  Extension of the Multi-Level Converter

To achieve high-speed switching, the NPC-type three-level topology uses four IGBTs and two clamping diodes. All of them need to be high speed, which contributes to the system’s expense. Meanwhile, not all of the devices within a leg are switched for a specific operation period. This could lead to a reduction of high-speed switches by replacing some parts with slow-speed devices. In this research, a new leg structure for the multi-level topology is proposed that can reduce the number of high-speed switches by replacing some high-speed switches with slow-speed ones.

It is clear that a two-level leg selects one of the input voltage levels and connects it to the output, making two inputs and one output. Since a multi-level leg is a set of two-level legs connected in series, simply by placing a two-level leg at the each level of the multi-level voltage source, the amount of output is less than the amount of input. Assuming that all of the two-level legs are switched to the same direction, the number of levels can be reduced by one at its output. Iterative use of this method results in one output line. This new structure performs the same function as that of the NPC topology. The biggest advantage of this structure becomes clear when the leg is operated with a high frequency PWM that usually requires high-speed switches. For the PWM, this structure uses only one set of high-speed switches in a two-level leg that is connected to an output line. All other switches can be replaced with slow-speed ones, such as SCRs or GTOs. By selecting appropriate gating signals between high- and slow-speed switches, the slow-speed switches can be switched with zero current.

6.1 Structure of the New Leg

Figure 6-1(a) shows a new three-level leg and (b) shows its equivalent switch representation. The main idea of the topology is a level reduction by using two-level legs. The new leg can be decomposed into three two-level legs, as shown in Figure 6-2.
Three of the input levels can also be divided into two two-level inputs. When the two-level legs are connected to each of the inputs, the outputs of the two-level legs make another two-level leg. The two output terminals can have four different voltages, $V_1-V_3$, $V_1-V_2$, $V_2-V_3$, and zero, when the two switches, $S_1$ and $S_2$, are connected to $S_{1p}$ and $S_{2n}$, $S_{1p}$ and $S_{2p}$, $S_{1n}$ and $S_{2n}$, and $S_{1n}$ and $S_{2p}$ respectively. In this case, when the input voltage sources are divided equally, $V_1-V_2$, $V_2-V_3$ become the same, which are $S_{1p}$ and $S_{2p}$, $S_{1n}$ and $S_{2n}$ cases, meaning all the switches move to the same polarity. The voltage difference...
between two terminals does not change and becomes $\frac{1}{2}(V_1-V_3)$, and another two-level leg can be attached to these outputs, as shown in Figure 6-2. By doing this, the output of the last two-level leg can make a final three-level output, and the voltage stress of the switches never exceeds the divided amount.

The leg shown in Figure 6-1 can be called a three-level cascade switch leg. A higher number of levels can be obtained by expanding this method. By generalizing the number of levels to $n$, the $n$-level cascade switch leg shown in Figure 6-9 can be obtained. The total number of switches needed is $n(n-1)$ for a $n$-level leg. Since the three-level leg is the simplest one, the operation stages of the new topology can be accomplished with the three-level leg, as shown in Figure 6-3.

6.2 Operational Stages

6.2.1 PWM Operation

The leg can be operated in two different modes as in the NPC type multi-level topology. The two modes can be operated with the PWM by switching the final two-level leg that is $S_{21p,n}$, shown in Figure 6-1. This final two-level leg can be called the PWM leg. All other two-level legs before the PWM leg can be kept still without switching during one switching cycle of the PWM operation of the final leg. Therefore, these legs can be called steady legs. The switching frequency of the steady leg depends on the output frequency of the converter, while that of the PWM leg depends on the frequency of the PWM. Below is a detailed explanation of the two mode operations. Figure 6-3 shows the two mode operations.

During the positive discharging mode, shown in Figure 6-3, the switches $S_{11p}$ and $S_{12n}$ are kept turned on. The PWM operation is performed by the switch $S_{21p}$ that makes the output voltage $V_p$ when it is turned on and $V_o$ when it is turned off. The load current will flow through the solid lines in Figure 6-3 when $S_{21p}$ is turned on, and flow through the dotted lines when it is turned off. In this mode, the PWM operation is performed by the PWM leg only, and the steady leg switches are not switched at all. For levels higher than three, the steady legs could be switched more than one time during one output cycle, but not as much as the PWM leg. The operations of the other modes are similar to that of the
positive discharging mode, except for changes of the switch states of $S_{11}$ and $S_{12}$. The amount of switching for each leg is the same throughout the different modes of operation.

Figure 6-3. Current paths for two different modes of operation

6.2.2 Soft-Switching Operation

When more than one switch is connected in series and switched at the same time, it is possible to concentrate the switching stress on one switch by making a specific switch turn off first and turn on later. This principle can be applied to this topology also. By making the PWM leg switch first and last, the other leg can be switched softly. Figure 6-5 shows four different operational modes of soft-switching operation and their timing.
diagrams.

(a) – $t_0$

Up to $t_0$, the PWM operation is performed by the high-speed switch pair $S_{21p}$ and $S_{21n}$. At $t_0$, $S_{21p}$ is turned off as part of the PWM operation. The switch $S_{11p}$ can be turned off, too. At this moment, the $S_{11p}$ does not flow current, because the $S_{21p}$ already turned off.

(b) $t_0 – t_1$

During this time, the load current flows through $S_{12p}$ and the anti-parallel diode of $S_{21n}$. The switch $S_{11p}$ starts to recover. The length of this period has to be more than the recovery time of the $S_{11p}$.

(c) $t_1$

The switch $S_{21p}$ is turned on again at $t_1$, and the switch $S_{12p}$ is turned off with no voltage. At this time, the switch $S_{11n}$ can be turned on, but no current flows through it.
Figure 6-4. Operational modes of soft-switching technique
During this time, the load current flows through the anti-parallel diode of $S_{11n}$. Therefore, the switch $S_{12p}$ also starts to recover. The length of this period has to be more than the recovery time of the $S_{12p}$, as well. At this time, the switch $S_{12n}$ can be turned on, but no current flows through it.

(e) $t_2 - t_3$

At $t_2$, the PWM switch $S_{21p}$ is turned off. The current will flow through the anti-parallel diode of $S_{12n}$. At $t_3$, the soft switching of the low speed switches finishes.

(f) $t_3 -$

From this time on, normal PWM operation can be started with negative voltage output.
6.3 Simulation Results

A simulation is done with Saber circuit simulation software using a three-level leg model. For the simulation, SCR models are used for the slow-speed switches and ideal switch models are used for the high-speed switches. The load is a series connection of a 1500-uH inductor and a 1-Ω resistor. The input voltage sources are two 900-V, and load current is 500-A peak. Figure 6-6 shows the output voltage and current of a three-level leg.
Figure 6-6. Simulation results of a three-level cascade leg
6.4 The Structure of the New Leg for the Chopper

The multi-level cascade leg topology shown in Figure 6-9 can also be applied to the chopper. Since the chopper has a two-quadrant operation, the switches for the quadrants which are not used can be eliminated. Figure 6-7 shows a set of three-level cascade chopper legs. Figure 6-7(a) shows the chopper leg for the quadrants with positive current, and Figure 6-7(b) shows those for the negative current. When the two legs are used together, as shown in Figure 6-8, a two-quadrant cascade leg chopper that can be used with the VSI is formed.

(a) For the positive current   (b) For the negative current

Figure 6-7. Two three-level cascade chopper legs

Figure 6-8. A three-level cascade two-quadrant chopper
6.5 Modification of the New Topology

Figure 6-9 shows one leg of the $n$-level topology. This topology can be called the $n$-level cascade leg. Even though the cascade leg can have slow-speed switches, the number of switches needed is an order of $n^2$. This number can be reduced further by using higher-voltage-rated devices.

In Figure 6-9, the number ‘$N$’, which is the number of input sources, is different from the number $n$, which is the number of input voltage levels, and the relationship between the two is $N=n-I$.

Figure 6-9. A leg of the new $n$-level cascade switch inverter
Usually a slow-speed switch such as a GTO has more than twice the voltage rating of a high-speed switch such as an IGBT. Therefore, mixing such devices together in the new topology makes the total system inefficient because the voltage rating of the slow-speed switch cannot be utilized fully. One easy method that can solve this problem is connecting more than two high-speed switches in series for each of the PWM leg switches. In this case, a voltage-sharing problem between those series connected switches arises. Here, another method is suggested that can divide the input source double of an ordinary multi-level leg. With this method, the three-level leg can be divided into two more levels, resulting in a five-level leg that is the minimum number of levels possible in this type. This topology can be called a double cascade switch leg.

Figure 6-10 shows the double cascade switch leg. The first column of the two-level legs are attached at every two divided input voltage sources from the top line to the bottom. Because of this, the number of input voltage sources has to be an even number to create corresponding odd-number levels. Another first column needs to be attached to the input lines between the first column, resulting in one less two-level leg compared to the first column. By expanding these columns until the odd-numbered column has two outputs while the even-numbered column has one, the final three output lines can be treated as a three-level input source and can be connected with a three-level cascade leg, as shown in Figure 6-1.
By doing this, the number of slow-speed high-voltage switches needed can be reduced to $\frac{1}{2}(n+1)(n-3)$. The number of slow-speed low-voltage switches needed is four. Figure 6-11 shows a five-level double cascade switch multi-level leg. All of the switches except the $S_4$ can be implemented with slow-speed switches. The first three switches, $S_{11}$, $S_{12}$, and $S_{21}$ should be able to handle two times higher voltage than the remaining switches $S_{31}$, $S_{32}$, and $S_{41}$. As the number of levels increases, the number of switches needed is a half of that of the cascade leg. This topology is more suitable for applications where the necessary level is more than five and the input voltage is high but still needs the PWM operation with a low-voltage high-speed switch.
This concept can be extended to higher voltages, up to the maximum possible switches available. For example, if there is a four-times higher voltage rating switch available, this topology can be extended two steps more. Figure 6-12 shows the first column of a quadruple-cascade switch nine-level leg. The first column has five output lines that can be fed into a double cascade switch leg. This method can be extended with integer multiples, such as 2, 3, etc.. However, when the multiple is $2^n$ times, the number of switches required can be at a minimum and the total number of the series connected switches from the input to the output reaches a minimum, too. When the leg is expanded with the binary expansion, the total number of switches becomes as follows:

$$\sum_{i=1}^{m} (2^i + 2)$$

where $m$ is number of binary expansion steps. The value of $m$ is three for the leg shown in Figure 6-12. The total number of levels becomes

$$n = 2^m + 1.$$
6.6 Conclusion

A new multi-level leg topology is suggested. The topology is suitable for high-voltage input, output, and high-speed PWM applications. The topology uses only two high-speed switches for the PWM operation, regardless of the number of levels.

Currently available multi-level topologies for the PWM operation use too many high-speed switches. Therefore, the system becomes expensive. The new topology can reduce the system cost by replacing all but two of the high-speed switches with slow-speed ones. The slow-speed switches can be turned off with zero current, with the help of the high-speed switches.

The new topology can be used as a two-quadrant chopper by removing unnecessary switches.

For more than three levels, the topology can reduce the number of switches further by using higher voltage rated switches and creating multiple interleaving legs to reduce the
number of levels until it becomes three levels, which finally can be reduced into one output using a three-level leg.
Chapter 7 Conclusions

Current PCSs use thyristors with a six-pulse operation, due to the power capacity limitations of high-speed switches. The six-pulse operation contains a great deal of harmonics. To reduce them, the PCSs use phase-matching transformers, with many of them using different firing angles. Due to the transformers, the PCSs become bulky and expensive. The transformers also limit the speed of the PCSs. By replacing the thyristor with an IGBT, the PCS can be operated with a high-speed PWM that makes the system fast enough to suppress most of the harmonics without the transformer, saving size and costs. The high-speed PWM also allows the system to have a fast dynamic response. However, the voltage ratings of the IGBT are not comparable to those of the thyristors. An alternative to this difficulty is the use of a multi-level topology that can extend the voltage rating of the system.

In this research, a new type of PCS that uses IGBTs is designed and its prototype is built and tested successfully. The topology of the new PCS is composed of a multi-level chopper-VSC, due to the total power rating requirements of the device and the limited voltage ratings of the IGBT. A 250-kVA 1800-V 200-A three-level chopper-VSC topology is selected as a prototype for the new PCS. The design of the prototype PCS is based on the PEBB concept, by defining a three-level leg as a PEBB cell.

The test results of the PEBB leg show that the middle switches of the leg get large voltage spikes due to the parasitic inductance. This is reduced by employing a laminated bus. It turns out that the maximum switching frequency of the device that is suitably rated for the PCS is about 3-kHz, due to the limitations of the thermal management of the switches. The switching loss can be reduced to about 90% by using soft-switching technique. The switching frequency can be extended up to 20-kHz by employing a ZCT-type of the soft-switching technique. Due to the duty cycle limitation of the soft-switching technique, the PEBB leg also needs to be operated with hard-switching technique.

Three of the PEBB legs are used to build the VSC. To generate three-phase output, the
VSC is modulated by a three-level SVM that has a minimum number of switchings and small current ripples. Test results of the VSC show that an efficiency level of more than 97% can be achieved, and the THD can be reduced to within 1.5%. With using a simple closed-loop control, control bandwidth can be extended up to 600-Hz and shows a 400-μs response time.

One of the big disadvantages of the multi-level structure is the use of so many high-speed devices that lead to high costs. A possible alternative topology that can replace many high-speed switches with slow-speed ones is suggested.
Reference A  The Power Conditioning System


Reference B Three-Level Power Converters


Dissertation VPI&SU, Dec. 6, 1996, pp. 179-203


Reference C Soft-Switching Technique


