Electronic Packaging Strategies for High Current DC to DC Converters

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Current trends in electronics are toward the use of reduced voltages. In the past, 5 V and higher voltages have been the standard, however, currently, 3.3V and 2.5V circuits are becoming increasingly common. While the operating voltage is decreasing, electronic systems are becoming more complex. The net result is that in many cases, the current required by the next generation of electronics will be far greater than in the past. These increased currents and low voltages pose dramatic problems for designers not the least of which is the effect of electronic packaging and circuit implementation on the overall power supply performance.

In addition, for many applications, space and weight are at a premium and converters are needed to power low voltage circuit assemblies that are highly efficient, low in weight, and small in total height and footprint.

This dissertation addresses these trends and needs through the design, fabrication and evaluation of a 3.3V DC/DC converter. Designs of 3.3V, 2.5V, and 1.5V are presented and evaluated while a
3.3V, 100 watt converter with a power density of 157 watts/in³ has been fabricated and evaluated in a miniature form. This converter utilizes a implementation strategy developed by the author which was selected due to its ability to handle the current levels required and its compact size.

Specific contributions of this work include:
• Analysis of the effects of packaging on low voltage high current converters in order to provide a guideline for converter implementation. This analysis has been performed for 3.3 V, 2.5 V, and 1.5 V designs, respectively.
• Development of high efficiency 2.5 V, 100 watt and 1.5 V, 75 watt designs based on previously reported half bridge topologies.
• Development of a packaging strategy which allows the fabrication of low voltage compact converters with high efficiency. A 3.3 V converter has been fabricated and with the simulated data validated these experimental results.

For very low (less than 50 watts and / or less than 10 amps) and high power levels (hundreds of amps or kilowatts), the implementation strategy is normally clear; PCB/IMS, and DBC respectively. However, for applications in the middle range of power or current level, the optimum implementation is often unclear. The question that this work seeks to answer is under what conditions are different implementation schemes most suitable.
# Table of Contents

## Abstract

### 1.0 Introduction

1.1 Identification of the Problem  
1.2 Significance of DC/DC Converters  
1.3 Electronic Packaging; Definition and Background  
1.4 Current Problems Associated with DC/DC Converters  
1.5 Relevance of Packaging to these Problems  
1.6 Technical Contributions  
1.7 Structure and Organization of Dissertation

### 2.0 Brief Survey of Converter Topologies

2.1 Application  
2.2 Selected Converter Topology  
2.2.1 Circuit Topology  
2.2.2 Secondary Circuit  
2.2.3 Synchronous Rectifiers vs. Conventional Rectifiers  
2.3 Figures of Merit  
2.4 Summary and Conclusions

### 3.0 Industry Packaging Strategies for DC/DC Converters

3.1 Printed Circuit Boards (PCB)  
3.1.1 Printed Circuit Board Fabrication
Abstract

3.1.2 Limitations and Advantages
3.1.3 A PCB Example

3.2 Insulated Metal Substrates (IMS)
  3.2.1 The IMS Process
  3.2.2 Advantages and Limitations
  3.2.3 An IMS Example

3.3 Hybrids & MCMs
  3.3.1 Thick Film Hybrid Fabrication
  3.3.2 Advantages and Limitations
  3.3.3 A Hybrid Example

3.4 Direct Bond Copper (DBC) & Active Metal Braze (AMB)
  3.4.1 Direct Bond Copper Ceramics
  3.4.2 Active Metal Braze
  3.4.3 Advantages and Limitations
  3.4.4 A DBC and an AMB Example

3.5 Summary and Conclusions

4.0 Electrical Simulation of a 3.3 Volt 100 watt Design
  4.1 Simulation of Ideal Converter
  4.2 Inclusion of Transformer Winding Losses
  4.3 Incorporation of Parasitic Effects into Circuit Model & Comparison of Technologies
  4.4 Summary and Conclusions

5.0 Electrical Simulation of a 2.5 Volt 100 watt Design
  5.1 Simulation of Ideal Converter
  5.2 Inclusion of Transformer Winding Losses
  5.3 Incorporation of Parasitic Effects into Circuit Model & Comparison of Technologies
  5.4 Summary and Conclusions

6.0 Electrical Simulation of a 1.5 Volt design
  6.1 Problems with Very Low Voltages
  6.2 Simulation of Ideal Converter & Inclusion of Transformer Winding Losses
  6.3 Incorporation of Parasitic Effects into Circuit Model
  6.4 Summary and Conclusions
Abstract

7.0 Miniaturized Control Circuit

7.1 Requirements of Control Circuits
   7.1.1 Active Devices
   7.1.2 Passive Components
   7.1.3 Isolation

7.2 Thick Film LTCC Design
   7.2.1 Design
   7.2.2 Fabrication Process
   7.2.3 Performance

7.3 Summary and Conclusions

8.0 Integrated Converter

8.1 Design
   8.1.1 Electrical Consideration
   8.1.2 Thermal Management

8.2 Fabrication
   8.2.1 DBC Substrate
   8.2.2 Assembly

8.3 Performance
   8.3.1 Electrical Performance
   8.3.2 Thermal Performance

8.4 Summary and Conclusions

9.0 Summary of Findings

9.1 3.3 Volt. 100 watt Converter.
   9.1.1 Electrical Simulation
   9.1.2 Design and Fabrication
   9.1.3 Results & Comparison to Simulation

9.2 2.5 Volt, 100 watt Converter.
   9.2.1 Electrical Simulation

9.3 1.5 Volt Converter
   9.3.1 Electrical Simulation

9.4 Summary and Conclusions
10.0 Conclusions and Future Directions

References

Appendix A: Data sheets for Circuit Components

Appendix B: CAD Files for Power Stage

Appendix C: CAD Files for MCM-C Controller

Biography On Candidate
1.1 Identification of the Problem

Today, the trend in electronics is driving toward reduced voltage levels. In the past, 5 V operating levels were the standard for virtually all electronic applications. Over the years, IC designers have realized that many problems can be solved through the reduction of this operation voltage including; improved speed, and reduced power per switch. This trend causes a serious problem for power circuit designers who are charged with providing power to these new low power devices. The key problem is that although the voltage is decreasing, the system power is still rising due to increased system complexity. The net result is that the current demand is now much
Significance of DC/DC Converters

higher than in the past. Since the loss is proportional to the square of the current for a
given resistance, the next generation of power supplies will be very challenging to
fabricate in a compact size, with high efficiency, due to these increased current levels.

1.2 Significance of DC/DC Converters

A number of different types of circuits can be used to power an electronic system
depending on the intended application. For example, a typical desk top computer contains
an AC to DC (AC/DC) converter which transforms the alternating current (AC) provided
by the residential or commercial power outlet into a direct current (DC) which can be used
by the computers’ electronics. Alternatively in other applications, such as automotive
applications, a DC/DC converter would be used to step down the direct current 12 V
power provided by the battery and the alternator, to a lower voltage DC power signal that
can be utilized by electronic systems.

While both AC/DC and DC/DC converters are important, for low voltage (less than
five volts), the DC/DC converter is probably more important, since in most applications, a
higher voltage such as 5 or 12 Volts is normally required. For example, in a computer
system, an AC/DC converter may be used to provide 12V to run the CD-ROM, Hard
Drive, and Floppy Drive motors. These higher DC voltages can be used to provide a
source for a DC/DC converter to provide a low voltage level to a localized electronic circuit.

In addition, for spacecraft and aerospace applications, a DC bus of 48-120 volts provides power to the entire craft. These high voltages are used to minimize ohmic losses in the distribution systems which run throughout the aircraft. For these applications, DC/DC converters are normally used to provide lower voltages to operate systems at the point of use.

Applications also exist where a low DC voltage needs to be converted to a higher voltage. However, these applications are not as common as the down converter and will not be considered within the course of this work.

Based on these issues and the increased use of low voltage systems, DC/DC converters will continue to be critical elements for a variety of applications for the foreseeable future.

1.3 Electronic Packaging: Definition and Background

Electronic packaging refers to the integration of semiconductor devices into a robust electronic system that can withstand environmental conditions for extended periods
of time. Packaging is necessary since fragile semiconductor devices cannot withstand exposure to the environment. Moisture and environmental pollutants, as well as physical abuse, will permanently damage semiconductor devices. As a result, the devised solution for over 30 years has been to enclose the device in a package which provides electrical input and output connections (I/O), power, physical protection, and thermal conduction of heat away from the device. Theses packages are then assembled together in order to create a circuit or system.

Packages can either be single chip in nature or of a multichip design. The single chip package is the conventional and least complex approach, where each individual semiconductor is placed in its own package and then these packages are interconnected on a common substrate, such as a printed circuit board (PCB), to form the electrical circuit. A sample of common single chip packages is shown in Figure 1.1. In some cases, this approach is limited by the distances between the single chip packages on the circuit as well as the fact the package is much larger than the device itself. In these cases, a multichip package approach which contains several devices and their interconnects can alleviate these problems by placing the devices in very close proximity and reducing the overall system size.
While this concept of packaging seems very straightforward, the exact implementation of a given set of devices and interconnects can have dramatic effects on the performance of a particular circuit, since the packages reduce the electrical performance and complicate thermal management of this circuit.

1.4 Current Problems Associated with DC/DC Converters

A radical change is currently taking place in digital electronics that promises to have a profound impact on the design and implementation of future converters; reduced power supply voltages.

Although predicting the future is a risky business, the Semiconductor Industry Association (SIA), as well as a number of other organizations, have sought to attempt to envision the future trends in electronics. A complete discussion is beyond the scope of this document, however, two trends are important to observe related to DC/DC converters; reducing voltage levels, and increased total system power.

Figure 1.2 illustrates the trends which are expected to take place in the next fifteen years, for a typical desktop computer system. The voltages are constantly being reduced in order to allow a greater number of devices to be incorporated onto a single very large scale integrated circuit (VLSI). While this trend toward lower voltages may seem innocuous,
coupled with increasing system complexity, and therefore power, the result is a significant increase in the required current levels.

To explore the effects of this increased current level on converter loss, consider the loss in a conductor which is given by,

\[ \text{Loss(watts)} = I^2 R \]

where \( R \) is the resistance of the conductor, and \( I \) is the current. \( R \) can be found from the sheet resistance (\( R_s \)) of the metal used to create the conductive interconnect,

\[ R_s = \frac{\rho}{t} \]
where \( \rho \) = resistivity of the metal, and \( t \) is the conductor thickness. The total resistance is then found from,

\[
R = \frac{R_s L}{W}
\]
where \( L \) is the conductor length, and \( W \) is the conductor width. This analysis assumes a rectangular conductor geometry, however similar expressions can be derived for other conductor geometries.

A plot of power loss for a typical 1m\( \Omega \) interconnect is provided in Figure 1.3 for several different voltage levels, based on a 100 watt power level. Note that the dependence

![Power loss Versus Current for a 1m\( \Omega \) Resistance](image)

*Figure 1.3 : Power loss for a 1 m\( \Omega \) interconnect versus output voltage level for a 100 watt supply.*
of the power loss is on the square of the current, so that at 1 V output (therefore 100 amps)
the power loss in that connection is now 10 watts or 10% of the total power rather than the
0.4 watts or 0.4% power loss found at 5V (therefore 20 amps).

This dependence on the square of the current means that for a given power level, a
lower voltage converter will exhibit a reduced efficiency. In fact, a survey of the
converters available for sale today reveals that most low voltage (3.3 Volt and lower)
designs are available at either lower power levels or lower efficiencies than conventional
converters (5 Volts and greater).

Typical efficiency figures for conventional converters range from 80-90%, while
efficiencies as low as 70% are common for low voltage designs. For a 70% efficiency
rating, almost one third of the power delivered to the converter is lost as heat in the
converter itself. In most cases, these low efficiencies are not acceptable.

As a result of these trends, new materials, devices, circuit topologies, and
implementation schemes will be needed for the next generation of DC to DC converters.
1.5 Relevance of Electronic Packaging to these Problems

With this trend in mind, it has become clear that for a range of applications, the conventional packaged component and PCB paradigm will not be practical. New packaging approaches will be needed in order to handle these large currents. In fact, it can be argued that the packaging will be a dominate limitation since the bulk of the parasitic resistance in a conventional converter is located in the circuit interconnections.

1.6 Technical Contributions

The author’s contributions to this problem will be to explore the role of packaging in this type of low voltage converter and to demonstrate a number of low voltage designs through simulation as well fabrication and testing to validate these designs and implementaions approaches.

The goal of this work is not to develop new circuit topologies, but to examine and analyze the effects of electronic packaging on an existing topology as well as to adapt the topology to low voltages including 2.5 V and 1.5 V.

The specific contributions include:

- Simulation and analysis of a 3.3V converter design in order to explore the ramifications of packaging on the circuits performance.
Modification of the existing 3.3V design to create 2.5V and 1V designs.

Simulation and analysis of the 2.5V and 1V design.

Design and fabrication of a 3.3V design with an optimized packaging strategy developed by the author. This strategy allows fabrication of the circuit in a far smaller size than previously reported, with very high efficiency.

Test and analysis of the optimized 3.3V design and comparison to the simulated results.

1.7 Structure and Organization of this Dissertation

This document is divided into ten Chapters. Chapter One outlines the problem and sets the stage for the chapters that follow. Chapter Two is a brief overview of converter topologies, and it describes the selected converter topology used in this work. Chapter Three describes the most common approach used in industry today for implementation of DC/DC converters. Chapters Four, Five, and Six present and discuss models that have been developed for the selected topology based on 3.3 V, 2.5 V, and 1 V designs, respectively. A 3.3 V design simulated and fabricated by the author is discussed in detail in Chapters Seven and Eight, and is compared to the equivalent simulation. Finally, Chapters Nine and Ten provide a summary of the research findings as well as suggested future directions for this research work.
CHAPTER 2

Selected Converter Topology

2.1 Application

The aerospace industry is currently moving toward a distributed power system for electronic systems in aircraft as well as spacecraft. This is largely due to the fact that a single power source or set of power sources normally provides power for the entire vehicle. As a result, power must be transported from the source(s) to the localized electronic circuits throughout the craft. A low voltage distribution system that directly provided 3.3V or similar power to electronic assemblies would suffer from tremendous losses due to the current levels required. As a result, the trend is toward a 48-120 V DC power bus with local DC to DC converters which step down...
the voltage at the point of use. This trend toward distributed power systems is driving a demand for reliable, efficient and compact DC-DC converters, which can provide localized power at the point of use.

The author has selected a card mounted DC-DC converter as a suitable application to demonstrate the problems and possibilities associated with these low voltage converters. This applications, as illustrated in Figure 2.1, is very interesting for a number of reasons,

- The converter is part of the cards infrastructure, and therefore from the card designers point of view simply overhead. As a result, the total foot print for the converter must be as small as possible.
- Thermal management is straight forward due to the fact that the card is liquid cooled.
- A common card spacing of ~ 0.2 inches, places a challenging restriction on the overall height of the supply. This type of spacing is typical for Standard Electronic Module, format "E" (SEM-E) cards and housings which are very common in aerospace systems.
- An input voltage of 48 -120 V, with an output voltage of 3.3 V or less.
- Power levels per card from 10-100 watts are common.
2.2 Selected Circuit Topology

2.2.1 Circuit Topology

The selected circuit topology, illustrated in Figure 2.2, was developed by other researchers and has been reported elsewhere in detail\(^1,2\). The basic design is a modification of the classic half bridge converter which allows for a secondary circuit that is tuned for low voltage high current applications\(^3\). The chief advantages of this design are the fact that the transformer can be fabricated with a single turn, and low loss synchronous rectifiers.
can be used for output stage. A single turn secondary has the advantage of low loss due to the high currents which are commonly found in these secondary circuits. While the use of synchronous rectifiers allows for much lower loss than the conventional diode rectifiers for a range of currents.

![Selected converter topology utilized in this work.](image)

**Figure 2.2 :** Selected converter topology utilized in this work.

### 2.2.2 Secondary Circuit

While the primary circuit used in the topology is essentially the standard half bridge converter and rather unremarkable, the secondary circuit is the key to high efficiency at low voltages. The output voltage of the circuit can be expressed as,
where, \( V_o \) is the output voltage produced by a circuit configured with an input voltage \( V_{in} \), a Duty cycle \( D \), and a transformer winding ratio \( N_s/N_p \). \( N_s \) represents the number of turns on the secondary of the transformer, while \( N_p \) represents the number of turns on the primary side of the transformer. For a given transformer ratio the output of the circuit can be adjusted to produce a range of output voltages through adjustment of the duty cycle (D). The design used by the author utilizes a nominally 50% duty cycle which is controlled by a PWM integrated circuit in order to regulate the output voltage of the circuit based on feedback. The transformer winding ratio is selected to provide the nominal output voltage based on this 50% duty cycle.

The output rectifiers utilized in the secondary circuit can be driven either in the so called “self driven” mode or by external drive. Self drive works well for converters with output voltages above 3 V since the output of the transformer is able to effectively turn on and off the switches. However, at lower voltages an external drive is required. The self drive mode of operation is very appealing from a standpoint cost, since no additional

\[
V_o = V_{in}D(1-D)\frac{N_s}{N_p}
\]  

(2-1)
control elements are required. However, for low output voltages an external drive is required to properly drive the synchronous rectifiers.

In addition, a key advantage of this secondary circuit is the fact that several rectifiers can be placed in parallel in order to increase the power handling capacity as well as reduce the overall loss.

### 2.2.3 Synchronous Rectifiers vs. Conventional Rectifiers

Synchronous rectifiers are far more attractive for these types of converters due to the high secondary current levels. For a range of current levels the synchronous rectifier has very low loss characteristics, and multiple rectifiers can be used in parallel in order to ensure that each device is operating in this low loss condition, while as group they can effectively control large currents.

The loss experienced by as synchronous rectifier in this type of circuit can be expressed as,

\[
P_{loss} = I_{RMS}^2 \cdot R_{on}
\]  

(2-2)
Figures of Merit

where \( R_{on} \) is the on resistance of the rectifier and \( I_{RMS} \) is the Root mean square current through the device. In contrast to this, the power losses in a conventional Schottky rectifiers is given by,

\[
P_{loss} = I_d V_d
\]  \hspace{1cm} (2-3)

where, \( V_d \) represents the voltage drop of the device and \( I_d \) is the average current through the device. \( V_d \) and \( R_{on} \) are characteristics of the devices themselves with common minimum values of 0.4 V and 10 m\( \Omega \) respectively.

As a result, for a range of output current levels the synchronous rectifier offers much lower overall loss than the conventional rectifier. For this reason synchronous rectifiers have been used throughout this effort.

2.3 Figures of Merit

Key metric that can be used to evaluate a converters performance include:

- Efficiency: A measure of how much of the power delivered to the supply is actually delivered to the load. Efficiencies of 70-90% are common.
- Output Ripple: In a switching supply some amount of output ripple will always exist, unlike a linear supply which provides a pure DC output. This is due to the fact that the switching supply converters the input DC power source into some ac signal which is
then transformed in voltage level, by various means, and converted back to a DC power source at the output. Although filters are used at the output in order to remove the bulk of the switching harmonics, some level of ripple will exist. Typically magnitude of the output voltage ripple should be minimized to less than 50 mV.

- Input voltage range: Normally a converter requires some minimum input voltage in order to provide a stable well regulated output level, while, some maximum rated input voltage also exists. Input voltages ranges from 12-24V, or 30-70V are the most common for low output voltage converters.

- Output voltage regulation: How well a supply can control the output voltage level in response to changes in the load or input voltage level is a key requirement. Normally supplies are capable of controlling the output to within a few millivolts.

While this list is hardly inclusive of all of the requirements desired from a converter, these items are usually the most important. The author will focus primarily on the issue of efficiency throughout this work. This is primarily due to the fact that high output efficiency is the most difficult of these criteria to achieve with a low output voltage and high power rating.

2.4 Summary and Conclusions

The selected converter topology is ideal for low voltage high power applications due to the single turn secondary, and the ability to utilize a number of synchronous rectifiers in parallel to carry large secondary currents with high efficiency. In addition, this topology
can easily step down relatively large input voltages into very low output voltages. Self
 driven rectifiers can be utilized for 3.3V converters based on this topology while, lower
 voltage design will most likely require an external drive circuit which can easily be
 incorporated into the control circuit.

Synchronous rectifiers are sued in the output stage due to their low loss over a range
 of current levels and their ability to be used in parallel in order to handle large current
 levels. The key to high efficiencies in a converter design based on these devices, is to
 ensure that the rectifiers are operating with in the low loss region based on the RMS
 current through each device.

While a variety of characteristics are important for DC/DC converters, the author will
 focus on the need for improved efficiency at low voltage and high current levels.
CHAPTER 3

Industry Packaging Strategies for DC/DC Converters

3.1 Printed Circuit Board (PCB)

3.1.1 Printed Circuit Board Fabrication

One of the most popular implementation schemes for DC to DC converters is the Printed Circuit Board. These converters are fabricated on FR-4 laminate dielectrics with etched copper foil as the conductor medium. The process of fabrication can be summarized as follows,

- A roll of glass fiber cloth is dipped in epoxy resin in a continuous web.
- A set of rollers squeezes out the epoxy to a uniform thickness. This roll is then partially cured and referred to as a prepreg of FR-4.
- Since the epoxy is only partially cured, a roll of copper foil can be easily laminated to the prepreg roll through heat and pressure. Copper may be laminated to one or both sides.
The resulting roll of material, ~10-30 mils of FR-4 bonded to 1/2-2 oz. (note 1 oz. of copper is about 1.4 mils in thickness) of copper foil, is the building block for a Printed Circuit Board (PCB).

Normally, sections of the board are then cut into panels which may range in size from a few inches square up to 18” square panels.

Each layer of copper foil is then etched to form the traces required.

For multilayer boards, the layers are then bonded together using heat and pressure to form the final cured FR-4 board.

Via holes are drilled and plated-through to form electrical interconnections between the individual layers.

Solder mask is applied to protect the copper traces which will not be covered with solder, and the final board geometries are cut out of the panel.

Electrical components are then soldered to the board, and a final inspection and testing are conducted.

3.1.2 Limitations and Advantages

The advantage of this process is that a large number of individual boards can be made in one panel, using very low cost materials and processing. For example, an 18” panel can make up to 81, 2” square, PCBs in one process flow. As a result, PCB technology is by far the lowest cost and therefore the most common method utilized.

Printed circuit boards also allow for integrated planar magnetics using what are often referred to as PCB magnetics. This approach utilizes the copper traces of the Printed Circuit Board with addition of an attached ferrite core in order to form an integral planar
magnetic which is part of the Printed Circuit Board design. This aspect is a very important advantage for power electronic circuits.

As well as the industry standard for consumer electronics, Printed Circuit Boards offer a good deal of flexibility in the design of the converters. Single and double sided boards can easily handle a relatively high density of circuit interconnects at a very low cost. The use of high conductivity copper foils is also attractive. However, many limitations do exist with this technology and can be summarized as follows,

- Low thermal conductivity of the PCB dielectric complicates the thermal management.
- Limitations in the thickness of the copper foil, due to process constraints, limit the high current performance.
- The lack of rigidity in the dielectric as well as its inability to handle high temperatures limits the use of these circuits in harsh environments, such as under the hood automotive applications.
- The large coefficient of expansion of the PCB as compared to the semiconductor devices is a fundamental limit of the technologies reliability.

Table 1 illustrates the thermal properties of common substrate materials. As can be clearly seen, the PCB materials are orders of magnitude lower than any other options. However, this can be partially alleviated using the high thermal conductivity copper traces to draw heat away from thermal sources. Although, this approach assists in the thermal management of power loss, many PCB power converters still require additional heat sinks to accommodate lossy components.

In many of these applications, size can be compromised in order to maintain safe temperature levels, by spreading the heat out over a larger area, the total power that a
circuit is able to deliver, while maintaining the silicon devices below their maximum temperature of ~125 °C, is increased. This approach of spreading the load out among many devices also helps alleviate the second limitation of the PCB; thin copper conductors. For many applications, the thickness of PCB traces is adequate, however, for high current applications, the loss of the conductors becomes to great and either limits the total converter efficiency or jeopardizes the integrated of the PCB by locally heating the board. Thicker copper is in general very difficult to achieve for all but the simplest of Printed Circuit Boards, since the difference in thermal expansion between the copper and the FR-4 causes delamination and bowing of the entire board.

The final two limitations result in the fact that the Printed Circuit Board is not suitable for harsh environments or applications where reliability is a critical issue. The low melting point of the epoxy in the FR-4 board limits its operation to environments lower than ~150 °C, while the lack of rigidity and CTE mismatch make these circuits unable to sustain significant shock and vibration.

As a result of all of these factors, Printed Circuit Board converters often find the most use in consumer electronic applications where the reliability is low priority, and the cost is a critical factor. In fact, the PCB is the dominate technology in these markets, primarily due to the fact that they are some cost competitive that every penny is critical.

3.1.3 An PCB Example

An example of the printed circuit board converter is illustrated in Figure 3.1. This design is a 3.3V, 100 watt converter which is designed to operate over a nominal input range of ~ 30 - 70 V.
The design is innovative in that it is basically using three sets of output rectifiers in one converter in order to reduce the current level through each device. In this way, the designers have worked around the limitations of the PCB by spreading the thermal load over a large area, and eliminating the need for thick conductors by reducing the current through the conductors by a factor of one third. This design also makes extensive use of PCB magnetics which allow for a compact design. Even though this design is successful in low cost applications, it is larger in size due to the additional components needed in the secondary circuit. Also, it is interesting to note that at full power the output circuit still operates over 100 °C, even with the three pairs of output rectifiers.

### TABLE 1. Thermal Properties of Substrate Materials.

<table>
<thead>
<tr>
<th>Materials</th>
<th>Thermal Conductivity (watts/ m°K)</th>
<th>CTE (ppm / °C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>150</td>
<td>4.2</td>
</tr>
<tr>
<td>GaAs</td>
<td>50</td>
<td>5.8</td>
</tr>
<tr>
<td>Al</td>
<td>220</td>
<td>23</td>
</tr>
<tr>
<td>Copper</td>
<td>393</td>
<td>17</td>
</tr>
<tr>
<td>BeO</td>
<td>210</td>
<td>6.7</td>
</tr>
<tr>
<td>AlN</td>
<td>180</td>
<td>4.5</td>
</tr>
<tr>
<td>AlSiC (70% SiC)</td>
<td>202-218</td>
<td>7-7.3</td>
</tr>
<tr>
<td>FR-4</td>
<td>&lt;1</td>
<td>10-15</td>
</tr>
<tr>
<td>Cu-Graphite MMC</td>
<td>250-350</td>
<td>6.3-1.8</td>
</tr>
<tr>
<td>Be-BeO MMC</td>
<td>228-240</td>
<td>8.7-6.1</td>
</tr>
</tbody>
</table>
3.2 Insulated Metal Substrates

3.2.1 The IMS Process

One technology which improves on the thermal and mechanical limitations of PCB, is that of Insulated Metal Substrates (IMS). An IMS board is basically a single layer FR-4 board bonded to a metal plate. Normally, aluminum or copper plates of ~ 0.05 inches in thickness are utilized. This metal plate provides a stiffening element which allows the converter to be bolted to heat sinks or housings, and also provides a dramatic improvement in thermal performance.

IMS boards are made by coating a metal substrate with an epoxy based dielectric material. The coatings are normally a few mils in thickness depending on the dielectric
breakdown properties desired. This epoxy coating also serves to adhere the metallization layer to the IMS substrate. The metallization consists of a copper foil identical to that used in the PCB fabrication process. In this case, the copper foil is bonded to only one side of the substrate. The epoxy is cured to provide the raw substrate. Standard lithographic techniques used in the PCB process are used to etch the copper foil in order to form circuit traces. Multilayer boards can be constructed applying additional dielectric and copper layers to the basic IMS substrate.

The key differences between this type of process and that of the PCB are the following:

- Components are mounted directly to the substrate in a surface mount configuration. This strategy improves thermal performance.
- The circuit density is normally lower since multiple circuit layers are limited.

3.2.2 Advantages and Limitations

In the case of PCB, very little heat is conducted out through the board in most circuit applications. Since IMS has a very short thermal path between the components, which are the thermal sources, and the metal substrate, significant heat can be effectively removed through the substrate. As a result, components are normally mounted in a surface mount configuration to an IMS board, where as on a Printed Circuit Board, thermal sources are mounted in a through-hole configuration which allows the attachment of heat sinks and improves the air flow across the components. In the IMS case, the heat source is soldered directly to the copper metallization, and the heat is conducted through the thin dielectric layer and then into the metal substrate.
Insulated Metal Substrates

Large thermal sources can even be mounted directly to the IMS substrate. This is achieved by leaving a window(s) in the polymer dielectric which directly expose the metal substrate. However, in these cases, the backside of the component will be connected to the electrical ground, which is normally the metal substrate, which may not be possible in some circuits.

For this reason, IMS has become the industry standard for the high power converters which are intended for industrial or commercial applications. It should be noted that one key limitation of the IMS technology still exists, which is primarily caused by the CTE mismatch between the metal substrate and the silicon active devices. As noted in Table 1, the difference between the CTEs of these materials is quite significant, and as a result, these converters do not tolerate thermal cycling over extended periods of time.

3.2.3 An IMS Example

Figure 3.2 illustrates a typical commercially available IMS converter. This particular converter is also a 3.3V design, however, it is much lower in power with a maximum rating of 20 watts. The design utilizes surface mount components throughout which are soldered directly to the metallization. The converter is designed to be flipped over and soldered down with the plastic I/O band visible at the top of the converter.

A second example of an IMS converter is illustrated in Figure 3.3. This converter is a higher power design 3.3V, 100 watt, 48 V nominal input (~30-70V operational input range). This design utilizes both an IMS and a PCB in one potted package, as seen in a cross section illustrated in Figure 3.4. The thermal sources are mounted directly to the IMS board while the PCB mounted above the IMS board serves control and protection functions. This approach produces a very high density
circuit with good thermal management capabilities, particularly, when the package is bolted to a heat sink structure.

Figure 3.2: An IMS converter 3.3V, 20 watts.
Figure 3.3: An IMS converter 3.3V, 100 watts.

Figure 3.4: Cross section of converter shown in figure 3.4. Note the use of both a PCB and IMS boards.
3.3 Hybrid Converters

3.3.1 Thick Film Hybrid Fabrication

Thick film circuits are fundamentally different from IMS and PCB encounters in almost every way. Thick film technology utilizes a ceramic substrate and thick film printed metallizations to form the circuit traces. In addition, much greater latitude is available for the incorporation of integrated passive components into the substrate or module to achieve more compact circuit density.

The basic process of thick film technology revolves around screen printing. Screen printing utilizes a stainless steel screen which has been coated with a photo emulsion. This photo emulsion is a polymer film which is photosensitive and can be hardened with UV light. Using a photoplot or similar artwork and UV light, the screen is exposed in a manner which transfers the artwork design from the photoplot to the screen. In this way, areas of the photo emulsion can be hardened while the rest of the photo emulsion can be washed away. The result is a screen which has open and closed mesh areas. A paste or ink or formulation can then be forced through the open areas and thereby transfer the pattern from the original artwork on the photoplot, to a conductive ink pattern on the substrate. This process allows the formation of metal traces down to 5 mils with 5 mils spacing on a variety of substrate materials realizing very complex patterns.

A variety of inks or pastes are available which can be used for conductors, resistors, dielectric, encapsulants, or even solders. The most common pastes used are silver pastes for conductors, ruthenium oxide pastes for resistors, and glasses for dielectrics and encapsulants. The majority of these pastes contain a small quantity of glass that is used to bond the ink to the substrate.
A typical process flow for a thick film circuit would be:

1. Print the first conductor layer on to the substrate, Figure 3.5, (a).
2. Fire this conductor at 850 °C, in order to sinter the glass and form a bond with the substrate.
3. Print and fire the dielectric layer. Again, this material is normally a glass/alumina based paste which is fired at ~ 850 °C, Figure 3.5, (b).
4. Print and fire the second conductor layer, Figure 3.5, (c).
5. Print and fire ruthenium oxide paste to form resistors. This material also fires at ~850 °C, which sinters the glass content to form a strong bond with the substrate, while oxidizing the ruthenium metal in order to form a resistive layer, Figure 3.5, (d) and (e).
6. Print and fire a glass passivation layer. This layer is normally a glass paste which fires at ~500-600 °C, and is used to encapsulate and protect the internal layers of the circuit. Windows are normally provided for I/O and component connections to the internal metal traces.
7. Solder is printed and the components are placed and solder to the silver traces. Bare die and surface mount components can be utilized in these circuits.
8. The final circuit may be encapsulated or soldered into a sealed hermetic case.

### 3.3.2 Advantages and Limitations

Hybrid microelectronics began in the military and aerospace fields four decades ago. This technology is ideally suited to high reliability applications for a variety of reasons, namely,

- Close CTE match is possible between almost all materials utilized in the module.
- Ceramic substrates with high thermal conductivity, strength, and thermal stability are utilized.
- Cermet conductors offer high conductivity and a close CTE match to the substrate.
Hybrid Converters

- The entire package can easily be mounted inside a hermetic case.

Clearly, this type of circuit implementation is fundamentally different than IMS or PCB modules. All of the layers are created in an additive process rather than in a subtractive etching process.

The advantages of this type of approach are as follows,

- The thermal management is excellent due to the fact that the ceramic substrates are at least ten times more thermally conductive than PCB.
- Thermal expansion of the ICs, metallization, and substrates is almost exactly matched, so that thermal stresses caused by thermal cycling are minimal.
- The overall reliability of these circuits is very high.
- Passive components can be integrated into the substrate which reduces the total size of the circuit.

The primary limitation of this approach is the increased cost. The materials are more expensive and the economies of scale cannot approach those of PCBs parts.

The conductors used for this technology are essentially pure gold or silver and approach the conductivity of pure metal. The metal thickness is limited to about 12 microns, which is ~ half the thickness used in PCB or IMS designs. Line and space resolutions down to 5 mils are possible to achieve using thick film technology.

The design of this type of converter is more complicated than for the other classes of converters. This is due to the fact that many of the passive components are incorporated into the board. However, a number of issues should be considered for the design of these circuits, such as,
Figure 3.5: Typical Thick Film Process Steps, using a gold conductor, Ruthenium Oxide resistors, and ceramic/glass dielectric.
- Mount large thermal sources, such as power FETs and Diodes, in close contact with the substrate.
- Thermal sources should be spaced as far a part as possible from each other and from the substrate edge, in order to prevent local heating.
- Power traces should be kept as short and wide as possible.
- In order to provide adequate isolation, traces with large voltage gradients should be separated by an adequate distance. Use of an encapsulation with a fixed breakdown voltage should be considered for high voltage traces.
- Parasitics can be minimized by placing components as close together as possible and through the use of a ground plane. Also, key components such as decoupling capacitor should be mounted as close as possible to the device they are intended to decouple.
- Integrated Resistors must be carefully designed in order to consider the effects of their power dissipation.

3.3.3 A Hybrid Example

Figure 3.6 is an illustration of a hybrid converter. In this case, the converter is composed of a number of aluminum oxide substrates which are printed with gold cermet conductors, printed glass encapsulation (the green areas), and bare die components. The top two substrates are the power circuits while the bottom is a control circuit. Separate substrates provide isolation between the circuit elements. Each of the ceramic substrates is soldered into the AlSiC housing which is then sealed hermetically. Also in this case, the electrical components are specified to withstand large radiation doses and still function properly. As a result, this converter could be bolted in a spacecraft, and will easily survive launch and provide a useful life of up to 50 years. Compared to the PCB converters where a lifetime of a year or two may be acceptable, and surviving a launch is unlikely. The clear
trade-off for this type of converter is the cost. The packaging alone for this converter is several times the cost of any of those technique discussed so far in this analysis. With all of the assembly cost and the complex screening, this type of converter can easily be thousands of dollars, while a PCB converter would cost a few hundred dollars. However, for high reliability applications, this type of converter is considered the industry standard.

Figure 3.6: Hybrid converter example produced by Magnitude-3, L.L.C. Photo courtesy of Magnitude-3, L.L.C

3.4 Direct Bond Copper and Active Metal Braze

3.4.1 Direct Bond Copper Ceramics

Very high power circuits are normally built using different techniques than conventional circuits. For example, a 600 Volt, 100 Amp motor drive would not be
possible using a Printed Circuit Board or even IMS. Primarily due to the fact that the thin conductors used in most electronic circuits are not capable of carrying these large currents. The loss in a conductor is defined as,

\[ \text{Loss (watts)} = I^2 R \]

where \( R \) is the resistance of the conductor, and \( I \) is the current. \( R \) can be found from the sheet resistance (\( R_s \)) of the metal,

\[ R_s = \frac{\rho}{t} \]

where \( \rho \) is the resistivity of the metal, and \( t \) is the conductor thickness. The total resistance is then found from the relation,

\[ R = R_s \frac{L}{W} \]

where \( L \) is the conductor length, and \( W \) is the conductor width. In most cases, the resistivity is fixed over a small range set by nature; the resistivity of metal. As a result, for a given length and width, the loss is inversely proportional to the conductor thickness. The conductors which can be used in PCB and IMS circuits are not thick enough for very high current applications. The solutions that have been developed for these applications normally include Direct Bond Copper (DBC), or Active Metal Braze (AMB).

DBC is a layer of thick copper, 0.008” – 0.012” in thickness, which is bonded to a ceramic substrate using an oxide bond developed at high temperature. BeO, AlN, and \( \text{Al}_2\text{O}_3 \) substrates are all available with DBC metallization. These substrates can be etched to form circuits, and are normally used in conjunction with bare die semiconductors. This type of substrate is normally soldered to a metal or metal matrix composite base plate.
which can then be bolted to a heat sink. This approach offers the ultimate performance in thermal management and current carrying capacity.

DBC is created by placing a copper foil on both sides of a ceramic substrate, and heating the assembly to \(~1000\) °C in a controlled atmosphere. Adequate oxygen exists within the furnace in order to bond the copper sheets to the ceramic with a strong oxide bond.

DBC is available on 5-40 mil thick alumina, BeO, and aluminum nitride, in thicknesses which range from 8 mils to 12 mils. Active metal braze utilizes similar substrates, however, the metallizations are normally 3 - 8 mils in thickness. A sample of DBC on alumina is illustrated in Figure 3.7.

Figure 3.7: Sample of an etched DBC on alumina substrate. The copper has been plated with a Nickel / Gold finish to prevent oxidation.

DBC is available on 5-40 mil thick alumina, BeO, and aluminum nitride, in thicknesses which range from 8 mils to 12 mils. Active metal braze utilizes similar substrates, however, the metallizations are normally 3 - 8 mils in thickness. A sample of DBC on alumina is illustrated in Figure 3.7.
3.4.2 Active Metal Braze (AMB)

AMB is very similar to DBC, however, the conductor is brazed to the ceramic using an active braze. Normally, the conductors are slightly thinner than DBC case, in the range of 0.003” - 0.008”. These substrates offer similar capabilities with slightly improved reliability, due to the thinner conductor.

![Direct bond copper DC/DC converter, (100 watt, 3.3 V) fabricated by the author.](image)

Active Metal Braze is bonded to the ceramic substrate using a high temperature braze alloy that bonds both to the ceramic and to the copper foils. The result of these techniques is a sandwich of ceramic between copper conductors.

3.4.3 Advantages and Limitations

DBC and AMB braze technologies are ideal for high current or high power applications. However, care must be taken to select the metal thickness, since very thick
metallizations may cause reliability problems due to the mismatch in CTE with the ceramic and copper metallization.

3.4.4 An DBC and an AMB Examples

An example of a DBC converter is shown in Figure 3.8. This unit was fabricated by the author and is a 100 watt, 3.3 V converter. Note that the active components are soldered directly to the substrate in a bare die format, and that 10 and 5 mil aluminum wedge bonds have been used to form the source connections on the top of the device. In addition, a planar magnetic, visible at the center of the board, is incorporated into the design. The substrate is 12 mil DBC on alumina.

An example of AMB circuit, also fabricated by the author, is illustrated in Figure 3.9. This circuit is not a converter but a power amplifier with a rating of over 1 kilowatt. The substrate used for this circuit is AlN due to its superior thermal conductivity; approximately ten times greater than alumina.
3.5 Summary and Conclusions

The most common implementation strategies for DC to DC converters include the following,

- Printed Circuit Board (PCB),
- Insulated Metal Substrate (IMS),
- Hybrid Thick Film, and
- Direct Bond Copper (DBC) or Active Metal Braze.

Of these options, the Printed Circuit Board normally is used for the low to medium power range. At still higher power levels, IMS is the dominate technology. For very high power or high current levels, DBC or AMB are the technologies of choice. Hybrids thick film technology finds the most use in high reliability applications or in harsh environments at a wide range of power levels.
CHAPTER 4

Simulation of a 3.3 Volt 100 watt Design

4.1 Simulation of the Ideal Converter

4.1.1 Converter Model

In order to understand the properties and potential of the selected topology and components, a model was prepared using the SABER simulation program by ANALOGY. SABER is ideal for this type of power circuit since it already contains a detailed library of the components needed for this circuit, and it is designed to accurately simulate these types of electronic circuits.

Figure 4.1 illustrates the schematic design used in the simulation. The reader will recall from chapter 2, that this schematic is the power stage of
the selected converter topology with the transformer and duty cycle adjusted for a 3.3 Volt output, and a 30-70 Volt input. For simplicity, the control portion of the circuit is not simulated. This is due to the fact that the control portion of the circuit is composed of devices for which models are not readily available. In addition, in this work, the researcher is only interested in the steady state performance, and as a result, the steady state control functions can be simulated using digital waveforms. As a result, the control has been replaced with a series of square waveform generators.

The simulation consists of an input supply, which was nominally set to 70 V, two IRF540 MOSFETS in a half bridge configuration, a transformer, and four output synchronous rectifiers, plus their associated passive components. This core set of components forms the heart of the converter, and allows a detailed evaluation of the losses and performance.

The transformer in the circuit is modeled using the saber model for a nonlinear three winding transformer. The two secondary windings are connected together and are one half turn each, which produces a one turn center tapped secondary. The saber model is based on the physical dimensions of the E22 core, see attached data sheet in Appendix A, used to fabricate the transformer and its material properties. The material used for these transformers was Philips 3F3, see attached data sheet in Appendix A.
Gate drive waveforms were produced using digital square waveforms. Complementary waveforms were generated using two sources out of phase. These sources allow for precise control of the rise and fall times, voltage levels, period, and phase of the signals. A total of four sources were used to provide drive signals for the primary and secondary switches.

The only real difference between the simulation and the real circuits is the use of an IRF540 in the simulation instead of the IRL540 used in the circuits. This was necessary since the model for the IRL540 was not available. In addition, the only difference between the IRF540 and the IRL540 is the drive characteristics, which are not relevant to this...
simulation. The IRL540 will operate with a lower drive voltage from a logic source, whereas the IRF540 is intended for analog drive circuits.

In addition, to the standard component models used within this circuit, a number of resistors have been placed within the circuit to simulate the effects of parasitic resistance within the traces, components connections, and wirebonds. For the ideal case, these resistors are set to negligible values (such as 1E-12 Ohms).

4.1.2 Results

Figure 4.2 illustrates the gate drive waveforms generated by the square wave generators. The high side gate drive has been normalized to be the same magnitude as the low gate drive signal for comparison purposes. Both signals are essentially identical, expect that the high gate drive must drive the MOSFET with respect to its source which is a 70 V square wave signal. As a result, the high side gate drive swings from 0 to 85 Volts. Note also that these waveforms are not ideal but are distorted by the input characteristics of the MOSFETs. While it is true that an ideal MOSFET does not draw any gate current, power MOSFETs have considerable gate capacitance which must be charged and discharged in order to turn the device on and off. The distortion of these drive waveforms is caused by this capacitance. The frequency of these waveforms is 500 KHz, with a rise and fall time of 120 ns, and a magnitude of 15 Volts.
Figure 4.2: Half bridge gate drive waveforms used in the simulations.
Figure 4.3: Primary and secondary waveforms for simulated converter.
Figure 4.4: Current and voltage waveforms for rectifier circuit.
Figure 4.5: Output voltage and power for simulated circuit.
Simulation of the Ideal Converter

Figure 4.6: Comparison of output and input power for simulated circuit.

Power In = 99.77 watts
Power Out = Efficiency = 91%
Power In = 99.77 watts
Power Out = 90.826 watts
Figure 4.3 illustrates the primary and secondary waveforms from the simulated circuit. The primary is a square waveform with a frequency equal to the gate drive signals, and a magnitude equal to the input voltage. The transformer then steps that voltage down into two complementary 7 volt waveforms on the secondary side, also illustrated in Figure 4.3. Note that some small amount of distortion exists in these waveforms induced by the input characteristics of the half bridge MOSFETs and the gate drive signals.

The two pairs of synchronous rectifiers on the output stage act in complement to sink current through the center tap and load, to provide the desired output, as illustrated in Figure 4.4. Note that each pair of rectifiers sinks ~ 30 amps of current for half a cycle, or approximately 15 amps each, while the other pair sinks the same current for the second half of the cycle. The result, as illustrated in Figure 4.5, is a 3.3 Volt output waveform with ~100 mV ripple at the switching frequency. This figure also illustrates the output power of ~ 100 watts, based on a load of 0.0625 Ohms.

Both the input power and the output power are plotted together for reference in Figure 4.6. Note that the simulation is running with an output power just under 100 watts, at 90.826 watts, while the total input power from all sources is 98.816 watts. The input power includes not only the input voltage source but also the gate drive sources. The result, is a net efficiency of 91%. This figure includes losses in the magnetic core, the
4.2 Inclusion of Transformer Winding Losses

The model developed in section one of this Chapter is quite accurate for low current levels, however, the losses in the windings must be considered for high current levels. This may seem surprising, since the secondary on the transformer is only a single turn with a center tap, however, even the resistance of this single turn can be a problem with very high current levels.

In order to include the losses caused by the winding, each winding is modeled as a resistance of a strip of copper \( \sim 6 \text{ mm} \times 35 \text{ mm} \), which is the actual dimension of a typical winding conductor used in a planar magnetic. The thickness of the conductor is 10 mils. This results in a sheet resistance \( R_s \) of \( 6.299 \times 10^{-5} \text{ } \Omega \), and a parasitic resistance value per winding of 0.399 m\( \Omega \) based on the relations,

\[
R_s = \frac{\rho}{t}
\]  

(1)
Using these figures, a winding loss was included in the model by directly plugging this winding resistance directly into the Saber Model. Figure 4.7, illustrates the performance of the circuit including the winding loss. Note that the loss has increased from 7.99 watts to 10.697 watts, which agrees fairly well with the expected $I^2R$ loss of the equivalent 0.399 mΩ resistor pair, which would equal ~ 1 watt.

\[
R = \frac{LR_s}{w}. \tag{2}
\]

4.3 **Incorporation of Parasitic Effects into Circuit Model & Comparison of Technologies**

The parasitics of the power stage circuit are a very strong function of the implementation scheme used to build the converter. Not only is the selected technology important, but the exact component placement, configuration and interconnections are important. As a result, an exact model of any given implementation would require a detailed analysis of that particular circuit design.

However, it is possible to generalize the analysis without the restrictions of a particular circuit implementation. This can be achieved by modeling the circuit interconnections based on an average estimated circuit connection. In other words, the
Figure 4.7: Comparison of output and input power for simulated circuit, with transformer winding loss included.
traces, wirebonds, and solder joints can all be modeled based on their average physical dimensions and material properties. In order to keep the analysis manageable for the entire circuit, the model used was that of a simple parasitic resistance. Inductive and capacitive effects are second order in these high current supplies due to the $I^2$ dependence of the resistive loss. As a result, each interconnection is modeled based on its physical dimensions and electrical conductivity.

In order to explore the potential of different technologies for these types of converters, a generalized model was developed for thick film, IMS and PCB, as well as DBC. This was accomplished by adding the parasitic resistance values $R_1$, $R_2$, $R_3$, and $R_4$ shown in Figure 4.8. Only the secondary circuit was considered since the parasitics in the primary circuit are of much lower importance due to the reduced current levels.

The circuit interconnects were modeled as 50 mil wide, 200 mil long strips of metal with $t$ thickness. While many of the traces in a real circuit may be shorter than this average length, some of the connections will be longer. As a result, this is a fairly good representation of what can be expected from a given technology. Wirebonds are modeled as a resistor of 1.4 mΩ which is typical for a 10 mil diameter, 100 mil long aluminum wedge bond. Normally, four bonds are utilized per source for a total resistance per source connection of 0.35 mΩ.
The thickness $t$ was selected for each technology based on the physical thickness in common use for that particular technology, which are tabulated in Table 1. The resistance for the average trace for each technology was then calculated from the metal conductivity and the geometry. These resistances, which are tabulated in Table 2 for each technology, are then plugged into the circuit model. The results, are illustrated in Figure 4.9 through Figure 4.12.

**TABLE 1. Material properties and thicknesses used for interconnects modeling.**

<table>
<thead>
<tr>
<th>Technology</th>
<th>Metal Thickness (mils)</th>
<th>Metal Resistivity ($\mu\Omega - \text{cm}$)</th>
<th>Sheet Resistance ($\Omega / \cdot$)</th>
<th>Equivalent Resistance of a 50 mil wide x 200 mil long Trace (m$\Omega$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB &amp; IMS (1 oz.)</td>
<td>1.4</td>
<td>1.6</td>
<td>4.5E-4</td>
<td>1.8</td>
</tr>
<tr>
<td>Thick Film (Ag / Pd)</td>
<td>0.5</td>
<td>2.54</td>
<td>2E-3</td>
<td>8</td>
</tr>
<tr>
<td>DBC (8 mil)</td>
<td>8</td>
<td>1.6</td>
<td>7.87E-5</td>
<td>0.315</td>
</tr>
<tr>
<td>DBC (12 mil)</td>
<td>12</td>
<td>1.6</td>
<td>5.2E-5</td>
<td>0.209</td>
</tr>
</tbody>
</table>

Figure 4.9 shows the predicted performance for IMS or PCB using 1 oz. copper metallization. The efficiency has dropped from the ideal level, including winding loss, from 89% to 83%. It is interesting to note that for the case of 12 mil DBC, the efficiency drop was almost negligible, with the DBC 12 mil simulation predicting an efficiency of 89%. In addition, the 8 mil thick DBC also showed little change with a predicted value also at 89%. The worst case was the thick film simulation with a predicted efficiency of
66%. This significant reduction is not surprising given the high resistance common in these silver palladium conductors as well as the reduced thickness.

![Figure 4.8: Typical 3.3V secondary circuit, illustrating parasitic resistance values.](image)

**4.4 Summary and Conclusions**

The key conclusion from the analysis conducted is that the technology selected for the implementation of this type of circuit can have a dramatic effect on the performance of the
final circuit. This is not unexpected due to the large currents involved in the secondary circuit.

In addition, this analysis predicts that the winding loss in the transformer magnetic may also have a dramatic effect on the circuit performance. For DBC implementations, the losses in the secondary windings and its interconnects are slightly larger than the losses in the rest of the secondary circuit interconnects.

### TABLE 2. Modeled Parasitic Resistance Values.

<table>
<thead>
<tr>
<th>Technology</th>
<th>R1 (mΩ)</th>
<th>R2 (mΩ)</th>
<th>R3 (mΩ)</th>
<th>R4 (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB &amp; IMS (1 oz.)</td>
<td>1.8</td>
<td>2.15</td>
<td>2.15</td>
<td>1.8</td>
</tr>
<tr>
<td>Thick Film (Ag / Pd)</td>
<td>8</td>
<td>8.35</td>
<td>8.35</td>
<td>8</td>
</tr>
<tr>
<td>DBC (8 mil)</td>
<td>0.315</td>
<td>0.665</td>
<td>0.665</td>
<td>0.315</td>
</tr>
<tr>
<td>DBC (12 mil)</td>
<td>0.209</td>
<td>0.559</td>
<td>0.559</td>
<td>0.209</td>
</tr>
</tbody>
</table>
Summary and Conclusions

Figure 4.9: Performance of the 3.3V, 100 watt converter incorporating PCB/IMS parasitics resistance values.
Figure 4.10: Performance of the 3.3V, 100 watt converter incorporating 12 mil DBC parasitics resistance values.
Figure 4.11: Performance of the 3.3V, 100 watt converter incorporating 8 mil DBC parasitics resistance values.
Figure 4.12: Performance of the 3.3V, 100 watt converter incorporating Thick Film parasitics resistance values.
5.1 Simulation of the Ideal Converter

5.1.1 Converter Model

Based on the model of the converter developed in Chapter 4 for a 3.3 V, 100 watt design, a nominal 2.5 V design was developed. This design is a slight modification of the 3.3 V, with a modified transformer and modified secondary drive waveforms. This model is useful for evaluating the effects of increased current on the electronic packaging of the circuit.

Based on the discussion in Chapter 4 for the operation of this circuit, one can visualize the basic operation of the circuit as follows. The primary circuit transforms the input power into a periodic waveform that can be
stepped down by the transformer. This fact is necessary since the transformer can only be used with this type of periodic waveform, and will not step down the DC voltage. The secondary portion of the circuit then rectifies this reduced periodic waveform, or converts it back to a DC power source. In this way, the output of the circuit is a “miniature” version of the input.

The key difference between the 3.3 V design and the 2.5 V design is the winding ratio of the transformer. On the 2.5 V design, the primary has a higher number of turns while the secondary is still fixed at one turn. The result is that the secondary voltage is stepped down to a lower voltage in the case of the 2.5V supply than in the 3.3V converter. In addition, the secondary drive for the synchronous rectifiers is now performed by an IC rather than a direct drive signal provided by the transformer. This is necessary since the secondary voltages are now so low that they can not effectively drive the rectifiers.

5.1.2 Results

The gate drive waveforms used to control the primary switches are illustrated in Figure 5.1. Note that the high side gate has been normalized, since it is much larger in magnitude due to the fact that it is referenced to the high side source. The switching frequency and duty cycle are identical to those utilized in the 3.3 V design. The drive waveforms for the secondary circuit are very similar to the these primary side waveforms.
Voltages on the primary and secondary of the transformer are illustrated in Figure 5.2. The larger waveform is the product of the half bridge, and is simply a square waveform of the input voltage, with a magnitude of ~70 Volts. The transformer then steps this voltage down to the smaller waveform which is ~6 V in magnitude.

Secondary voltage and current waveforms are illustrated in Figure 5.3 for this 2.5 V design. The top two waveforms are the voltages on the high and low side of the secondary, while the bottom two waveforms are the associated currents. The operation of this circuit is identical to the 3.3V design in that the secondary high and secondary low are the complement of one another. In addition, the high side and low side pair of rectifiers sink current through the load each for half a cycle. Note however, that the average current has now increased from ~30 amps to ~40 amps. Figure 5.4 illustrates the secondary drive waveforms and their relation to the secondary current through each pair of rectifiers.

Typical results for this circuit are illustrated in Figure 5.5. This graph plots both the output voltage and output power as a function of time. The initial transients represent the startup of the circuit which then settles rapidly into a stable output. The output voltage is not exactly 2.5V due to a lack of feedback in this model which would normally adjust the drive waveforms in order to produce a constant output voltage. The output power also is
Inclusion of Transformer Winding Losses

not exactly 100 watts, since a resistive load is used and the output voltage is lower than expected.

Both the input power and the output power are plotted combined for reference in Figure 5.6. Note that the simulation is running with an output power just under 100 watts, at 88 watts, while the total input power from all sources is 98.169 watts. The input power includes not only the input voltage source but also the gate drive sources. The result is a net efficiency of 88%. This figure includes losses in the magnetic core, the devices and components, but does not include losses within the transformer windings, and the circuit interconnects. This again will be referred to as the “ideal” efficiency since it represents the best possible implementation using this design.

5.2 Inclusion of Transformer Winding Losses

As in this case of the 3.3V design, the model developed in section one of this Chapter is quite accurate for low current levels, however, the losses in the windings must be considered for high current levels. In this case, the winding losses are addressed in the exact same way as in the 3.3V design, with a parasitic resistance value per winding of 0.399 mΩ.
Figure 5.1: Gate drive waveforms used for half bridge primary of the ideal 2.5 V converter. Note high side switch drive has been normalized for comparison purposes.
Figure 5.2: Simulated primary and secondary waveforms for the ideal 2.5 V design.
Figure 5.3: Simulated secondary voltage and current waveforms for the ideal 2.5V design.
Figure 5.4 : Secondary current waveforms and drive signals for the ideal 2.5V design.
Figure 5.5: Simulated output of the 2.5 V design.
Figure 5.6: Comparison of output and input power for simulated 2.5V circuit.
Using these Figures, a winding loss was included in the model by integrating this winding resistance directly into the Saber Model. Figure 5.7 illustrates the performance of the circuit including the winding loss. Note that the loss has increased from 11.85 watts to 13.55 watts, which agrees almost exactly with the expected $I^2R$ loss of the equivalent 0.399 m$\Omega$ resistor pair, which would equal ~ 1 watt. The net result is an efficiency of 87%.

### 5.3 Incorporation of Parasitic Effects into Circuit Model & Comparison of Technologies

As was done in Chapter 4 with the 3.3 V converter, models have been developed to explore the potential of different technologies for these types of converters with the lower voltage 2.5V and its associated higher current levels. A generalized model was developed for thick film, IMS and PCB, as well as DBC technologies. As with the 3.3V model, only the secondary circuit was considered since the parasitics in the primary circuit are of much lower importance due to the reduced current levels.

The circuit interconnects were again modeled as 50 mil wide, 200 mil long strips of metal with t thickness, and an equivalent wirebond source resistance of 0.35 m$\Omega$ per device connection was used. The results are illustrated in Figure 5.8 through Figure 5.11.
Figure 5.7: Comparison of output and input power for simulated circuit, including winding losses.
Figure 5.8 shows the predicted performance for IMS or PCB using 1 oz. copper metallization. The efficiency has dropped from the ideal level, including winding loss, of 87% to 81.1%. This represents several watts of power consumed as heat within the PCB or IMS traces which results in this nearly ten percent reduction in the efficiency of these circuitries.

Figure 5.9 illustrates the performance of a simulated 12 mil thick DBC converter. It is interesting to note that for the case of 12 mil DBC, the efficiency drop was almost negligible, with the DBC 12 mil simulation predicting an efficiency of 86%. In addition, the 8 mil thick DBC also showed good performance with a predicted efficiency value of 85%, as shown in Figure 5.10.

The worst case was the thick film simulation, shown in Figure 5.11, with a predicted efficiency of 57%. This significant reduction is not surprising given the high resistance common in these silver palladium conductors as well as the reduced thickness of most thick film circuits due to the inclusion of many additive components. Clearly, these levels of loss are unacceptable.
Figure 5.8: Performance of the 2.5V, 100 watt converter incorporating PCB/IMS parasitics resistance values.
Figure 5.9: Performance of the 2.5V, 100 watt converter incorporating 12 mil DBC parasitics resistance values.
Figure 5.10: Performance of the 2.5V, 100 watt converter incorporating 8 mil DBC parasitics resistance values.
Figure 5.11: Performance of the 2.5V, 100 watt converter incorporating Thick Film parasitics resistance values.
5.4 Summary and Conclusions

The key conclusion from this analysis is that the technology selected for the implementation of this type of circuit can have a dramatic effect on the performance of the final circuit. This is not unexpected due to the large currents involved in the secondary circuit.

In addition, this analysis predicts that the winding loss in the transformer magnetic may also have a dramatic effect on the circuit performance. For DBC implementations, the losses in the secondary windings and its interconnects are almost identical to the losses in the rest of the secondary circuit interconnects combined.
CHAPTER 6

Simulation of a 1.5 Volt Design

6.1 Problems with Very Low Voltages

In previous Chapters, the author has shown how low voltage high current converters can be successfully fabricated with high efficiencies. Both 3.3V and 2.5V design have been demonstrated through simulations, and the ramifications of the implementation technology have been explored.

As the technology moves to the next step of 1.5 V or 1V supplies, the challenges become much greater due to a number of factors, namely,

- The output voltage level approaches the noise level.
Problems with Very Low Voltages

- Output filtering becomes critical since the conventional 100 mV ripple, which is commonly found in commercial supplies at higher voltages, is now 10% of the output level.
- Current levels, for all but the lowest total power rated converters, are now at critical levels for the current generation of available devices.

The first two items may require careful consideration of the circuit topology as well as the output filter. However, the last issue is far more difficult to address. This is due to the fact that in most cases, the power loss in a synchronous rectifier can be closely represented by the relationship,

\[ P_{\text{loss}} = I_{\text{RMS}}^2 \cdot R_{\text{on}} \]  \hspace{1cm} (6-1)

with \( I_{\text{RMS}} \) equals to the RMS current through the device, and \( R_{\text{on}} \) equals to the on resistance of the device. Most commercially available MOSFETs used for these applications exhibit on resistance values on the order of 10 mΩ. Based on equation 6-1, the loss of a typical low loss synchronous rectifier as a function of current is illustrated in Figure 6.1. Although this device is rated to 75 amps, clearly it is only capable of reasonable operation below 20-30 amps. At higher current levels, the total circuit efficiency, as well as the ability to cool the output rectifiers, would be unacceptable in most cases. As a result, to achieve higher current levels, multiple output rectifiers must be used in parallel in order to handle the desired current with acceptable losses. For the case of 3.3V and 100 watts, two rectifiers works well with an average current of 15 amps each.
to meet the total requirement of 30 amps. Similarly for the case of the 2.5 V, 100 watt design two rectifiers will also work well with an average current of 20 amps each to meet the total requirement of 40 amps. However, for 1.5 V or 1V designs the losses with only two rectifiers are enormous. For example for two rectifiers at 1.5V and 100watts, the average current per device needed to make the total 66 amp requirement would be 33 amps each. At 33 amps each rectifier would exhibit a loss on the order of ~8 watts compared or almost double the loss of the equivalent 2.5 V design.

Figure 6.1 : Power loss in a typical low loss synchronous rectifiers as a function of current.
As a result, the maximum power rating, with reasonable efficiency and operating temperatures in mind must be based on the number of rectifiers and therefore the maximum allowed current. A four rectifiers circuit, two pairs, is efficient up to ~ 40 amps, while a six rectifier circuit could be efficient up to ~60 amps.

6.2 Simulation of Ideal Converter & Inclusion of Transformer Winding Losses

Based on the above analysis, a 1.5V converter was designed and simulated using six output rectifiers. This circuit is very similar to the 2.5 V design and utilizes the same basic circuit design. The key differences are the winding ratio of the transformer and the number of output rectifiers. This circuit was simulated using Saber, and the results are illustrated in Figure 6.2 through Figure 6.4, and include the winding loss but do not include the losses caused by the interconnects.

The output voltage and power delivered to the load are illustrated in Figure 6.2. With a 1.5 V output and power level of 107 watts, this simulated circuit delivers an average current of 71 amps, or ~ 24 amps per rectifier. The resulting efficiency of 75% is illustrated in Figure 6.3, with both the input and output power waveforms. Current and power dissipation waveforms are illustrated in Figure 6.4 for one of the rectifiers. Note that the RMS current is 20 amps and the loss per rectifier equals 4 watts which agrees
precisely with equation 6-1. This fact or finding also explains the low efficiency since six devices with a power loss of 4 watts each produces a loss of 24 watts which is responsible for 70% of the power loss represented in Figure 6.3. Based on this analysis as predicted in section 6.1, the 1.5V, 100 watt design with six devices, places the rectifiers in the higher loss region with the resulting impact on efficiency.

A second simulation was conducted with the same 1.5V circuit at a 75 watt power level. This model includes the winding losses but does not included any losses due to the implementation, such as losses in the wirebonds and traces. The result is an efficiency of 87% as illustrated in Figure 6.5. Note that very high efficiencies are possible even at these current levels since the rectifiers are operating just barely within the low loss region of Figure 6.1.

### 6.3 Incorporation of Parasitic Effects into Circuit Model

As in the case of the 3.3 V and 2.5 V designs, a simulation was performed in order to evaluate the parasitic effects of the implementation of the converter. Based on the results from the 2.5 V and 3.3 V cases, only DBC implementations were evaluated. Other implementation options were not considered since they are not realistic for the current levels observed in this design.
Figure 6.2 : Output of a 1.5V converter including winding loss operating at 100watt.
Figure 6.3: Performance of a 1.5V converter including winding loss operating at 100watt.
Figure 6.4: Current and loss in an output rectifier for a 1.5V design.
Figure 6.5: Performance of a 75 watt, 1.5V converter including winding loss.
The same procedure was utilized as in the 2.5 V and 3.3 V cases, however, the values were modified to reflect the connections due to the additional pair of rectifiers. The results from this simulation are shown in Figure 6.6, with an efficiency of 84%. While this is a nontrivial decrease caused solely by the interconnects, this circuit would be of practical value and could be realistically constructed on 12mil DBC Aluminum nitride.

6.4 Summary and Conclusions

Designs with output voltages below 2 volts and power levels above 50 watts are possible, however, great care must be given to manage the rectifier output losses. Parallel rectifiers can be used in order to share the current while maintaining each rectifier at a low loss current level.

In addition, 1.5 V supplies with up to 75 watt power levels have been demonstrated through simulation. Power levels beyond 75 watts may be unrealistic with current rectifier on resistance values without resorting to a large number of rectifiers.
Figure 6.6: Performance of a 75 watt, 1.5V converter implemented in 12 mil DBC.
CHAPTER 7  

Miniaturized Control Circuit

7.1 Requirements of Control Circuit

As discussed in previous Chapters, the requirements for the control section of most converters are radically different than those of the power stage. This issue can create problems for some technologies, however, it can also be an opportunity for innovative technique(s) of implementation. Potential problems arise from the fact some of the techniques used to create high power circuitry are not ideal for fine pitch low power circuitry. For example, an ASIC controller with a large number of I/O would be difficult to accommodate within a DBC substrate, due to the inability to produce fine lines and features with DBC technology. On the other hand, opportunities arise from the fact that design of the control section is largely freed from the onerous constraints of the power stage with its extreme constraints on thermal management and high current levels. In addition, for most of the
control signals the high voltage requirements are also relaxed, although a small number of high voltage signals may exist within the control circuit.

Figure 7-1 illustrates the schematic for the control portion of the prototype converter used in this research study. In comparison to the high power stage design, the control stage can be miniaturized using much of the machinery developed for low power digital and analog applications. This includes Flip Chip, Chip Scale Packages, as well as Multichip Module implementations. The particular type of implementation depends on the applications requirements. Many applications require low cost, while the overall size is not important. On the other hand, other applications are less cost sensitive and a high priority is placed on size and weight.

This control circuit is based on a pulse width modulation chip (PWM) and two driver ICs. The PWM chip generates the gate drive waveforms based on feedback from the output and the driver ICs provide the drive current and isolation for the power switches.

7.1.1 Active Devices

The heart of the control circuit is a Pulse Width Modulation Chip. This device is an analog small scale Integrated Circuit (IC) with approximately 10 I/Os. Two driver chips are utilized, which are also analog ICs with approximately 10 I/Os each. These devices are nominally 90 mils square, and are top surface metallized with aluminum. The back side of these devices are non active (they do not serve as electrical contacts) and are often metallized with nickel. In addition, a small number of discrete active components are included in the design. These devices include Schottky and Zener diodes as well as a bipolar transistor. Most of these discrete actives are small in size ranging from 30 -100 mils square.
Appendix A includes data sheets, package configuration illustrations, as well as bare die sizes and configurations for the components utilized in implementing this circuit.

### 7.1.2 Passive Components

One of the challenges of this type of control circuit is the passive components that are required. Typically, a number of resistors and capacitors are needed to provide decoupling, RC time constants, as well as voltage division for feedback and other electrical functions.
In this design, approximately 10 resistors and 10 capacitors are needed in the control circuit.

The resistors are reasonably achieved for this circuit since the majority of them are midrange values ~1-100 K and all are low power rating. The only real challenge is that in some cases, the exact resistance value is difficult to determine prior to the implementation of the circuit. For example, adjustment of the dead time is accomplished by an RC time constant and can vary with the parasitic effects of different power stage implementations. As a result, implementation of this RC time constant in an integrated form effectively “locks” in a dead time. Similarly, the feedback is adjusted by a set of resistors which divides the output voltage and feeds this signal back into the PWM chip. Integration of these resistors in a compact form also “locks” in the output voltage. This presents a major problem in the prototype stage but less of a problem in the final production environment.

The capacitance in this circuit is more challenging, primarily due to the large values which are required. In order to adequately decouple the ICs, a capacitance of ~ 10 µF is required. This is due to the fact that the PWM and driver chips are required to source large current spikes and the input voltage to these devices must be capable of providing these sharp spikes of power. The decoupling capacitance serves to locally store a quantity of energy in close proximity to the device in order to meet this demand. In addition, large voltage spikes are common in converter circuits of this nature due to the switching voltages in the power stage. The decoupling capacitance must filter out these voltage spikes and provide a clean power source to each IC. The real challenge is producing these large capacitance values in a compact form factor. Fortunately, only low voltage rating are needed, however, capacitors are commonly 120 mils x 80 mils in size.
In addition, several smaller value capacitors are needed for RC time constants and other functions. These elements are all low voltage low value components that are relatively easy to integrate into a compact control design.

This design also makes use of high voltage driver ICs and as a result does not require any magnetic components for isolation. As a result, no inductors or transformers are utilized in the control design.
7.1.3 Isolation & Parasitics

Other than interconnection and implementation of the individual components in the control circuit, the chief concerns of this type of circuit design must be providing adequate isolation and minimizing parasitic effects. The need for isolation arises from the fact that points within the control circuit, such as the connection between the midpoint of the half bridge and the HIP2100 driver, must withstand voltages up to ~70 Volts. This is not an extreme requirement, however, as the control circuit shrinks in size, this issue must be considered in order to provide adequate space. Normally, a safety factor of at least 2 should be assumed. Also, note that the breakdown voltage of air is a very strong function of the humidity. This difference can lead to an order of magnitude different breakdown strengths for a converter, in Nome Alaska on a cold dry day versus southeast Asia on a hot summer day. In general, these issues must be considered in the implementation of a specific design.

Parasitics are also a key issue since this type of analog circuit can be sensitive to parasitic inductance on the circuit interconnects. For example, inductive interconnections of ground connections to the PWM and drivers ICs can reduce the effectiveness of the decoupling capacitance, or even mandate large values. Similarly, inductive interconnects to the gates of the power switches can alter the dead time or other key circuit parameters and reduce the overall circuit efficiency.
7.2 LTCC Controller Design & Fabrication

7.2.1 LTCC Controller Design

The miniaturized control was fabricated using Low Temperature Cofired Ceramic. Low Temperature Cofired Ceramic (LTCC) was selected as the material of choice, since this technology offers fine line resolution, with adequate thermal conductivity, and high...
circuit density. The design was based on four 8 mil thick ceramic layers to provide a final fired thickness of approximately 24 mils. These four dielectric layers allow for five metal layers including the back side of the bottom layer. Two of the layers are used for signal routing, while the others form the land grid array on the back surface, and separate power and ground planes. The goal of this design was to minimize the total foot print of the control circuit. The multilayer design is illustrated in Figure 7-2, while each individual layer is illustrated in Figure 7-3.

Both silver and mixed metals implementations of the design were developed in this work. The mixed metal system allows for the low cost of silver with the high reliability of gold conductors on all external surfaces. Some of the passive components were integrated into the substrate in the form of thick film resistors, which were laser trimmed to a tight 1% tolerance. Device attachment was performed using screen printed solder, solder preforms, or conductive adhesive and 1 mil aluminum wedge bonds.

Blind and buried vias, 6 mil in diameter, through the control module layers provide electrical connections to the internal routing layers, as well as to the land grid array on the back surface of the module. This land grid array is composed of 8 I/O pads which mate with interconnections on the power board, to provide electrical and mechanical connections to the MCM controller.

7.2.2 Fabrication Process

The LTCC control MCMs were fabricated in a four up panel, which allowed four circuits to be fabricated from a single 3 inch square panel of LTCC, as shown in Figure 7-4. The general process of the LTCC fabrication are discussed in detail in Chapter 3,
however, it will be informative to discuss the details of this particular circuit’s fabrication. Figure 7-5 illustrates a flowchart of the fabrication process for the reader’s reference.

Each layer was blanked out to a 3”x3” size from a 12” roll of Dupont 851AT or similar LTCC tape. This blanking process formed each layer of the module as well as cut the registration marks which are needed to align the vias and conductors to each layer and ultimately the layers to one another. A manual blanking press was used for this step of the process.

Drill files which contain the coordinates of each via or cut that needs to be performed were created from the original design in ORCAD. These files are converted into a format compatible with the Nd:YAG laser. These files are included as Appendix B. The result is an individual file for each separate layer.
Each layer of the module was placed on the laser stage and held in place via vacuum. The laser automatically performs the needed cuts via computer control. A typical layer for this module after laser processing is illustrated in Figure 7-6. The layers are then inspected for defects using an optical microscope. At this point, the layers are ready for the printing processes which fill each via and create the metallization for interconnects on each layer.

A Presco 465 printer equipped with a porous stone vacuum chuck was used to hold the green LTCC sheets in place during the printing process. Vias were filled using Dupont 6141 or similar via fill pastes and contact printing. The masks used for this printing process were 1 mil thick stainless steel cut using the same laser files and Nd:YAG laser. The layers were dried and inspected and then the conductors were printed using stainless steel screens with a screen mesh size of 325, at 45°, 0.9 mil configuration. Dupont 6142 or similar conductive inks were used for this process. The layers were then dried and
individually inspected. After each of the layers had been inspected and verified, the layers were laminated together using an isostatic laminator and conditions appropriate for the LTCC material in use. The parts were then ashed and fired in a two step process.

The bottom and top metallizations as well as integrated resistors were deposited using screen printing after the substrates were complete. This is necessary since most of the cofired metallizations suffer from poor solderability due to the high glass content in the film. The parts are then refired in order to sinter these metallizations and resistors.
Singulation of the parts was achieved through post machining after firing with an Nd:YAG laser. In the initial design, the notch in the upper left corner was post machined. This approach left the corner of the L shape with significant stresses, which lead to reliability concerns and even cracking in some cases. As a result, a revised design was developed in which a square area which encompasses the notched area was premachined prior to firing using an Nd:YAG laser. Final singulation of the MCM substrates was still performed in a post machining process. The final dimensions for this MCM controller were 0.9” x 0.5”. A partially singulated initial prototype is illustrated in Figure 7-7.

7.3 Electrical Performance

This compact controller was tested in a stand alone mode as well as with the intended power stage. The electrical performance was as expected, and is illustrated in Figure 7-8.
The green waveform, number 1, is the signal generated by the PWM chip to examine the feedback signal. The duty cycle of this waveform will shift in order to maintain a constant 3.3V output level. The red and blue waveforms, number two and three, respectively, are the low side and high side gate drive signals. These signals are just mirror images of the PWM signal, however, the high side gate drive is inverted. Also, the high side waveform is referenced to the center of the half bridge, in order to drive the gate of the high side MOSFET with respect to its source.

Figure 7-8: Electrical waveforms from LTCC Controller.

The green waveform, number 1, is the signal generated by the PWM chip to examine the feedback signal. The duty cycle of this waveform will shift in order to maintain a constant 3.3V output level. The red and blue waveforms, number two and three, respectively, are the low side and high side gate drive signals. These signals are just mirror images of the PWM signal, however, the high side gate drive is inverted. Also, the high side waveform is referenced to the center of the half bridge, in order to drive the gate of the high side MOSFET with respect to its source.
7.4 Conclusions

Using LTCC, a very compact controller circuit has been developed which is several times smaller than a conventional PCB design. This unit was fabricated from four layers of LTCC and is a land grid array, which solders directly to a power stage substrate. In this way, the electrical and mechanical connections to the power stage are completed in one simple step.

Electrical results and data demonstrate that this LTCC MCM part offers identical performance to a conventional design, with the added benefits of greatly reduced volume and weight.
8.1 Design

8.1.1 Electrical Considerations

Although the schematic, as illustrated in Figure 8-1, for the power stage appears simple, the implementation of this design in a compact manner with high efficiency is complicated. This arises from two primary problems, namely,

- The need for minimum parasitics in the power stage. In particular, parasitic resistance decreases the efficiency and increases the dissipated power which must be conducted away from the power converter as heat.

- Proper thermal management in order to maintain the devices within safe operating temperature ranges. In general, the reliability and efficiency of
a power circuit is inversely proportional to the maximum device temperatures.

Examination of the schematic reveals that the power stage can be broken into two sections; the primary, and the secondary. The primary side of the circuit is a high voltage low current halfbridge, while the secondary is a low voltage high current rectifier. Normally, 35-70 Volts is applied to the input side, which then draws approximately 1 amp of current. The secondary side voltage is only a few volts, however, load currents up to 33 amps are required.

For the primary side, the main electrical design consideration is that adequate spacing be provided in order to prevent voltage breakdown, and that parasitic inductance is minimized by maintaining short trace lengths. In contrast, the secondary design is dominated by the need for short wide traces to provide interconnections with minimum resistance. In addition, fusing currents must be considered in order to prevent fusing wirebonds or other interconnect structures. Consideration must also be given to the interconnection of the control and power circuits. The control circuit, discussed in Chapter

Figure 8-1: Schematic of Power Stage Circuit.
Design

7, is designed to be integrated into the power stage, however, the interconnects between the individual power circuit elements and the controller should be as short as possible. In particular, inductance and noise on the gate drive signals can cause ringing of the halfbridge which reduces the circuits efficiency and can be destructive in severe cases to the halfbridge driver and MOSFETs. These parasitics are problematic since they modify the speed at which the power switches turn on and off. In a half bridge configuration, the correlation between the on time of the high side and low side MOSFETs is usually specified by a “dead time” where both devices are turned off. Short dead times can result in both devices turning on simultaneously which shorts the input power to ground. Too long of a dead time reduces the circuit efficiency and increases the output ripple.

8.1.2 Thermal Management

Due to the significant power loss expected in this circuit, at least 5 to 10 watts, thermal management cannot be ignored. This generic term includes the consideration of all of the materials, and interfaces which exist between the power sources and the heat sink. As discussed in earlier Chapters, this circuit is designed to mount to a water cooled card or other heatsink. As a result, great care must be given to the substrate materials and components attachment. The substrate should be as thermally conductive as possible and the number interfaces should be minimized.

In addition, to the selection of the substrate material greater care must be observed in the attachment of all of the heat generating components to the substrate. In particular, the transformer and power devices must be in intimate void free contact with the substrate.
8.1.3 Design Strategy

Based on these issues and the need for minimum size, a design strategy was developed and it is illustrated in Figure 8-2. The foundation for the converter is a DBC AlN or BeO substrate, which provides the mechanical support for the power supply, thick conductors for the secondary circuit, and an effective thermal path for heat flow to the heatsink. Although, both AlN and BeO provide similar results, AlN was utilized for the bulk of this work. This DBC AlN substrate is etched on one side in order to provide the circuit traces, while the other side is not etched to form a complete copper plane which can be used for mounting the substrate to the card assembly. The copper traces are plated with a nickel / gold finish to promote wirebonding and to prevent oxidation of the copper. A pure nickel finish would normally be used in the production of this type of circuit since a nickel finish is more suitable for Aluminum wirebonding, and Pb/Sn solder. All of the active components are utilized in a bare die format, which are soldered directly to the AlN DBC using Sn 62 (62% Sn, 36% Pb, ~2% Ag). Electrical connections to the top side of the devices were completed using 5, or 10 mil aluminum wedge bonds.

The transformer was included in this circuit as a planar magnetic component with the core of the device bonded directly to the AlN DBC. A vendor supplied winding prepared from Flex circuitry was used to minimize the total height of the transformer. Thick copper metallization used to form the winding was soldered directly to the DBC circuit traces in order to minimize both the thermal and electrical resistance of these connections. An E & I core set were used and attached to the DBC substrate with thermally conductive adhesive.
Control signals from the various devices were provided by the etched copper traces in the DBC, which also provided the sites for mechanical connection of the LTCC controller using Sn 62 solder.

8.2 Fabrication

8.2.1 DBC Substrate

A panel of 12 mil thick DBC copper 2” x 3” was etched using the artwork illustrated in Figure 8-3, to form two of the power stage circuits in one process cycle. Dry film photoresist was applied to the panel on both sides and one side was exposed through the required artwork, while the other side was exposed completely. The panel was then developed in a spray exposure system using a Sodium Bicarbonate solution. A spray
etching system with a Sodium Persulfate solution was then used to etch the DBC panel and form the required circuit traces.

The panel was then plated using an electroless Phosphorous Nickel solution, followed by a cyanide based electroless gold process. The result is a thin Nickel / Gold finish that is ideal for wirebonding and solder wetting. In a production module, the gold

*Figure 8-3 : Two up design of power stage circuits on a 2” x 3” panel of DBC.*
process would most likely not be included since it would likely decrease the modules reliability through the formation of intermetallics in the aluminum wirebond connections. In addition, care must be taken in the use of tin solders on gold finishes due to the strong solubility of gold in tin. Tin solders will leach the gold coating, forming a mechanically weak solder joint. However, for prototype applications, the author has used the gold finish to improve the wirebonding yield, since gold is much easier to bond to than nickel. After the substrate panels were prepared, a diamond saw was used to section the panel into to separate circuits.

8.2.2 Assembly

Assembly of the circuit was accomplished through reflow soldering and wirebonding. Solder preforms of Sn 62 were cut from a ribbon of 2 mil thick solder, for each component. Indium Corporations 5RMA flux was used sparingly with the solder preforms and a Sikima 5x5 conductive reflow oven to attach the individual components to the board. The bare dice were soldered initially followed by wirebonding and then the attachment of the remaining components and the I/O connections were performed.

An Orthodyne model 20, semiautomatic wirebonder, equipped with 10 mil aluminum wire was utilized to wirebond the source connections of the halfbridge MOSFETs as well as the Synchronous rectifiers. Two ten mil bonds were placed on each of the primary side FETs, while 4 or 5 ten mil bonds were formed on the secondary synchronous rectifiers. Selection of the number of bonds was largely determined by the available source area and the wedge bond foot size. The same wirebonder equipped with 5 mil wire was utilized to create the gate connections to these devices. Only one gate bond was formed due to the small gate size and lack of current flow through these connections.
The final assembly step included the attachment of the transformer core to the substrate through the use of Epoxy Technologies H70E thermally conductive adhesive. H70E was selected since this material is thermally conductive, it serves as an electrical insulator, and it can be cured at low temperature (~100 °C). The need for an electrical insulator and thermal conductor arises from the fact that this type of ferrite core (Phillips E/I 22, in 3F3 material, see appendix A) is highly conductive and needs to be electrically isolated from the rest of the circuit. However, thermal conduction to the substrate is
critical for maintaining the transformer operating at a low temperature. The components which form the transformer are illustrated in Figure 8-4, while the completed transformer is illustrated in Figure 8-5.

Figure 8-6 illustrates a prototype converter without the integrated control stage.

![Power stage of prototype converter without control stage. The connector at the top left of the circuit was used to provide power and control connections during preliminary testing. Note the traces used for the connector are designed to mate with the control MCM.](image)

The controller was soldered to the substrate at the same time as the other components using the same Sn 62 solder. However, the Sn 62 solder was applied to the controller connections in a paste form rather than as a preform. Sn 62 was selected since it is compatible with the silver traces found on bottom side of the control circuit, due to the silver content. These solder connections serve as the electrical and mechanical connections from the power stage to the control stage.
8.3 Results

8.3.1 Electrical Performance

After final assembly, the prototype circuit was evaluated for functionality and electrical performance potential. For most of the testing work, the control stage was
powered separately with an external supply. This simplifies the startup process and allows for the current delivered to the control to be monitored.

The initial measurements revealed that the deadtime of the circuit was not optimum which required two resistors in the control portion of the circuit to be modified. The resistors were removed and new ones were installed. Dead time is important for the halfbridge portion of this circuit since if both switches are on at the same time for even a few microseconds, this would effectively short the input to ground which is catastrophic for the circuit efficiency and may also damage the circuit.

Once the deadtime was adjusted, the circuit operation was improved, with an initial turn on voltage of just over 40 volts required to active the 3.3V output regulation, the circuit delivered a highly regulated 3.3 V output with minimum ripple. The control circuit
required approximately one half of a watt of power for proper operation while the overall circuit efficiency was ~ 90% depending on the load power.

For this type of circuit, the overall efficiency typically varies with output power. Normally, the efficiency is lower for both high and low output power levels and peaks near the middle of the power range. This type of behavior was observed in the prototype circuit as illustrated in Figure 8-8. Measurements revealed that the deadtime was still not completely optimized and that some of the power loss may be due to cross conduction in the primary halfbridge. However, modification of the passive components in the control stage is very difficult, and no further optimization was pursued at this time. As a result, it may be possible to further enhance the efficiency of this circuit through the optimization of the control stage.

8.3.2 Thermal Performance

The thermal performance of this circuit was remarkable. Thermal performance was tested using the circuit pressed against a small heatsink under natural convection conditions. With the full rated load, the active components operated at temperatures less than 40 °C. The highest temperatures were observed for the transformer, which routinely operated in the 80-90 °C range. These results illustrate the effectiveness of this strategy.

Power loss and temperature are synonymous. Therefore, these results seem to indicate that much of the power loss is related to the transformer. Contributing to these elevated temperature levels is the increased thermal resistance provided by the thermally conductive adhesive used to attach the transformer as compared to the solder used for the active components.
CHAPTER 9  

Summary of Findings

9.1 3.3 Volt. 100 watt Converter

9.1.1 Electrical Simulation

As discussed in detail in chapter 4, the electrical simulation of the 3.3V 100watt converter design, previously developed and published by other researchers, demonstrates that this voltage and power level are possible with relatively high efficiencies in a number of implementation schemes.

A summary of the efficiency data produced by the simulations is illustrated in Figure 9.1. Recall that the “ideal” circuit represents the losses caused by the components themselves without interconnects or transformer winding losses, while the “winding loss” configuration includes the ideal as...
well as transformer winding loss components. The other four values represent simulated efficiencies for the IMS/PCB, DBC 12 mil, DBC 8 mil, and Thick Film respectively. Note that the winding loss is a nontrivial part of the loss, and in fact for the cases of the 12 mil and 8 mil DBC, the winding loss is larger than the losses created by the rest of the secondary circuit interconnections.

![Efficiency Graph](image)

*Figure 9.1: Summary of 3.3V simulations.*

Each of the technologies illustrated in Figure 9.1, has a number of advantages and limitations from cost, reliability, and mechanical points of view, however, from an electrical point of view the advantages of direct bond copper are clear. It is also interesting
to note that at this current level, little difference exists between the 8 mil and 12 DBC simulations. As a result, 8 mil DBC or AMB may be ideal for these supplies since the reliability of the 8 mil metal may be better than the 12 mil metallization due to the CTE mismatch between the copper and the ceramic substrate.

Both IMS and PCB are more attractive from a cost standpoint, however, the conventional metallizations used in these approaches reduces the overall efficiency of the circuit by 6%. In addition, the associated thermal losses will reduce the overall reliability of the circuit since in general circuit reliability is inversely proportional to operating temperature. These problems may be reduced through the use of thicker metallizations, however, much of the cost advantages may be lost if unusually thick metallizations are required of IMS or PCB vendors.

These simulations also illustrate the fact that conventional thick film is not suitable for high current converters. This fact is not surprising, and it may be that through the use of thicker metallizations and or other means such as solder coated metallizations the efficiencies could be improved. However, it is unlikely that these approaches could compete with DBC or AMB on a cost or performance basis.
9.1.2 Design and Fabrication

Based on the simulations, the converter described in chapters 7 and 8 was designed and fabricated using 12 mil DBC on aluminum nitride. The strategy utilizes the DBC substrate as the foundation and support for all of the other components as well as the power conductors. An integrated MCM control module has been included directly on the board and provides all of the necessary support functions. In addition, a planar transformer was used in order to minimize the secondary losses and reduce the overall converter height.

The power stage circuit was fabricated in a two up configuration on a DBC AlN substrate. All of the active devices were soldered directly to the DBC conductors which were plated with a Nickel and then Gold finish. Sn 62 solder was utilized throughout. Source and gate connections to the devices were made with 5 and 10 mil aluminum wedge bonds.

LTCC technology was utilized to fabricate the control module, based on four layers of ceramic tape. The control utilizes a number of integrated resistors and chip and wire assembly for inclusion of the active components. The entire MCM is a land grid array and solders directly to the DBC substrate to provide both a mechanical and electrical connection to the main power circuit.
9.1.3 Results & Comparison to Simulation

This electrical and thermal performance of this prototype was very promising with an overall efficiency of 89-91% (depending on the load conditions). In addition, the thermal performance was also quite attractive since the semiconductor devices operated at full power with temperatures under 50 °C. The greatest temperatures were found in the magnetic component due to its proportionally high level of loss as well as its increased thermal resistance through the winding to the DBC substrate.

Based on the excellent performance, compact footprint and minimal volume and height, this type of implementation is attractive for a variety of applications. In addition, this converter's performance agrees well with the simulated 12 mil DBC performance to within a few percent.

9.2 2.5 Volt, 100 watt Converter

9.2.1 Electrical Simulation

Using a similar technique and model as that developed for the 3.3V design, a 2.5V design was simulated, which represents a modification developed by the author to a previously published design. This design differs in the magnetic design and secondary drive. The efficiency results are summarized in Figure 9.2
Similar to the 3.3V case, an “ideal” efficiency of 88% was realized, excluding winding loss and interconnect losses. Incorporation of the winding loss reduces the efficiency to 87%. Each of these technologies was simulated with resulting efficiencies ranging from 86 to 57%.

The printed circuit board and IMS designs begin to show the effects of the 40 amps of current required by this design. With a drop in efficiency of 6%, the losses in the interconnects are significant. Very careful layout of the secondary interconnects would be
required to develop this circuit in a PCB or IMS implementation due to the several watts of power consumed in these interconnects. There may be a real danger of over heating or even damage of the FR-4 board, as well as fusing of the conductors.

While thick film may be able to reliably handle the type of power loss exhibited by this simulation, due to its ceramic foundation, the efficiency of 57% is clearly unacceptable for any application. Conventional thick film is clearly out of the question for these lower voltage, high power designs.

As expected, the direct bond copper simulations provided the highest level of performance. At 86% and 85% for 12 mil and 8 mil DBC, respectively, this technology is clearly the ideal choice from an electrical perspective. It is interesting to note, that unlike the 3.3V case, the 2.5V case is beginning to show the effects of added thickness of metallization for the 12 mil and 8 mil simulations.

Again, as in the case of the 3.3V design, the effects of the winding loss are dramatic when compared against the entire losses in the secondary for the DBC cases. Careful design of the secondary winding and its interconnection to the rest of the power circuit is warranted.
9.3 1.5 Volt Converter

9.3.1 Electrical Simulation

Although significant challenges exist for lower voltage designs, a successful 1.5V design has been demonstrated through simulation. This design is very similar to the 2.5V designs, however, the secondary has been modified to handle the additional current and to provide a lower voltage output. Six output rectifiers are now used rather than the conventional four. A summary of the performance results is illustrated in Figure 9.3.

At a 100 watt power level the output rectifiers are operating at such high current levels that the losses are most likely to great for most applications, even though the circuit now utilizes two sets of three rectifiers which share the current. The net effect is an efficiency of 75% including winding losses. Approximately 70% of this loss is in the rectifiers themselves. However, when the power level is reduced to 75 watts, the current demand is reduced sufficiently to allow an efficiency of 87%, which is similar to the high operating efficiencies found in the 3.3V and 2.5V cases.

The only technology case that was used to evaluate the effect of parasitics on the circuit was the 12 mil DBC. While 8 mil DBC is probably not unrealistic, the other implementation options, namely PCB, IMS, and Thick Film are out of the question due to the high current levels. The 12 mil DBC simulation yielded an efficiency of 84%, which
represents a drop of 3 percentage points. However, with an overall efficiency of 84%, this circuit would be viable for a number of applications.

![Figure 9.3: Summary of 1.5V simulations.](image)

9.4 Summary and Conclusions

Simulations were used to determine the effects of the transformer construction and packaging implementation on the performance of 3.3V, 2.5V, and 1.5V DC to DC converters. The results indicate that for the 3.3V case, and to some degree the 2.5V case,
an implementation scheme based on PCB or IMS technology would be viable solutions from a performance perspective. However, conventional thick film would suffer greatly from losses within the conductor and is not an attractive option for any of these voltage and power levels. Similarly, DBC has been shown to be the star of the available options from an electrical perspective.

The 1.5V design cases illustrates the effect of increased current levels caused by the reduced voltage levels. While 1.5V designs at 75 watts of power are possible, careful design is needed to ensure reliable circuit performance with high efficiency. In this case, DBC is most likely the only option due to the extreme current levels and stringent thermal management demand.

In addition, a 3.3V converter with a power rating of 100 watts has been developed with an efficiency of 90% and an overall power density of 157 watts / in³. This unit is very compact and size, height, and overall volume, and is ideal for card mounted local power supply applications. The agreement between the measured results from this converter and the simulated 3.3V results validates the models developed within this work.


10.1 Conclusions

Low voltage circuits are far more challenging for power supply designers than the conventional higher voltage circuits. This fact coupled with what appears to be a trend toward increased system complexity will mean that the next generation of electronics will not be compatible with the current existing state of the art DC/DC converter.

The author has shown through simulations that 3.3 V, and 2.5V designs can be fabricated with high efficiency up to and in some cases beyond 100watt power levels.
Future Requirements and Directions

A 3.3V design utilizing an optimized packaging strategy developed by the author validates these simulations and illustrates the need for more advanced packaging technologies which can handle these large currents. This design yielded an efficiency of 90% with an overall power density of 157 watts / in³.

In addition, converters without output levels as low as 1.5V are possible, however, these supplies are not realistic above ~50-75 watts due to the large number of output rectifiers that would be required and their associated high cost.

10.2 Future Requirements and Directions

Two primary limitations are highlighted by this work; the on resistance of the current state of the art rectifier as well as the need for an improved transformer.

With on resistance values of ~10 mΩ, the current generation of devices is inadequate for very low voltage high power supplies. Devices are needed with on resistance values of at least half of the current generation of devices. To illustrate this point the author has fabricated and tested a 50 watt, 3.3V converter using an experimental GaAs VFETs in the output stage. The converter is illustrated in Figure 10.1, while the on-resistance of the device including the source connection wirebonds is illustrated in Figure 10.2.
Figure 10.1: Prototype 3.3V, 50 watt Converter based on experimental GaAs Device.

On Resistance of GaAs VFET

Figure 10.2: On-resistance of experimental GaAs VFET device versus current.
Note that this device offers approximately half the losses of the current generation of silicon rectifiers.

The advantage of these devices is illustrated in Figure 10.3, as compared to conventional rectifiers. This device could operate at much higher current levels with lower losses than either the current generation of Schottky rectifiers or synchronous rectifiers.

Regrettably the device is much more difficult to utilize since it is composed of fragile GaAs and operates with in a normally on mode. This mode of operation is the opposite of conventional silicon devices which are normally off. The normally on mode of operation is more complicated to drive and control, and as a result wide spread adoption of this new device would not be easy in spite of its excellent performance. In addition, the cost of this device is estimated to be significantly higher. Based on these issue the manufacturer of this particular device has decided not to pursue production. However, other companies are working on devices with reduced on-resistance and these devices should become available in the next few years.

In addition to the rectifier losses, the losses in the transformer are a major causes of concern from both a reliability and efficiency standpoint. Since reliability is generally inversely proportional to the maximum temperature, the transformer is most likely the weak link in these converters.
The author proposes to improve these converters and eliminate these problems by using a new planar magnetic design which implements the secondary portion of the transformers windings with the direct bond copper metallization. This will be accomplished by cutting slots in the AlN substrate for the core legs to protrude through, with the E portion of the core on one side of the substrate and the I core on the other side of the substrate. The primary could be implemented using either a DBC layer or with a laminated flex circuit. At the time of publication a vendor has been contacted to fabricate some initial prototype substrates based on this design concept. In addition, a patent disclosure is planned.

*Figure 10.3: Losses in available rectifiers versus an experimental GaAs VFET device.*
Utilizing the next generation of low on-resistance rectifiers and this modified transformer design, converters with output voltages as low as 1V, with power ratings of 100 watts should be possible in very compact form factors with high efficiency.
References


Appendix A

Data Sheets for Components Utilized in the Converter Design.
HIP2100

100V/2A Peak, Low Cost, High Frequency Half Bridge Driver

Features
- Drives N-Channel MOSFET Half Bridge
- Space Saving SO8 Package
- Bootstrap Supply Max Voltage to 116VDC
- On-Chip 1Ω Bootstrap Diode
- Fast Propagation Times Needed for Multi-MHz Circuits
- Drives 1000pF Load at 1MHz with Rise and Fall Times of Typically 10ns
- CMOS Input Thresholds for Improved Noise Immunity
- Independent Inputs for Non-Half Bridge Topologies
- No Start-Up Problems
- Outputs Unaffected by Supply Glitches, HS Ringing Below Ground, or HS Slewing at High dv/dt
- Low Power Consumption
- Wide Supply Range
- Supply Undervoltage Protection
- 3Ω Output Resistance

Applications
- Telecom Half Bridge Power Supplies
- Avionic DC-DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

Description
The HIP2100 is a high frequency, 100V Half Bridge N-Channel MOSFET driver IC, available in 8 lead plastic SOIC. The low-side and high-side gate drivers are independently controlled and matched to 8ns. This gives the user maximum flexibility in dead-time selection and driver protocol. Undervoltage protection on both the low-side and high-side supplies force the outputs low. An on-chip diode eliminates the discrete diode required with other driver ICs. A new level-shifter topology yields the low-power benefits of pulsed operation with the safety of DC operation. Unlike some competitors, the high-side output returns to its correct state after a momentary undervoltage of the high-side supply.

Ordering Information

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<th>TEMPERATURE RANGE</th>
<th>PACKAGE</th>
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<td>HIP2100IB</td>
<td>-40°C to +85°C</td>
<td>8 Lead Plastic SOIC (N)</td>
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</table>

Features
- Drives N-Channel MOSFET Half Bridge
- Space Saving SO8 Package
- Bootstrap Supply Max Voltage to 116VDC
- On-Chip 1Ω Bootstrap Diode
- Fast Propagation Times Needed for Multi-MHz Circuits
- Drives 1000pF Load at 1MHz with Rise and Fall Times of Typically 10ns
- CMOS Input Thresholds for Improved Noise Immunity
- Independent Inputs for Non-Half Bridge Topologies
- No Start-Up Problems
- Outputs Unaffected by Supply Glitches, HS Ringing Below Ground, or HS Slewing at High dv/dt
- Low Power Consumption
- Wide Supply Range
- Supply Undervoltage Protection
- 3Ω Output Resistance

Applications
- Telecom Half Bridge Power Supplies
- Avionic DC-DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

Pinout

Application Block Diagram

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1995
**Functional Block Diagram**

![Functional Block Diagram](image)

**Other Applications**

![Other Applications Diagram](image)

**FIGURE 1. TWO-SWITCH FORWARD CONVERTER**

**FIGURE 2. FORWARD CONVERTER WITH AN ACTIVE CLAMP**
Specifications HIP2100

**Absolute Maximum**

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<td>CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the recommended operating conditions of this specification is not implied.</td>
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**Recommended Operating Conditions**

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**Electrical Specifications** \( V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO, Unless Otherwise Specified**

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<td>( I_{VDD-HB} = 100\mu A )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>High-Current Forward Voltage</td>
<td>( V_{DH} )</td>
<td>( I_{VDD-HB} = 100mA )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Dynamic Resistance</td>
<td>( R_{D} )</td>
<td>( I_{VDD-HB} = 100mA )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>LO GATE DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Level Output Voltage</td>
<td>( V_{OLL} )</td>
<td>( I_{LO} = 100mA )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>High Level Output Voltage</td>
<td>( V_{OHL} )</td>
<td>( I_{LO} = 100mA ), ( V_{OHL} = V_{DD} - V_{LO} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Peak Pullup Current</td>
<td>( I_{OH} )</td>
<td>( V_{LO} = 0V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Peak Pulldown Current</td>
<td>( I_{OL} )</td>
<td>( V_{LO} = 12V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>HO GATE DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Level Output Voltage</td>
<td>( V_{OLH} )</td>
<td>( I_{HO} = 100mA )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>High Level Output Voltage</td>
<td>( V_{OHH} )</td>
<td>( I_{HO} = 100mA ), ( V_{OHH} = V_{HB} - V_{HO} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Peak Pullup Current</td>
<td>( I_{OHH} )</td>
<td>( V_{HO} = 0V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Peak Pulldown Current</td>
<td>( I_{OLH} )</td>
<td>( V_{HO} = 12V )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A</td>
</tr>
</tbody>
</table>
Specifications HIP2100

Switching Specifications  \( V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, \) No Load on LO or HO, Unless Otherwise Specified

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>( T_J = 25^\circ C )</th>
<th>( T_J = -40^\circ C )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower Turn-Off Propagation Delay (LI Falling to LO Falling)</td>
<td>( t_{LPHL} )</td>
<td>-</td>
<td>20</td>
<td>35</td>
</tr>
<tr>
<td>Upper Turn-Off Propagation Delay (HI Falling to HO Falling)</td>
<td>( t_{HPHL} )</td>
<td>-</td>
<td>20</td>
<td>35</td>
</tr>
<tr>
<td>Lower Turn-On Propagation Delay (LI Rising to LO Rising)</td>
<td>( t_{LPLH} )</td>
<td>-</td>
<td>20</td>
<td>35</td>
</tr>
<tr>
<td>Upper Turn-On Propagation Delay (HI Rising to HO Rising)</td>
<td>( t_{HPLH} )</td>
<td>-</td>
<td>20</td>
<td>35</td>
</tr>
<tr>
<td>Delay Matching: Lower Turn-On and Upper Turn-Off</td>
<td>( t_{MON} )</td>
<td>-</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>Delay Matching: Lower Turn-Off and Upper Turn-On</td>
<td>( t_{MOFF} )</td>
<td>-</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>Either Output Rise/Fall Time</td>
<td>( t_{RC,IFC} )</td>
<td>( C_L = 1000\mu F )</td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td>Either Output Rise/Fall Time (3V to 9V)</td>
<td>( t_{IR,IF} )</td>
<td>( C_L = 0.1\mu F )</td>
<td>-</td>
<td>0.5</td>
</tr>
<tr>
<td>Either Output Rise Time Driving DMOS</td>
<td>( t_{RD} )</td>
<td>( C_L = IRFR120 )</td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>Either Output Fall Time Driving DMOS</td>
<td>( t_{FD} )</td>
<td>( C_L = IRFR120 )</td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td>Minimum Input Pulse Width that Changes the Output</td>
<td>( t_{PW} )</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Bootstrap Diode Turn-On or Turn-Off Time</td>
<td>( t_{BS} )</td>
<td>-</td>
<td>10</td>
<td>-</td>
</tr>
</tbody>
</table>

**Pin Descriptions**

<table>
<thead>
<tr>
<th>PIN NUMBER</th>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( V_{DD} )</td>
<td>Positive Supply to lower gate drivers. De-couple this pin to ( V_{SS} ) (Pin 7). Bootstrap diode connected to HB (pin 2).</td>
</tr>
<tr>
<td>2</td>
<td>HB</td>
<td>High-Side Bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.</td>
</tr>
<tr>
<td>3</td>
<td>HO</td>
<td>High-Side Output. Connect to gate of High-Side power MOSFET.</td>
</tr>
<tr>
<td>4</td>
<td>HS</td>
<td>High-Side Source connection. Connect to source of High-Side power MOSFET. Connect negative side of bootstrap capacitor to this pin.</td>
</tr>
<tr>
<td>5</td>
<td>HI</td>
<td>High-Side input.</td>
</tr>
<tr>
<td>6</td>
<td>LI</td>
<td>Low-Side input.</td>
</tr>
<tr>
<td>7</td>
<td>( V_{SS} )</td>
<td>Chip negative supply, generally will be ground.</td>
</tr>
<tr>
<td>8</td>
<td>LO</td>
<td>Low-Side Output. Connect to gate of Low-Side power MOSFET.</td>
</tr>
</tbody>
</table>

**Timing Diagrams**

FIGURE 3.

FIGURE 4.
Typical Performance Curves

**FIGURE 5.** OPERATING CURRENT vs FREQUENCY

**FIGURE 6.** LEVEL SHIFTER CURRENT vs FREQUENCY

**FIGURE 7.** HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

**FIGURE 8.** LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

**FIGURE 9.** UNDervoltage lockout THRESHOLD vs TEMPERATURE

**FIGURE 10.** UNDervoltage lockout HYSTERESIS vs TEMPERATURE
**Typical Performance Curves (Continued)**

- **FIGURE 11. PROPAGATION DELAYS vs TEMPERATURE**
- **FIGURE 12. PULLUP CURRENT vs OUTPUT VOLTAGE**
- **FIGURE 13. PULLDOWN CURRENT vs OUTPUT VOLTAGE**
- **FIGURE 14. BOOTSTRAP DIODE I-V CHARACTERISTICS**
- **FIGURE 15. BIAS CURRENT vs VOLTAGE**
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FAX: (65) 748-0400

HARRIS SEMICONDUCTOR
3A DUAL HIGH-SPEED MOSFET DRIVERS

**FEATURES**

- High Peak Output Current .................................. 3A
- Wide Operating Range .......................... 4.5V to 18V
- High Capacitive Load Drive Capability ........... 1800 pF in 25 nsec
- Short Delay Times ...................... <40 nsec Typ
- Matched Rise/Fall Times
- Low Supply Current
  - With Logic "1" Input .................. 3.5 mA
  - With Logic "0" Input .................. 350 µA
- Low Output Impedance ..................... 3.5Ω Typ
-Latch-Up Protected: Will Withstand 1.5A Reverse Current
-Logic Input Will Withstand Negative Swing Up to 5V
-ESD Protected ............................................. 4 kV
- Pinouts Same as TC1426/27/28; TC4426/27/28

**GENERAL DESCRIPTION**

The TC4423/4424/4425 are higher output current versions of the new TC4426/4427/4428 buffer/drivers, which, in turn, are improved versions of the earlier TC4426/4427/4428 series. All three families are pin-compatible. The TC4423/4424/4425 drivers are capable of giving reliable service in far more demanding electrical environments than their antecedents.

Although primarily intended for driving power MOSFETs, the TC4423/4424/4425 drivers are equally well-suited to driving any other load (capacitive, resistive, or inductive) which requires a low impedance driver capable of high peak currents and fast switching times. For example, heavily loaded clock lines, coaxial cables, or piezoelectric transducers can all be driven from the TC4423/4424/4425. The only known limitation on loading is the total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Package</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC4423COE</td>
<td>16-Pin SOIC (Wide)</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>TC4423CPA</td>
<td>8-Pin Plastic DIP</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>TC4423EOE</td>
<td>16-Pin SOIC (Wide)</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>TC4423EPA</td>
<td>8-Pin Plastic DIP</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>TC4424MJA</td>
<td>8-Pin CerDIP</td>
<td>−55°C to +125°C</td>
</tr>
<tr>
<td>TC4424COE</td>
<td>16-Pin SOIC (Wide)</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>TC4424CPA</td>
<td>8-Pin Plastic DIP</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>TC4424MJA</td>
<td>8-Pin CerDIP</td>
<td>−55°C to +125°C</td>
</tr>
</tbody>
</table>

**FUNCTIONAL BLOCK DIAGRAM**
**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage ......................................................... +22V
Input Voltage, IN A or IN B ...... V_{DD} + 0.3V to GND – 5.0V
Maximum Chip Temperature ......................... +150°C
Storage Temperature Range ...................... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ............. +300°C

Package Thermal Resistance
- CerDIP R_{θJA} ........................................... 150°C/W
- CerDIP R_{θJC} ........................................... 55°C/W
- PDIP R_{θJA} ............................................... 125°C/W
- PDIP R_{θJC} ................................................ 45°C/W
- SOIC R_{θJA} ............................................. 155°C/W

**SOIC R_{θJC} ................................................... 75°C/W**

Operating Temperature Range
- C Version ................................................. 0°C to +70°C
- I Version .............................................. -25°C to +85°C
- E Version .............................................. -40°C to +85°C
- M Version ............................................. -55°C to +125°C

Package Power Dissipation (T_{A} ≤ 70°C)
- Plastic DIP ................................................. 730mW
- CerDIP ..................................................... 800mW
- SOIC ........................................................... 470mW

**PIN CONFIGURATIONS**

**ELECTRICAL CHARACTERISTICS:** \( T_{A} = +25°C \) with \( 4.5V \leq V_{DD} \leq 18V \), unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>V_{OH} Logic 1 High Input Voltage</td>
<td></td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V_{IL} Logic 0 Low Input Voltage</td>
<td></td>
<td>—</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>I_{IN} Input Current</td>
<td>( 0V \leq V_{IN} \leq V_{DD} )</td>
<td>–1</td>
<td>1</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Output</td>
<td>V_{OH} High Output Voltage</td>
<td>( V_{DD} - 0.025 )</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V_{OL} Low Output Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>R_{O} Output Resistance, High</td>
<td>( I_{OUT} = 10 , mA, , V_{DD} = 18V )</td>
<td>—</td>
<td>2.8</td>
<td>5</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>R_{O} Output Resistance, Low</td>
<td>( I_{OUT} = 10 , mA, , V_{DD} = 18V )</td>
<td>—</td>
<td>3.5</td>
<td>5</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>I_{PK} Peak Output Current</td>
<td></td>
<td>—</td>
<td>3</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>I_{REV} Latch-Up Protection</td>
<td>Duty Cycle ≤ 2%</td>
<td>1.5</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Withstand Reverse Current</td>
<td>t ≤ 300 μs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Switching Time (Note 1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( t_{R} ) Rise Time</td>
<td>Figure 1, C_{L} = 1800 pF</td>
<td>—</td>
<td>23</td>
<td>35</td>
<td>nsec</td>
</tr>
<tr>
<td></td>
<td>( t_{F} ) Fall Time</td>
<td>Figure 1, C_{L} = 1800 pF</td>
<td>—</td>
<td>25</td>
<td>35</td>
<td>nsec</td>
</tr>
<tr>
<td></td>
<td>( t_{D1} ) Delay Time</td>
<td>Figure 1, C_{L} = 1800 pF</td>
<td>—</td>
<td>33</td>
<td>75</td>
<td>nsec</td>
</tr>
<tr>
<td></td>
<td>( t_{D2} ) Delay Time</td>
<td>Figure 1, C_{L} = 1800 pF</td>
<td>—</td>
<td>38</td>
<td>75</td>
<td>nsec</td>
</tr>
<tr>
<td>Power Supply</td>
<td>I_{S} Power Supply Current</td>
<td>( V_{IN} = 3V ) (Both Inputs)</td>
<td>—</td>
<td>1.5</td>
<td>2.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{IN} = 0V ) (Both Inputs)</td>
<td>—</td>
<td>0.15</td>
<td>0.25</td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTE:** Duplicate pins must both be connected for proper operation.
ELECTRICAL CHARACTERISTICS (Cont.)

Over operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Logic 1 High Input Voltage</td>
<td>$V_{DD} - 0.025$</td>
<td>—</td>
<td>—</td>
<td>$0.025$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic 0 Low Input Voltage</td>
<td>—</td>
<td>—</td>
<td>$0.8$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input Current</td>
<td>$0V \leq V_{IN} \leq V_{DD}$</td>
<td>$-10$</td>
<td>—</td>
<td>$10$</td>
<td>$\mu$A</td>
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</tbody>
</table>

Output

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>High Output Voltage</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Output Voltage</td>
<td>—</td>
<td>—</td>
<td>$0.025$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$R_O$</td>
<td>Output Resistance, High</td>
<td>$I_{OUT} = 10 mA$, $V_{DD} = 18V$</td>
<td>$3.7$</td>
<td>—</td>
<td>$8$</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$R_O$</td>
<td>Output Resistance, Low</td>
<td>$I_{OUT} = 10 mA$, $V_{DD} = 18V$</td>
<td>$4.3$</td>
<td>—</td>
<td>$8$</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$I_{PK}$</td>
<td>Peak Output Current</td>
<td>—</td>
<td>—</td>
<td>$3$</td>
<td>—</td>
<td>A</td>
</tr>
<tr>
<td>$I_{REV}$</td>
<td>Latch-Up Protection</td>
<td>Duty Cycle $\leq 2%$</td>
<td>—</td>
<td>$1.5$</td>
<td>—</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Withstand Reverse Current</td>
<td>$t \leq 300 \mu$s</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Switching Time (Note 1)

- $t_R$ | Rise Time | Figure 1, $C_L = 1800 \mu$F | — | $28$ | $60$ | nsec |
- $t_F$ | Fall Time | Figure 1, $C_L = 1800 \mu$F | — | $32$ | $60$ | nsec |
- $t_{D1}$ | Delay Time | Figure 1, $C_L = 1800 \mu$F | — | $32$ | $100$ | nsec |
- $t_{D2}$ | Delay Time | Figure 1, $C_L = 1800 \mu$F | — | $38$ | $100$ | nsec |

Power Supply

- $I_S$ | Power Supply Current | $V_{IN} = 3V$ (Both Inputs) | — | $2$ | $3.5$ | mA |
- $I_S$ | Power Supply Current | $V_{IN} = 0V$ (Both Inputs) | — | $0.2$ | $0.3$ | mA |

**NOTE:** 1. Switching times guaranteed by design.
TYPICAL CHARACTERISTICS

Rise Time vs Supply Voltage

Fall Time vs Supply Voltage

Rise Time vs Capacitive Load

Fall Time vs Capacitive Load

Rise and Fall Times vs Temperature

Propagation Delay vs Input Amplitude
TYPICAL CHARACTERISTICS (Cont.)

- **Propagation Delay Time vs Supply Voltage**
  - C LOAD = 2200 pF
  - \( t_{D2} \)

- **Delay Time vs Temperature**
  - C LOAD = 2200 pF

- **Quiescent Current vs Supply Voltage**
  - \( T_A = +25°C \)
  - BOTH INPUTS = 1
  - BOTH INPUTS = 0

- **Quiescent Current vs Temperature**
  - INPUTS = 1
  - INPUTS = 0

- **Output Resistance (Output High) vs Supply Voltage**
  - WORST CASE \( @ T_J = +150°C \)
  - TYP @ \( T_A = +25°C \)

- **Output Resistance (Output Low) vs Supply Voltage**
  - WORST CASE \( @ T_J = +150°C \)
  - TYP @ \( T_A = +25°C \)
SUPPLY CURRENT CHARACTERISTICS (Load on Single Output Only)

Supply Current vs Capacitive Load

Supply Current vs Frequency

Supply Current vs Capacitive Load

Supply Current vs Frequency

Supply Current vs Capacitive Load

Supply Current vs Frequency

Supply Current vs Capacitive Load

Supply Current vs Frequency
3A DUAL HIGH-SPEED MOSFET DRIVERS

**TC4423**
**TC4424**
**TC4425**

---

**TC4423 Crossover Energy**

![Graph showing crossover energy vs. input voltage (Vin)](image)

**NOTE:** The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

---

**Thermal Derating Curves**

![Graph showing power vs. ambient temperature](image)

---

**Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings (See page 2) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.**

---

**PACKAGE DIMENSIONS**

**8-Pin Plastic DIP**

![Diagram of 8-pin plastic DIP package dimensions](image)

- **PIN 1**
- **.260 (6.60)**
- **.240 (6.10)**
- **.045 (1.14)**
- **.030 (0.76)**
- **.070 (1.78)**
- **.045 (1.14)**
- **.400 (10.16)**
- **.348 (8.84)**
- **.200 (5.08)**
- **.140 (3.56)**
- **.150 (3.81)**
- **.115 (2.92)**
- **.040 (1.02)**
- **.020 (0.51)**
- **.015 (0.38)**
- **.090 (2.29)**
- **.022 (0.56)**
- **.015 (0.38)**
- **.015 (0.38)**
- **.008 (0.20)**
- **.400 (10.16)**
- **.310 (7.87)**

**Dimensions: inches (mm)**
8-Pin CerDIP

16-Pin Plastic SOIC (Wide)

Dimensions: inches (mm)
DATA SHEET

E22/6/16
Planar E cores

Product specification
File under Magnetic Products, MA01

1997 Nov 21
Planar E cores

**CORES**

Effective core parameters of a set of E cores

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
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</thead>
<tbody>
<tr>
<td>$\Sigma(I/A)$</td>
<td>core factor (C1)</td>
<td>0.414</td>
<td>mm$^{-1}$</td>
</tr>
<tr>
<td>$V_e$</td>
<td>effective volume</td>
<td>2550</td>
<td>mm$^3$</td>
</tr>
<tr>
<td>$l_e$</td>
<td>effective length</td>
<td>32.5</td>
<td>mm</td>
</tr>
<tr>
<td>$A_e$</td>
<td>effective area</td>
<td>78.5</td>
<td>mm$^2$</td>
</tr>
<tr>
<td>$A_{\text{min}}$</td>
<td>minimum area</td>
<td>78.5</td>
<td>mm$^2$</td>
</tr>
<tr>
<td>$m$</td>
<td>mass of core half</td>
<td>$\approx$ 6.5</td>
<td>g</td>
</tr>
</tbody>
</table>

Effective core parameters of an E/PLT combination

<table>
<thead>
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<th>SYMBOL</th>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
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<td>$\Sigma(I/A)$</td>
<td>core factor (C1)</td>
<td>0.332</td>
<td>mm$^{-1}$</td>
</tr>
<tr>
<td>$V_e$</td>
<td>effective volume</td>
<td>2040</td>
<td>mm$^3$</td>
</tr>
<tr>
<td>$l_e$</td>
<td>effective length</td>
<td>26.1</td>
<td>mm</td>
</tr>
<tr>
<td>$A_e$</td>
<td>effective area</td>
<td>78.5</td>
<td>mm$^2$</td>
</tr>
<tr>
<td>$A_{\text{min}}$</td>
<td>minimum area</td>
<td>78.5</td>
<td>mm$^2$</td>
</tr>
<tr>
<td>$m$</td>
<td>mass of plate</td>
<td>$\approx$ 4</td>
<td>g</td>
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Ordering information for plates

<table>
<thead>
<tr>
<th>GRADE</th>
<th>TYPE NUMBER</th>
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<tbody>
<tr>
<td>3F3</td>
<td>PLT22/16/2.5-3F3</td>
</tr>
<tr>
<td>3F4</td>
<td>PLT22/16/2.5-3F4</td>
</tr>
<tr>
<td>3E6</td>
<td>PLT22/16/2.5-3E6</td>
</tr>
</tbody>
</table>

Fig. 1 E22/6/16.

Dimensions in mm.

Fig. 2 PLT22/16/2.5.

Dimensions in mm.
## Planar E cores

**Core halves for use in combination with an non-gapped E core**

$A_L$ measured in combination with a non-gapped core half, clamping force 20 ±10 N, using a PCB coil containing 5 layers of 20 tracks each, total height 2.5 mm, E + PLT is measured with a single PCB coil, E + E with two PCB coils stacked.

<table>
<thead>
<tr>
<th>GRADE</th>
<th>$A_L$ (nH)</th>
<th>$\mu_e$</th>
<th>AIR GAP ($\mu$m)</th>
<th>TYPE NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>3F3</td>
<td>160 ±3%</td>
<td>53</td>
<td>900</td>
<td>E22/6-3F3-A160-E</td>
</tr>
<tr>
<td></td>
<td>250 ±3%</td>
<td>82</td>
<td>490</td>
<td>E22/6-3F3-A250-E</td>
</tr>
<tr>
<td></td>
<td>315 ±3%</td>
<td>104</td>
<td>360</td>
<td>E22/6-3F3-A315-E</td>
</tr>
<tr>
<td></td>
<td>400 ±5%</td>
<td>132</td>
<td>280</td>
<td>E22/6-3F3-A400-E</td>
</tr>
<tr>
<td></td>
<td>630 ±8%</td>
<td>208</td>
<td>160</td>
<td>E22/6-3F3-A630-E</td>
</tr>
<tr>
<td></td>
<td>4300 ±25%</td>
<td>1420</td>
<td>0</td>
<td>E22/6/16-3F3</td>
</tr>
<tr>
<td>3F4</td>
<td>160 ±3%</td>
<td>53</td>
<td>900</td>
<td>E22/6-3F4-A160-E</td>
</tr>
<tr>
<td></td>
<td>250 ±3%</td>
<td>82</td>
<td>490</td>
<td>E22/6-3F4-A250-E</td>
</tr>
<tr>
<td></td>
<td>315 ±3%</td>
<td>104</td>
<td>360</td>
<td>E22/6-3F4-A315-E</td>
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<tr>
<td></td>
<td>400 ±5%</td>
<td>132</td>
<td>280</td>
<td>E22/6-3F4-A400-E</td>
</tr>
<tr>
<td></td>
<td>630 ±8%</td>
<td>208</td>
<td>160</td>
<td>E22/6-3F4-A630-E</td>
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<tr>
<td></td>
<td>2400 ±25%</td>
<td>790</td>
<td>0</td>
<td>E22/6/16-3F4</td>
</tr>
<tr>
<td>3E6</td>
<td>22000 ±40/-30%</td>
<td>7250</td>
<td>0</td>
<td>E22/6/16-3E6</td>
</tr>
</tbody>
</table>

**Core halves for use in combination with a plate (PLT)**

$A_L$ measured in combination with a plate (PLT), clamping force 20 ±10 N, using a PCB coil containing 5 layers of 20 tracks each, total height 2.5 mm, E + PLT is measured with a single PCB coil, E + E with two PCB coils stacked.

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<th>$\mu_e$</th>
<th>AIR GAP ($\mu$m)</th>
<th>TYPE NUMBER</th>
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</thead>
<tbody>
<tr>
<td>3F3</td>
<td>160 ±3%</td>
<td>42</td>
<td>950</td>
<td>E22/6-3F3-A160-P</td>
</tr>
<tr>
<td></td>
<td>250 ±3%</td>
<td>66</td>
<td>550</td>
<td>E22/6-3F3-A250-P</td>
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<tr>
<td></td>
<td>315 ±3%</td>
<td>83</td>
<td>400</td>
<td>E22/6-3F3-A315-P</td>
</tr>
<tr>
<td></td>
<td>400 ±5%</td>
<td>106</td>
<td>280</td>
<td>E22/6-3F3-A400-P</td>
</tr>
<tr>
<td></td>
<td>630 ±8%</td>
<td>166</td>
<td>160</td>
<td>E22/6-3F3-A630-P</td>
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<tr>
<td></td>
<td>5000 ±25%</td>
<td>1320</td>
<td>0</td>
<td>E22/6/16-3F3</td>
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<tr>
<td>3F4</td>
<td>160 ±3%</td>
<td>42</td>
<td>950</td>
<td>E22/6-3F4-A160-P</td>
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<tr>
<td></td>
<td>250 ±3%</td>
<td>66</td>
<td>550</td>
<td>E22/6-3F4-A250-P</td>
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<tr>
<td></td>
<td>315 ±3%</td>
<td>83</td>
<td>400</td>
<td>E22/6-3F4-A315-P</td>
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<tr>
<td></td>
<td>400 ±5%</td>
<td>106</td>
<td>280</td>
<td>E22/6-3F4-A400-P</td>
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<tr>
<td></td>
<td>630 ±8%</td>
<td>166</td>
<td>160</td>
<td>E22/6-3F4-A630-P</td>
</tr>
<tr>
<td></td>
<td>2900 ±25%</td>
<td>770</td>
<td>0</td>
<td>E22/6/16-3F4</td>
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<tr>
<td>3E6</td>
<td>26000 ±40/-30%</td>
<td>6900</td>
<td>0</td>
<td>E22/6/16-3E6</td>
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DEFINITIONS

Data sheet status

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<td>This data sheet contains target or goal specifications for product development.</td>
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<tr>
<td>Preliminary specification</td>
<td></td>
<td>This data sheet contains preliminary data; supplementary data may be published later.</td>
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<tr>
<td>Product specification</td>
<td></td>
<td>This data sheet contains final product specifications.</td>
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</table>

Application information

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<th>INDICATION</th>
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<td>These are products that have been made as development samples for the purposes of technical evaluation only. The data for these types is provisional and is subject to change.</td>
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<tr>
<td>Design-in</td>
<td></td>
<td>These products are recommended for new designs.</td>
</tr>
<tr>
<td>Preferred</td>
<td></td>
<td>These products are recommended for use in current designs and are available via our sales channels.</td>
</tr>
<tr>
<td>Support</td>
<td></td>
<td>These products are <strong>not</strong> recommended for new designs and may not be available through all of our sales channels. Customers are advised to check for availability.</td>
</tr>
</tbody>
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Printed in The Netherlands
3F3
Material grade specification

File under Magnetic Products, MA01

1997 Nov 21
Material grade specification

3F3 SPECIFICATIONS

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<th>SYMBOL</th>
<th>CONDITIONS</th>
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<th>UNIT</th>
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<td>$\mu_i$</td>
<td>$25 , ^\circ C; \leq 10 , kHz; \leq 0.1 , mT$</td>
<td>$1800 \pm 20%$</td>
<td></td>
</tr>
<tr>
<td>$\mu_a$</td>
<td>$100 , ^\circ C; 25 , kHz; 200 , mT$</td>
<td>$\approx 4000$</td>
<td></td>
</tr>
<tr>
<td>$B$</td>
<td>$25 , ^\circ C; 10 , kHz; 250 , A/m$</td>
<td>$\geq 400$</td>
<td>mT</td>
</tr>
<tr>
<td></td>
<td>$100 , ^\circ C; 10 , kHz; 250 , A/m$</td>
<td>$\geq 330$</td>
<td>mT</td>
</tr>
<tr>
<td>$P_V$</td>
<td>$100 , ^\circ C; 100 , kHz; 100 , mT$</td>
<td>$\leq 80$</td>
<td>kW/m$^3$</td>
</tr>
<tr>
<td></td>
<td>$100 , ^\circ C; 400 , kHz; 50 , mT$</td>
<td>$\leq 150$</td>
<td>kW/m$^3$</td>
</tr>
<tr>
<td>$\rho$</td>
<td>DC; $25 , ^\circ C$</td>
<td>$\approx 2$</td>
<td>$\Omega m$</td>
</tr>
<tr>
<td>$T_C$</td>
<td></td>
<td>$\geq 200$</td>
<td>$^\circ C$</td>
</tr>
<tr>
<td>density</td>
<td></td>
<td>$\approx 4750$</td>
<td>kg/m$^3$</td>
</tr>
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</table>

Fig. 1 Complex permeability as a function of frequency.

Fig. 2 Initial permeability as a function of temperature.

Fig. 3 Typical B-H loops.
Material grade specification 3F3

Fig. 4 Amplitude permeability as function of peak flux density.

Fig. 5 Incremental permeability as a function of magnetic field strength.

Fig. 6 Specific power loss as a function of peak flux density with frequency as a parameter.

Fig. 7 Specific power loss for several frequency/flux density combinations as a function of temperature.
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Appendix B

Computer Aided Design (CAD)
Drawing of Power Stage
Appendix C

Computer Aided Design (CAD)
Drawing of Control Module
Top Layer Metallization

First Via Layer
2nd Layer Metallization

2nd Via Layer
3rd Layer Metallization

3rd Via Layer
C6  Electronic Packaging Strategies for High Current DC to DC Converters
Fred D. Barlow III
Fred D. Barlow III

Fred Barlow earned a Bachelors of Science in Physics and Applied Physics from Emory University in 1990, and a Masters of Science in Electrical Engineering from Virginia Tech in 1994. He has worked as a Senior Research Associate in the Electrical Engineering Department at Virginia Tech, while pursuing this Ph.D. Degree in Electrical Engineering.

He has published widely on Electronic Packaging and Electronic Materials Evaluation. He is coeditor of The Handbook of Thin Film Technology (McGraw Hill, 1998) and has written several book chapters including two chapters on thin films and one on components and devices. He has been awarded several educational grants during the course of his study. He also has achieved the Outstanding Contribution Award with IMAPS society in recognition of his efforts in developing and implementing the CD-ROM project for IMAPS publications, IMAPS Home Page on the Internet, and for his technical contributions. He currently serves on the IMAPS technical committee for power packaging.

Fred Barlow will be joining the University of Arkansas, HIDE Center, as a Research Assistant Professor, effective Fall 1999.
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