Model Development, Synthesis and Validation Using the Modeler’s Assistant

by

Soumya Narnur

Thesis submitted to the Faculty of
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements of the degree of

Master of Science
In
Electrical Engineering

APPROVED:

James R. Armstrong, Chairman

F.Gail Gray

Dong S. Ha

August, 1999
Blacksburg, Virginia
Model Development, Synthesis and Validation Using the Modeler’s Assistant

By

Soumya Narnur

Dr. James R. Armstrong, Chairman

Electrical and Computer Engineering

(ABSTRACT)

This thesis discusses ‘Modeler’s Assistant’, an interactive graphics tool which aids in the rapid development of VHDL models. The tool provides modeling, test bench generation, simulation, synthesis and validation features. The ‘Process Model graph’ which has representations for the concurrent processes is used as the basis on which the Modeler’s Assistant is built. Test generation environment is integrated into the tool. A range of test bench options are provided to the user. The tool interfaces to ‘Synopsys’ VHDL analyzer, graphics debugger and synthesis tools. Validation of the behavioral model versus the synthesized structural model is also discussed. A detailed programming manual with many examples is provided for the benefit of the user.
To Amma, Anna and Soujanya
Acknowledgements

I thank my advisor, Dr. James Armstrong for all his support, encouragement and guidance. It was a memorable experience working with him for nearly 2 years.

I thank Dr. Dong Ha for all his suggestions and helping me. I am grateful to Dr.Gray for serving on my committee and for his support.

I thank God for all his blessings. I thank my parents, Sri.Gopinatha Rao and Smt.Vidyullatha without whose support I wouldn’t have come here and studied in this wonderful University. I thank my sister, Soujanya for being such a wonderful sister.

I thank Mr.Farooq Azam, System administrator, Workstation Lab and Mr.Libo,System Administrator, VISC Labs for their continued support

I would like to thank my friend, Ravi Bulusu for all the help he rendered without which it would have been difficult in the initial stages. I thank Ramprasad for being such good brother.

And finally all my friends who made my stay at Virginia Tech a memorable one.
TABLE OF CONTENTS

Chapter 1
Introduction

1.1 Motivation ................................................................. 1
1.2 Overview................................................................. 2
1.3 Basic Approach To Modeling...................................... 4

Chapter 2
Previous Limitations and Enhancements

2.1 Previous Work............................................................ 8
2.2 Current Version of Modeler’s Assistant........................ 10
2.3 Implementation Details .............................................. 13

Chapter 3
Packages

3.1 Packages Overview .................................................. 15
Chapter 4

Test Bench Creation

4.1 Various Test Benches ................................................................................. 20

Shell ............................................................................................................. 20

Combinational Input Generator ................................................................. 22

CG + OSC ................................................................................................... 23

File IO ......................................................................................................... 24

File IO + OSC ............................................................................................ 26

Validation ................................................................................................. 26

Syncad ........................................................................................................ 29

4.2 Analysis ................................................................................................. 29

4.3 Simulation and Synthesis ..................................................................... 31

Chapter 5

Programming Manual

5.1 Development Process ..........................................................................33

Chapter 6

Future Work .............................................................................................. 67
Bibliography .................................................................................................................69

Appendix A
For Users .....................................................................................................................71

Appendix B
Future Developers ......................................................................................................73

Appendix C
File Description .........................................................................................................76

Vita .............................................................................................................................80
LIST OF FIGURES

Figure 1.1 A PMG ........................................... 3
Figure 1.2 The PMG with vector signals ........................................... 6
Figure 2.1 Block Diagram of Modeler’s Assistant ........................................... 14
Figure 3.1 The Package Menu in Modeler’s Assistant ........................................... 17
Figure 3.2 Showing the Definition and Declaration of a Package ........................................... 18
Figure 4.1 Showing the simple ‘Shell’ Test Bench ........................................... 20
Figure 4.2 Showing the ‘CG’ Test Bench Block Diagram ........................................... 22
Figure 4.3 Showing the ‘CG +OSC’ Block Diagram ........................................... 23
Figure 4.4 Showing the ‘FileIO’ Test Bench ........................................... 24
Figure 4.5 Showing the ‘Validation’ Test Bench ........................................... 27
Figure 4.6 The ‘Analyzer’ Window ........................................... 31
Figure 4.7 Showing the ‘Design Analyzer Script’ File ........................................... 32
Figure 5.1 The ‘Process’ Menu ........................................... 34
Figure 5.2 The ‘Specify’ Window ........................................... 37
Figure 5.3 The ‘Unit’ Menu ........................................... 39
Figure 5.4 The ‘Add’ Menu ........................................... 40
Figure 5.5 The ‘Shell’ Test Bench ........................................... 43
Figure 5.6a The ‘CG+OSC’ Test Bench ........................................... 47
Figure 5.6b  Continuation of ‘CG+OSC’ Test Bench  .......................48

Figure 5.7a  The Test Bench with ‘Wait’ Statements  .......................52

Figure 5.7b  Continuation of Test Bench with ‘Wait’ Statements  ........... 53

Figure 5.8a  The Test Bench with ‘Transport’ Statements  .......................54

Figure 5.8b  Continuation of the Test Bench with ‘Transport’ Statements  .......................55

Figure 5.9a  The ‘Validation’ Test Bench  .......................60

Figure 5.9b  Continuation of ‘Validation’ Test Bench  .......................61

Figure 5.10  The ‘Synthesis’ Window  .......................64

Figure 6.1  The Linked List Structure  .......................74

Figure 6.2  Various Parameters  .......................75