Chapter 5. Future applications of the Dimple Array interconnect

5.1 Discrete power package
Discrete power packages are usually medium- to low-power packages that are mounted in a circuit using the through-hole or the surface-mounting techniques. The conventional wire bond package is single-side cooled and normally requires heat sinking, which needs extra PCB space. In addition, current handling capability is highly limited when wire bonds are used.

5.1.1 Conceptual CAD design
Figure 5.1 (a) shows an artistic view of a TO-247 DAI package, in comparison with a conventional wire bond package (b). For the wire bond TO-247 package, the aluminum wire bond is vulnerable and must be protected using glob-top molding. Note that in order to show the inside of the wire bond package, the top molding compound is hidden. For the DAI TO-247 package, the gap between the dimple interconnect and the silicon device is underfilled, and there is no need to build a top-molding compound because the top of the dimple interconnect does not need to be isolated from the environment.

In the Dimple Array technique, improvement in current handling capability is achieved due to the use of shorter, thicker solder joints instead of wire bonds.

![Figure 5.1](image)

Figure 5.1 (a) Artistic view of the Dimple Array TO-247 discrete MOSFET package; and (b) the wire bond TO-247 discrete MOSFET package, top molding not shown.
5.1.2 Fabrication of the DAI TO-247 package

A fabrication flowchart of the DAI TO-247 MOSFET package is shown in Figure 5.2. The MOSFET device is first solder-attached to the standard copper base metal. The backside of the device is the drain electrode, which connects to the center lead. Next, solder paste is screen-printed onto the solderable device pads. Solder preforms can also be used. The pre-stamped dimple interconnect flex (with polymer coating on top) is then aligned with the solder pads. The assembly is reflowed to form the dimple solder joints. CTE-matched, high-flow epoxy can be used to fill the gap between the dimple flex and the device for enhanced reliability. Last, the assembly is encapsulated with a conventional molding compound.

Figure 5.2 Fabrication flowchart for the DAI TO-247 MOSFET.

5.1.3 Thermal modeling and discussion

The thermal performance of a DAI TO-247 package is compared with the wire bond package TO-247 using FEA modeling. The packages are mounted on a heat spreader by bolting through the hole in the package. For both packages, heat is exchanged with the environment through the following two paths: by the conduction from bottom heat spreader and by the convection from the tops of the packages. For the wire bonding package, however, the heat dissipation from the top is very limited due to the large
thermal resistance of the molding compound needed for protection of the wires. For the DAI package, the planar dimple copper flex (source) is more robust and does not need molding protection. The flex serves as a good heat path that exchanges heat with the environment through convection. Obviously, using the DAI substantially improves the heat-dissipation capability because double-sided cooling is enabled. Either forced-air cooling or heat sinking can be used to cool the topside of the DAI.

Figure 5.3 show plots of the temperature distributions obtained by FEM; the temperature is displayed on several planes sliced through the packages.

Figure 5.3  Thermal performance of TO-247 power packages: wire bond (a) and DAI (b) (Graphs courtesy of Dr. Tao Lin, Math Dept. at Virginia Tech).
For easy observation of the difference, the scale in these plots is windowed around the highest temperature of the wire bond package. These plots show that the overall temperature of the DAI package is obviously lower than that of the wind bond package (lighter color represents hotter regions). In particular, a reduction of junction temperature in the silicon of the DAI package is observed, due to its double-sided cooling.

5.2 Packaging of FTO

The double-sided IGBT, or Fast Turn-Off (FTO) IGBT device, has been proposed to break through the major limitation; i.e., the IGBT $V_F-E_{off}$ trade-off. FTO is a symmetric, double-gated IGBT structure (Figure 5.4). Capable of directing current or blocking voltage in both directions, the FTO also has very low switching loss. These advantages might make it possible to build much-simplified power electronics modules, such as inverters, with close to ideal switching characteristics.

![Figure 5.4 FTO device structure.](Image)

5.2.1 Available packaging schemes

Packaging ultimately determines the final performance of the FTO. The double-sided IGBT sets a challenge, however, for existing packaging solutions. Available packaging
approaches (the wire bonding, the press pack, the deposited metallization, and the solder area array bumping), all require that at least one side of the devices be dedicated to heat dissipation. The symmetric structure of FTO features gate connections on both sides of the devices. The device fabrication group in the Naval Research Laboratory (NRL) requires at least 5 mil clearance between the device surface and the contact metals on each side. Modification of existing packaging techniques might lead to feasible packaging approaches with increased structure complexity. Figure 5.5 depicts schemes of packaging the FTO using some of these available packaging techniques.

Figure 5.5 Various approaches for FTO packaging: (a) ThinPak; (b) press pack; (c) wire bond; and (d) solder area array.

5.2.2 Processing

Although many approaches are available for packaging the FTO, only the area array solder bumping approach is discussed in this report. Area array solder bumping has straightforward structure and simple processing. Figure 5.6 shows the processing flowchart for area array solder bumping for packaging FTO:
Figure 5.6 FTO packaging process using dimple area array bumping.

As shown in Figure 5.6, DBC substrate has been used as the substrate material. The DBC has etched patterns that allow the gate and the collector electrode to be connected. Solder bumps offer a liftoff of the device from the substrate surface. The solder ball-limiting regions are defined by applying a solder mask. The bottom bumps, which are high-melting-temperature solder (Pb90-Sn10), are first formed on DBC through a reflow process. Then, eutectic tin-lead solder paste is dispensed on the collector side of the device. The devices are picked up and aligned with the solder bumps on the DBC and placed on top of them. The second reflow bonds the device to the DBC with the help of self-alignment of the solder bumps. Underfill dispensing is employed to fill in the gap between the chip and the DBC for a robust mechanical support. The underfill needs to be cured at 120°C for 20 minutes before the next steps. Then, solder is dispensed over the FTO emitter pads, and the stamped dimple interconnect is pick-and-placed to align with the device. A final reflow completes the joining process. Again, underfill is dispensed into the gap between the dimple interconnect and the device, and this is followed by another curing process.
5.2.3 Thermal considerations for FTO packaging

Transient and steady-state thermal characteristics of the FTO packaged by area array solder bumping are evaluated using CFD software I-DEAS Electronics System Cooling (ESC). The prototype single-chip module is shown in Figure 5.7 (a), and the simulation model is shown in Figure 5.7 (b). A series of transient power pulses were applied to the models. A comparison of the simulated transient thermal impedances of a wire bond module and the FTO module is shown in Figure 5.8.

![Prototype FTO package (a) and simulation model (b).](image1)

**Figure 5.7** Prototype FTO package (a) and simulation model (b).

![Transient thermal impedance for wire bond model (a) and Dimple Array bumping FTO model (b).](image2)

**Figure 5.8** Transient thermal impedance for wire bond model (a) and Dimple Array bumping FTO model (b).

For the wire bond module, the transient stage no longer exists when pulse width exceeds 0.1 second. The steady-state thermal impedance reaches 0.047K/W. For FTO module, the impedance is not stabilized until the single power pulse width is longer than three
seconds. Its steady-state resistance is 36 times larger than that of the wire bond. This result shows that, due to the symmetrical interconnection of the FTO device, and thus no large-area die-attach is incorporated in the FTO package, the resulting transient thermal impedance characteristics are intolerably compromised.

Modifications, both in device electrode layout design and packaging scheme of the FTO, are necessary to meet the goals specified by the system’s thermal requirement. An increase in the electrode area, which enables the utilization of greater device area and the bumping of reduced-standoff-height solder bumps, can dramatically improve the thermal characteristics. Since current underfill materials do not help in thermal dissipation, seeking a different underfill with higher-thermal-conductivity filler is another option.

The thermal performance of the FTO can also be improved using SPCO ThinPak or press pack techniques. However, the reliability of large-area soldering of the device to a ceramic lid poses a concern for the ThinPak structure. The press pack approach, as conceptualized in Figure 5.5, can improve both the thermal performance and the reliability of the FTO, although this is a more expensive approach and needs additional insulation and cooling.

The Dimple Array solder bumping technique at least provides a fast and economical way to package FTO devices for reliable electrical testing.