Switchmode Power Supply Miniaturization with Emphasis on Integrated Passive Components on Prefired High Performance Ceramic Substrates

by

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ABSTRACT

This Dissertation is a study of Switched Mode Power Supply (SMPS) miniaturization and how to effectively use the available technologies to achieve the ultimate goal of a reduced size without loss of functionality while maintaining a cost effective design. This research investigates several methods used to obtain low loss, highly compact power supplies. Within these constraints, the Dissertation investigates the issues of design, materials, and cost in order to design and achieve these miniaturized power supplies.

This research addresses high performance ceramic, passive component integration. Three key issues; electrical characterization, thermal analysis and simulation, and material characterization, are examined in this work. Thick film passive components (capacitors and resistors) on AlN have been developed. Also, guidelines for the design implementation and steps necessary to integrate these passive components on prefired alumina (Al₂O₃) and aluminum nitride (AlN) ceramic surfaces, for power electronic applications, have been generated. The use of aluminum nitride, as a high performance ceramic substrate and the resulting issues concerning compatible inks, have been investigated. Since a sizable amount of heat is generated by power electronic circuits, the integrated components are analyzed with respect to tolerance and degeneration over a range of temperatures and frequencies. Thick film capacitors on the order of 120pF/mm² with breakdown voltage ratings of 250V have been developed on prefired AlN.
Resistors were developed with impedances ranging from 10Ω to 10MegΩ. Thermal measurements, of these resistors, show that the thermal conductivity of the aluminum nitride with passivation layer is two to three times that of alumina.

Several versions of a typical SMPS boost circuit have been generated using Direct Bond Copper (DBC) on ceramic, Insulated Metal Substrate (IMS), Printed Circuit Boards (PCB), and prefired ceramic thick film technology. The integrated passive components developed are applied on prefired ceramic versions and compared to the DBC, IMS and PCB versions.

A small daughter board consisting of the boost circuit control is introduced to further supplement miniaturization and reduce cost. The daughter board uses thick film technology with integrated thick film resistors. The design of the mother board, which houses the power boost section, can be designed and implemented on virtually any type of substrate (PCB, DBC, IMS, or conventional thick film). The fabrication and testing of each version is reported in this work.
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1. Introduction

The industrial revolution started an explosion in rapid development of goods that helped saturate the market with quality, low cost manufactured goods. Currently, the industry is experiencing the infancy stage of an electronics revolution. The same revolutionary concept applies. The engineers are in the midst of rapid development of electronics that are saturating the market with quality, low cost devices. They are just getting a taste of what electronics miniaturization can do to ease the our everyday burdens and make everyone's lives more enjoyable to live. Everyone's future holds the exciting prospects of complete interpersonal connectivity, direct interface computational ability, and fully automated electromechanical manufacturing and transportation.

The electronics revolution is bringing about changes daily. New and different ideas are constantly being conjured up in order to advance the technology to a new level of integration. It is up to the engineers to sift through this vast amount of information and determine which innovation is applicable to a current situation. Now, while the technologies that have the widest appeal get the most attention, there are hundreds of advancements that are short lived but provide valuable stepping stones to the next level. There are others that just broaden the knowledge and provide one a better understanding of science in general.

Thirty years into the electronics revolution leaves the electrical engineer sitting at the edge of a large sea of information. Through the exchange and interchange of information, common interests and objectives can be rapidly explored. It is the diversity and complexity of this information that forces each electrical engineer into a specialty. While electrical engineers may not
have the fancy specialty names, such designations are very important in order to fix, cure or find a solution to a problem.

Faster, lighter, and smaller, today's push in electronics, require a team of specialists to achieve the objectives set. Design, layout, packaging, RF, analog, digital, and mixed mode are just a handful of specialties on a design team. IC designers have been getting most of the notoriety due to the doubling of processor power every eighteen months as predicted by Moore's law. It is the new methods of gate width reduction that keep Moore's law from becoming obsolete. Just as it seems that further reduction cannot be achieved, a new technology emerges to pick up where the old one left off. Hard drive magnetic technology has had the same frantic pace, more and more in less and less space.

So with all this integration and processing technology, why is it that cell phones are not the size of a hearing aide? There is still a large lag in technology. In order to keep the costs down, integrated circuits must be surrounded by a host of support components (such as resistors, capacitors, and inductors) to make them flexible enough to be used in multiple applications. It was always expected that as more and more functionality was incorporated into a piece of silicon that the need for passive components would diminish. This has not been the case. As a result, the electronics industry has now hit a bottle neck. To cure this problem, a new specialist has been created, the Integral Substrate (IS) specialist and the Integrated Passive Component (IPC) specialist. These specialists search for new ways to reduce the area and cost required of passive components.

The impetus behind ISs and IPCs is circuit miniaturization. Reliability and cost reduction are important secondary considerations. For the same reasons, the through hole passive
components started to give way to surface mount components in the mid 1980s. Therefore, it is not a matter of whether IPCs will be eventually implemented, it is one of how and when.

At this current time, there are several competing technologies. The two main categories are Integral Substrates and Integrated Passive Components. IPCs combine many of the same type of passives and incorporate them into a single package. For example, five resistors into one SOIC type package. On the other hand, ISs are integrated into the substrate, either on top or within the inner layers of a substrate, or onto the top of the bare die itself. Examples of this type would be printed thick film resistors and capacitors or, thin film deposited resistors onto a silicon chip.

If integrating passives were easy and straight forward, it would already have been achieved at this time. Several issues must be resolved in order to advance this technology. The first hurdle is the technological knowledge needed to integrate components. Materials and processes must be investigated. CAD tools must be developed that can accurately model the new components. And most importantly, the present status quo must be challenged in order to get manufacturers to change from surface mount components over to integrated components.

For ISs and IPCs to succeed, they must be as convenient to use, cheaper, and at least as reliable as present SMT components. It is convenient to replace a SMT component with another during the manufacturing of a device if it is determined that it has drifted or fails to meet specifications. Using SMT components, it is relatively simple to develop a single circuit to perform multiple functions by simply changing out a few passives. For instance, making a radio receiver for both US and European markets. Simple adjustments of the LC tank circuit elements can adjust for the frequency standard differences.

The problem with integrated passives is that values are fixed and, depending on the technology, large tolerances may exist if the components are buried within the inner layers of a

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substrate. While surface layer thick film resistors can be laser trimmed to tolerances of 0.5%, buried components may vary by as much as 50% or more. Power dissipation may also be a problem for buried components. The function of a resistor is to change electrical energy into thermal energy. If the heat is not properly removed, this will adversely affect the stability of the resistor and other components in close proximity.

It is the intent of this research work to investigate one possible solution to Switched Mode Power Supply (SMPS) circuit miniaturization through the development of integrated passives for high performance ceramic substrates. Thermal management, interconnects reliability, low volume, light weight, and electrical ratings plague the designer. Thick film circuit technology can address these issues, if properly applied, and provide an attractive alternative to printed circuit board methods in the realization of power electronics circuitry.

The introduction of AlN as a thick film substrate has opened the door for cost effective and environmentally responsible circuit construction. AlN offers seven times the thermal conductivity of Al₂O₃ and does not have the toxic properties of Beryllium Oxide (BeO). Also, AlN based circuits can be processed using the same equipment used for Al₂O₃ circuit production; thus, additional capital investment is not necessary. Since this material is fairly new in the use as a thick film substrate material, there is a great need for research in this area in order to expose this technology's strengths and weaknesses.

This Dissertation is organized into ten chapters. Chapter 1, this chapter is a general introduction. Chapter 2 presents a background and a literature review with regard to integral passives and switch mode power supply miniaturization. Chapter 3 details the processes and characteristics of integral thick film capacitors that were developed as part of this Dissertation work. Chapter 4 covers the characterization of thick film resistors on aluminum nitride with

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passivation layer. Also covered is the thermal characterization of the aluminum nitride and the effects of the passivation in respect to thermal degradation. Chapter 5 covers the electrostatic discharge measurements that were conducted on the thick film resistors and capacitors. Chapter 6 covers the characterization of a thick film ferrite paste using spiral inductor measurements. The chapter also covers the mathematical calculations for a multilayer thick film planar transformer with attached ferrite core. Chapter 7 covers the basics of switched mode power supply miniaturization. The issues of high voltage and high current are covered. Chapter 8 discusses the miniaturization efforts of a boost circuit switched mode power supply. In this chapter, printed circuit board, direct bond copper, and surface mount technologies are investigated. Chapter 9 details the switched mode power supply miniaturization efforts with regard to integral thick film passive components. Finally, Chapter 10 gives conclusions and future directions in regard to the conducted research.
2. Background and Literature Review

Miniaturization of electronic systems has been a daunting task that started in the late fifties with the development of integrated circuits. While miniaturization of integrated transistors and in turn processing power has progressed at a steady rate according to Moore’s law, the electronics packaging industry has been cursing the expediency at which ICs have gained ground over the miniaturization of the interconnects and support components necessary to connect these chips.

ICs keep gaining ground since they are finding a way to use the same amount of material to produce more functionality. Passive component miniaturization has lagged far behind for several reasons. Passive circuitry (interconnect and support components) is still struggling to find a medium in which all the components can be integrated. Once total integration is successfully achieved, successive generations on miniaturization can evolve as it has in the silicon sector. Only then will miniaturization become a function of physics of reduction rather than the issues of integration. At that point, CAD tools and accurate device models will become of utmost importance.

What is the ultimate medium for interconnect and passive components integration? The answer is none. While scientists continue on the quest for the ultimate medium, several technologies hold promise. The big battle is between semiconductor, ceramic, and polymers. Cost, cost, and cost keep circuit designs from imploding into an ultra miniature form. Therefore, once again let’s look to the silicon sector. A circuit design starts out with a design with an IC or a set of ICs and a host of support components. If this design is common to several other similar designs or is going to be manufactured in quantities of 100,000 or more, then as most of the support components and individual ICs are incorporated into one IC. Thus, a small expensive piece of
silicon can replace a much larger and less reliable interconnect and support circuitry for less cost. Each and every year, more and more can be compressed into the same small area of silicon which makes it the envy of package research engineers. It must be remembered that not all the components and functionality are integrated onto the silicon. There is a cost prohibitive and functionality flexibility issue that governs what is included on the silicon. The same is true for a support component and interconnect technology; include only what is cost effective.

The last five years has seen a boom in Integrated Passive Components (IPCs) and Integral Substrate (IS) research. This Chapter will review the work that has been conducted and hence published in this area with regard to Aluminum Nitride (AlN). While the majority of this Dissertation is concerned with thick film component integration on AlN, this literature review will give a broad review of the IS research in this area.

With the electronics era booming, the demand on the nation’s power grid has become excessive. Computers, televisions, and lighting all put large demands on the power generation plants. It as now become common place to make these components “Green”. The term originating from an environmental perspective, “Green” devices are highly efficient and power themselves down when not in use. This means they use less power, in turn, cause less natural resource to be used in power generation, and thus benefit the “Green” biological environment.

So what does all this “Greenness” mean for the power electronics engineer? Well, the old power supplies are no longer satisfactory. They are physically large, inefficient, and do not power themselves down when not in use. Not only do these new supplies have to be small, more efficient, and smarter, but the trend to lower the operating voltages on the integrated circuits has increased the current demand from these circuits. To pack more transistors onto the same size piece of semiconductor, the gate length of the transistor is reduced. this reduction in gate length
lowers the breakdown voltage of the device. To remedy this problem, the operating voltage of the circuit is lowered. While the voltage has been lowered, many more transistors reside in the same area. This results in the IC needing the same amount of power to operate. Ohms law tells us that if the power remains the same and the voltage decreases, then the current must increase. Peak currents of 20 to 30 amps are not uncommon for today's computer systems.

2.1. Passive Components

Passive components can be applied in several ways. The oldest method is the through hole component. The passive has two or more wire leads which are inserted through the substrate and solder attached to the opposite side of the substrate. The surface mount passive is usually a small rectangular ceramic based, single or multilayer, component. Often called chips, either end is metallized and attached to a substrate by solder attachment on the component side of the substrate. An Integral Substrate has passive components incorporated in the substrate or some other part of the circuit, such as on the semiconductor die itself. The integrated component can be one of two types, either on the surface of buried within multiple layers. An IS component is not solder attached, but is deposited by a thick or thin film process and is in intimate contact with the metal traces and substrate or the semiconductor die.

The surface mount component is now typically used when circuit miniaturization if to be performed. It has taken about fifteen years for surface mount components to become commonplace over the passive through hole counterpart. This time transition can be attributed to the materials, processes, standards, CAD tools, and equipment necessary it implement Surface Mount Technology (SMT) components. The initial switch from through hole components to SMT
components provided a reduction in size while larger cost reductions were achieved later as the standards were established and processes, materials, and equipment became common place.

A typical cellular phone may have upwards of 1000 passive components. In contrast, there may only be 20 to 30 integrated circuits on the same board. Typically, there is a 20:1 passive to IC ratio in cellular phone units and the ratio can reach as high as 40:1 for items such as pagers [REC98]. As an example, the Motorola StarTAC cellular phone uses 993 passive components and 45 integrated circuits; a 22:1 ratio. At an average cost of conversion (cost of purchase, stocking, placement, test, repair, and warranty) of $0.023 per passive component, passives account for $23 in this unit [BOW98]. Another example, the Motorola pen pager uses 142 passives and 3 integrated circuits; a 47:1 ratio.

With these high ratios, it is undisputed that the reduction in the size of passive components will result in very large reductions in overall circuit area and volume. The question becomes: what is needed to cross the gap and reduce the size of the passives?

Several issues must be resolved in order to advance this technology. The first hurdle is the technological knowledge needed to integrate components. Materials and processes must be investigated. CAD tools must be developed that can accurately model the new components. And most importantly, the present status quo must be challenged in order to get manufacturers to change from surface mount components to integrated component versions.

Current size reduction efforts for SMT passives have centered around reducing the physical size of the chip. Where “0805” (80mils x 50mils) components were common, passive SMT components are now commonly “0603” (60mils x 30mils) and are moving to “0402” (40mils x 20mils). As the size continues to decrease, the complexity of the pick-and-place machines used to attach the SMT components increases significantly. Solder or conductive epoxy
attachment also becomes increasingly more difficult as solder and epoxy bridging will become more common.

When reduction efforts involve using the same technology, the new process tends to be adopted rapidly. With transistor integration, ultra miniaturized circuits have been achieved since reduction has been based on the same technology with advancements being made in methods of gate length reduction. If higher transistor integration and faster transistor operation were based on a major technology change, for instance, silicon based MOSFETs to Gallium Arsenide based MESFETs, integration may not have progressed as fast. Probably the biggest reason for this is that people do not like change. If something works, it is generally accepted that small modifications will continue to be used until a new technology is good enough to dethrone the old one. The capital cost required to switch over to all new equipment must be justified along with the risks of a positive return on the investment. But if accepted, a technological breakthrough is said to have occurred.

IPCs and ISs are at the edge of a technological breakthrough. Each technology is vying for position to acquire the small advantage that will give it the edge to push it into mass acceptance. While each IPC ad IS method holds a nitch market, the one explosive technique has yet to surface. If IPC or IS could be adjusted as easily as an EEPROM while maintaining a cost and size advantage, then we would see a huge shift in the passive market. Perhaps an electrically adjustable passive technology is on the horizon, but until then, there are several viable technologies almost ready for production, including passive components developed in this research.
2.2. Integrated Components and Integral Substrates

This section will survey the current published developments in ISs and IPCs. ISs can be placed into two categories; thick film components screen printed on a single or multilayer ceramic or polymer, or thin film deposited onto a polymer, ceramic substrate or silicon die.

2.2.1. IS and IPC Development

By the middle of the 1990’s, the industry was beginning to take note of the fact that the percentage of passives used for a particular application was increasing. Not all the support passive components were being integrated into silicon as expected. For instance, the Intel 486 computer used 124 passive components while the next generation processor, the Pentium®, used 252 [ZAN91]. Another example is that 90% of all components in a cellular telephone are passive [LIO97A].

This increase in the number of passives started to make the electronics industry look for a solution to this growing problem. Integrated passive components would solve many of the problems if low cost and design flexibility could be achieved. The initial problem is that IPCs, multiple resistors or capacitors in one package, cost 50% to 100% more than discrete components [MCK97] and the price will not drop until the demand goes up. While component cost is higher, placement and rework costs should be lower. Reliability would also be expected to increase since fewer solder joints and connections are needed.

To help get integrated passives off the ground, the Electronic Industries Association (EIA) decided to set up standards for IPCs and ISs [LIO97a]. While standards are still being developed, proprietary configurations will enter the market. Most of these standards will be for multiple passives in a package. The National Electronics Manufacturing Initiative (NEMI) has created a
passive component road map which forecasts the trends in passive components [REC97a]. This road map predicts that hand held wireless products will move from 14 components per cm² to 54 components per cm² in seven years. This correlates to a 300% increase in component density.

To help identify the emerging technologies, NEMI has categorized passives into four groups, namely,

1. Discrete components
2. Integrated passive components (IPC)
3. Integral substrates (IS)
   a. IS-O (Organic)
   b. IS-C (Ceramic)
   c. IS-S (Silicon)
   d. IS-G (Glass)
4. On chip

No one technology at this point stands out as a future industry leader, but discrete components has the short term lead due to the fact that reduction efforts are geometry based using current technology.

2.2.1.1. Integrated Passive Components (IPCs)

Two directions have emerged, integrated passives and integral passives. The first, integrated passives, is an idea that has spawned from makers of passive components. Typically, surface mount components are manufactured as individual components on small pieces of ceramic. Metallization is then added to ceramic and the device is surface mounted on the circuit board. Integrated passives attempt to incorporate several passive devices onto a single piece of ceramic. Multiple metallization terminations are added to the single piece of ceramic. This in turn will reduce the cost of several mounted components to the cost of picking and placing a single component. It will also reduce the area. Current cutting edge passive technology uses 0402
(4 mils by 2 mils) chip size. A limitation due to the accuracy of the pick-and-place machines that mount the passives onto the circuit board. For example, an integrated resistor may contain four resistors in a single package. Each resistor within the package may be 2 mils by 1 mils, and the overall package size on the order of 11 mils by 2 mils (1102), an area of 22 mils$^2$ (accounting for a 1 mil internal space between components and 2 mils being the smallest dimension that a pick-and-place machine can accurately mount). The equivalent area of four 0402 resistors is 32 mils$^2$. Already, there is area reduction before tolerances of pick and place machines are taken into account (space needed between devices). The cost reduction will be four to one for placement. Although, there may be a slight increase in cost and area due to more complex interconnect routing.

2.2.1.2. Integral Substrates (ISs)

The second direction, integral passives, incorporate the components into the circuit board, substrate, or directly onto the integrated circuit. On ceramic, these devices are either thick film screen printed were deposited using thin film techniques (sputtering and evaporation). On polymers, the devices may either be thick film screen printed, thin film deposited, or incorporated into an individual layer, and then laminated together into a multilayer substrate.

Ceramic has the ability to integrate passive components, while Low Temperature Cofired Ceramic (LTCC) can even bury these components on inner layers. The problem is essentially cost. The size reduction that can be achieved with ceramic substrates, at this time, is not great enough. Thick film technology offers the cheapest solution, but resolution is limited to several mils. Thin film technology can reach sub mil ($< 25\mu m$) resolution, but it still is a costly process for the size
that can be achieved. There are even thick film pastes that are processed like thin films with an etch process. This process may the intermediate solution.

2.3. Thick Film AlN

Thick film technology has been around since the 1960’s. Techniques for passives are well established for alumina and for surface passives on alumina based Low Temperature Cofired Ceramic (LTCC). In its infancy, thick film technology was used when small, lightweight, medium production volume circuits were required. For instance, in the aerospace industry, size and weight are more important than cost issues.

Thick film technology not only has the advantage of integral passives, but these components can be made small since the thermal conductivity of alumina far exceeds that of a printed circuit board. RF applications tend to convert a large amount of electrical energy to thermal energy and alumina is a good substrate material for removing this heat from localized hot spots.

With the greater need for more compact circuits, thermal density increased significantly. Beryllia (BeO) was developed into a thick film substrate and new thick film materials were developed for this substrate. The drawback is that beryllia is considered a toxic material, once it is machined, cut, or fractured the resulting beryllia dust can cause a lung conduction known as berylliosous. While the thermal conductivity of beryllia is ten to twelve times that of alumina, its health concerns have kept it from having mass appeal. As a result, there was a search for a material with high thermal conductivity and no toxicity. Aluminum Nitride (AlN) emerged as one possible solution.
The mid 1980’s, Toshiba Corporation reported several technological advances on AlN as a suitable hybrid substrate. In 1984 and 1985, Toshiba Corporation began to publish their findings on AlN as a multilayer and single layer prefired thick film substrate compatible technology [IWA84a, IWABB, IWA84b, IWACC]. Iwase, of the Toshiba Corporation, developed a method for using thick film gold (Au), Silver-Palladium (Ag/Pd) and copper (Cu) on AlN substrates. The thermal conductivity of the AlN at this time was 60 to 100 W/mK, still well below BeO which has a thermal conductivity of 250 W/mK but, well above alumina at 20 W/mK. This research paved the way of AlN as a viable thick film substrate.

This type of thick film could also be applied to standard firing conditions as Al₂O₃ [IWAAA]. This was significant since when manufacturing a great deal of time is required to set a belt furnace to a desired profile, and once the desired profile is achieved, a manufacturer will be reluctant to change it. Currently, since one profile could be used for both Al₂O₃ and AlN, adoption would become much easier.

Further characterization was conducted by Bloom [BIOAA]. The reliability of Copper (Cu) thick film was conducted. It was found that Cu adhered well to AlN. This research used AlN with thermal conductivity of 170 W/mK. It was found that an AlN substrate could withstand four times more power cycles and a greater number of thermal shocks than Al₂O₃.

Thick film characteristics on AlN was investigated by Dettmer [DET87a]. Both conductor pastes and a low dielectric constant, K, dielectric pastes produced by DuPont were found to be compatible on AlN substrates. This research proved that standard printing and processing, as used with Al₂O₃, could be used to develop thick film AlN Circuits. The phenomena of thick film paste blistering is mentioned in this dissertation. This can occur when the nitrogen is released from the substrate and rises up through the paste during firing.

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In 1987, Dettmer published a paper that exposed some of the issues that needed to be resolved before AlN could become a viable thick film alternative substrate [DET87a, DET87b]. It was found that on some manufacturers AlN substrates, (specifically Toshiba) the surface layer was actually an oxide, $\text{Al}_2\text{O}_3$, to be exact. This would explain why in previous studies, thick film materials for $\text{Al}_2\text{O}_3$ substrates would work so well on AlN. Other manufacturers substrates did not have this surface layer of Oxide. As a result, the surface does not have the same smooth topology. This roughness can cause poor line resolution when printing thick films. The absence of an oxide may also cause adhesion problems if $\text{Al}_2\text{O}_3$ pastes are used since the oxide is used as the bonding mechanism in these pastes, therefore; new formulations of paste maybe required for AlN.

The thermal conductivity of AlN can be controlled by the amount of oxygen content introduced into the sintering process during the formation of the substrate. [IWADD]. The tradeoff is that the less oxygen introduced, the higher the grain boundary.

2.4. Low Profile and Planar Magnetics

Magnetic components are one of the physically largest elements in an electronic circuit. In the most basic form an inductor is several turns of wire (metal conductor) and a transformer is two or more separate coils of wire magnetically coupled.

Miniaturization efforts of magnetic components must center around several critical issues. The current through the conductor governs the size of it’s cross sectional area. If the wire is too thin, current will generate excessive heat in the conductor due to its inherent resistance. This heat will melt the conductor and create an open circuit. If this excessive heat can be removed, smaller and thinner conductors can be used.
Skin depth of the conductor also places a restriction on the thickness. For high frequency operation (100kHz and above), the charge within a conductor will concentrate on the outer perimeter. The skin depth is the depth where the current density decreases to about 37% of the current density at the surface of the conductor. For a metal conductor the skin depth is expressed as:

\[
\text{skin depth} = \frac{K}{\sqrt{f}}
\]

Where K is a constant that depends on the metal material and f is frequency. For a cylindrical wire with a diameter of greater than two skin depths, there will be essentially no current flowing in the center. To improve the energy storage characteristics of a magnetic component, a high flux density is desired. If the conductor windings can be made small, they can be placed closer together thus increasing the flux density.

Iron and ferrite cores are also used to concentrate the flux density around the conductor coils. The permeability of these materials, particularly ferrites is very temperature dependent. As the core material has a magnetic resistance which will cause it to heat up when a magnetic field is applied. If the temperature becomes too high the permeability will decrease causing the inductor or transformer to saturate. For two identical transformers, the one with superior thermal management will be capable of transferring larger amounts of electrical power. What it all comes down to is that a magnetic component has core losses and winding losses. It is through the effective management of these losses that miniaturization will be achieved.

Planar magnetics has emerged as the leader in the area of transformer and inductor miniaturization. Instead of a wire wound bobbin, a planar magnetic uses several layers of flat spiral windings separated by an insulating material and then laminated into thin multilayer substrate [EST89]. A core can be attached to help increase the flux density within the windings.
Planar magnetics have many advantages over the traditional wire wound bobbin and core magnetics. The construction of these magnetics can use traditional multilayer Printed Circuit Board (PCB) fabrication techniques; therefore, they are typically part of the circuit board itself. This technique provides consistent and precise devices, even when manufactured in high volume. Flexible circuits (copper and Kapton laminates) and stamped-copper foils are other popular techniques for planar magnetic construction [DAI94].

Since the conductor traces are flat and wide, both sides of the conductor act as a surface for current. The skin effect becomes less of a factor than in the traditional cylindrical wire wound magnetics. Expensive Litz wire (multistranded individually enameled wire) is often used in traditional wire wound magnetics to reduce the skin effects. Flat wide conductors avoid the currentless inner region associated with a cylindrical conductor by spreading the charge over a larger surface area. It is this low area/perimeter ratio that keeps the AC resistance low in planar magnetics [PRI96].

Another advantage is the low profile of planar magnetics. The height of a planar magnetic is governed by the height of the windings along with the height of the core. The winding window is thin because of the thin nature of the windings. In turn the core is kept thin in profile. Since the size of the overall circuit is very often governed by the height of the magnetic, planar magnetics allow for smaller and thinner circuits to be constructed. The volume of the overall magnetic can be reduced by reducing its height, but there is a point beyond which further height reduction will require an increase in the volume to maintain the same power density [DAI96].

Several algorithms have been developed to efficiently and systematically design planar magnetics. Rascon published a paper on the design of low profile magnetics using flex coils [RAS97]. Custom cores were designed with a height under 4mm, and flex foil was used for the
windings. Optimization was achieved by use of a Finite Element Analysis (FEA) computer program. Rascon found that the proximity of the windings in relation to the gap affected the losses. If the windings are placed close to the gap, AC winding and resistance losses increase. It was found that increasing the separation between the gap and the windings reduces the AC resistance but the influence is not great. A distributed gap can reduce the winding resistance and thus conductor losses, but may increase manufacturing costs.

Huang investigates design techniques for planar windings with low resistances [HAU95]. Detailed mathematical relations are given for circular, spiral, and rectangular patterns. Relations are also given for windings of variable turn widths. By varying the width of the conductor as it spirals toward the outer conductor, the resistance can be kept constant thus reducing conductor loss. The mathematical relations are verified using a FEA program and found to be within 10% of each other.

Planar transformer optimization techniques have been developed by Prieto [PRE96]. The research investigates easier and cheaper methods to produce planar magnetics. A method for a multilayer PCB transformer is developed.

Cobos has developed a low profile planar transformer using a ferrite substrate and a multiple layer thick film spiral [COB97]. The prototype was used on a DC to DC converter. The design is limited to four printed conductor layers which is attributed to the process limitations of thick film technology. FEA analysis was conducted in order to optimize the design. The models predicted by the FEA program were then compared to the constructed prototype.

Several problems exist with planar magnetics. Assembly techniques are still in their infancy, therefore, relatively expensive. The close proximity of the windings can cause undesired
capacitive coupling between the windings. Thermal management has also been a large problem. Maximum heat rise is limiting the power density of planar magnetics.

Typical techniques that have formally been classified as Hybrid techniques can be used to miniaturize planar magnetics. The first problem is the thermal management. Ferrites are extremely temperature dependent. The temperature rise in the core limits the size and the amount of power that can be stored. One technique that has not been explored if the intimate coupling of the ferrite to a high performance substrate. Conductive epoxies have been used to couple the ferrite to the substrate but it may also be possible to sputter a thin film to the bottom of the core and then solder attach the core to a high performance substrate.

Solder would provide a better thermal path out of the ferrite. This would effectively increase the power density of the magnetic by lowering the temperature rise for a given input. The stress analysis would need to be conducted between the substrate and the ferrite to ensure that separation or fracturing of the ferrite or substrate will not occur.

High performance substrates such as Al₂O₃, AlN, AlSiCs, and other Metal Matrix Composites (MMCs) could be used better manage the thermal buildup in the core. While these materials come at a premium cost, there are applications where a higher cost can be justified in exchange for size. Thermal simulations would provide an excellent means of initial evaluation of the best configuration of substrate material and planar magnetic power density. A FEA program such as Flotherm™ could be used for such an analysis.

There is also the possibility of a multilayer planar magnetic component using Low Temperature Cofired Ceramic (LTCC). The same experiments and analysis that the literature review revealed could be applied to LTCC spiral inductor with an attached ferrite core. LTCC with a higher thermal conductivity than PCB would help remove the heat due to the copper.

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losses. It also has the capability on integral resistors and capacitors. this would allow the entire circuit to be fabricated into a single multilayer substrate, contain planar magnetics and integral passives all in a reduced miniature size.

Thick film on AlN and Al₂O may also provide an answer. Some investigation into a screen printable thick film ferrite paste has been conducted. The problem at this time is that the permeability of the paste is very low, around 10. this does not mean that future research will no develop a paste with a reasonable permeability, tens of thousands. This is an area where a break through could occur. Of course the same applies to thin film, if a high permittivity material can be deposited, integral inductors would become common place.

These are just a few of the many possibilities that can be applied to planar magnetics using traditionally Hybrid techniques. Thermal management is critical in miniaturization and many of the new MMCs can help. These areas should be explored in the effort to increase the power density of magnetics.

2.5. Switchmode Power Supplies (SMPS)

The research work in this dissertation concentrates on power supply miniaturization; in this regard is important to the general understanding of the switch mode power supply topologies. This section will review the current, most popular types of power supplies. Characteristics of each type of supply and the benefits and disadvantages will be given. New designs and novel switching techniques are continuously being developed but the overall concept remains unchanged. This overview is meant to give insight so that the switch mode power supply miniaturization research, described in later chapters, may be understood.
A power supply design starts out with the specification of several design criteria. These criteria are as follows,

1. Weight.
2. Volume.
3. Power.
5. Heat generation.
7. Efficiency.
8. Time to market.

To achieve these goals, a power supply can be classified into three types of systems: Linear power supply, Pulse Width Modulated switching power supply, Quasi-resonant and Resonant switching power supply.

### Linear Power

A linear power supply is characterized by the way it regulates power with the use of an active device operating as a variable conductance. In the most common linear power supply, the series-pass regulator, the active device is placed between the input voltage source and the load and it is used to drop a high input voltage to a lower regulated output voltage. The load current must pass through the active device while it is dropping the difference of the input voltage and the load voltage. Large amounts of power are therefore dissipated in the active device and in turn this power loss in the active device is transformed into heat. This power loss and the corresponding heat generation is the cause of the low efficiency rating of this type of power supply, typically 30 to 50 percent. Reasonable heat sink size limits the linear supply to less than 10 watts of output power.
The advantage of the linear supply is that since the active device is not actually switching (turning completely on and off) but acting as a variable conductance, very little noise is generated. The low noise figure of the linear power supply makes it very popular in Radio Frequency (RF) applications, medical monitoring, and environmental measuring systems. Another advantage is low cost and short development time. For off-line applications, an isolation transformer can be easily added to protect the load from high power line level voltages. The linear power supply is typical of the plug in wall supply that accompanies most small consumer electronic components such as answering machines, TV video games, and laptop computers. Also, linear power supplies are used in system level design where a main supply voltage must be further reduced and regulated for a low power subsystem.

**Pulse Width Modulated (PWM) switching power supplies**

A PWM power supply can be characterized by the active devices being operated as a switch; either fully on of fully off. Several different types of semiconductor devices are used as these switches including but not limited to: MOSFETs, IGBTs, diodes, BJTs. A capacitor-inductor combination, used as an energy storage medium, along with a properly configured switching configuration, is used to convert the input voltage to the desired regulated output voltage. A PWM power supply is much lower in weight and size than an equivalently rated linear supply. A low volt-ampere product across the active devices is maintained through the use of microprocessors or Application Specific Integrated Circuits (ASICs). Keeping either the voltage across the device or the current through the device zero when switched, then very little power is dissipated in the device and the overall power supply efficiencies can reach from 70 to 85 percent. It is the high efficiencies that permit these supplies to deliver output power in excess of several
thousand watts. For low power applications, an advantage is achieved over the linear supply since much smaller heatsinks are required for the same output power level.

Unlike the linear power supply, the PWM supply can produce output voltages lower or higher than the input voltage by different configurations of the capacitor, inductor and switches. The two general categories are forward-mode (buck converter) which produces a lower output voltage than input voltage and the flyback-mode (boost converter) which produces a higher output voltage than the input voltage. There is also a combination of the two, buck-boost, which can perform both functions by adjusting the switching times.

The PWM supply has the advantage of efficiency, versatility and size over the linear supply but at expense of higher cost, more complexity, and higher RF noise. The numerous active devices and ASICs not only monetarily drive up the cost of the PWM supply but also generate RF noise at the fundamental switching frequency as well as numerous harmonics. A PWM power supply designer must be an analog, digital and RF designer in order to successfully develop such a design. This deeper complexity leads to longer development time. PWM supplies have found a market where the higher cost of development and electronic components, and longer development time is repaid by savings in operational efficiency and smaller size. IC manufactures, such as IR and Motorola, have produces generic ASIC controllers that have helped reduce development time and design complexity.

**Quasi-resonant (QR) and resonant switching power supplies**

Quasi-resonant and resonant switching power supplies are a variation of pulse width modulation power supply discussed the previous section. These type of supplies are smaller and lighter weight than the PWM supplies. The Quasi-resonant and resonant supplies also have lower
radiated and conducted EMI and RFI for a comparable rated power supply. The tradeoff in using this type of supply is that development time is greatly increased. It is much more difficult to design and debug this type supply. But if this increased development time can be tolerated, the benefits are reduced size, reduced weight, increased efficiency, and lowered EMI. For these reasons these type of supplies currently used in high-end systems, such as, military aircraft, space applications, and other applications were size, weight, efficiency, and low EMI are more important than cost and design time.

Quasi-resonant and resonant power supplies achieve their improved characteristics by forcing the voltage and current, through the main switching components, to be sinusoidal. These switching methods have reduced the power losses within the switching components. As a result, higher operating frequencies may be used without incurring large power losses. As a direct result, the storage devices used in the power supply, inductors and capacitors, can be made smaller in value and physical size. This is the trend seen in power supply design today; circuit design topologies that reduce frequency and switching loss and then increasing the frequency of operation in order to reduce component size. The operating frequency is currently limited by component and layout parasitics, magnetic losses (eddie currents, skin effects, and hysterisis). It is knowing and predicting these losses that increases design time and development.

The Quasi-Resonant (QR) supply is generally classified into two categories, the Zero Current Switching (ZCS) supply and the Zero Voltage Switching (VCS) supply. In order to reduce power losses in the switching semiconductors, it is desired that either the current or the voltage be equal to zero at the time when the power semiconductor switches turn off or on. The QRZCS forces the current through the power switch to be sinusoidal and equal to zero when it is switched. The QRZVS forces the voltage through the power switch to be sinusoidal and equal to zero.
zero when it is switched. The QRZVS topology is more popular for several reasons. One is that the operation is less dependent on the circuit parasitics. Another is that QRZVS have better performance for larger loads.

### 2.6. Switchmode Power Supply Miniaturization

There are several instances in literature citing power supply miniaturization. Most of these center around what was once called hybrid techniques. This involved using ceramics, both prefired and fired, with either thick film, thin film, or direct bond copper. These designs did not consider integrated passives, cost, or combined substrate technologies. The research in this dissertation builds upon this previous research.

The first hybrid switchmode power supply designs to began to appear in the mid 1980s. Hopkins publish a paper describing a 2 MHz off-line quasi-resonant switch mode power supply using hybrid thick film techniques. This application used a quasi-resonant zero current topology. This 84watt circuit was developed to work directly off the power line (off-line) of 300 volts DC input. Switching was conducted at 2MHz. efficiency ratings reached 74 percent, and power density was 36W/in³. Skin effects due to the higher resistivity of the conductor traces was investigated and compensated for [HOP88, HOP89a].

Effects of thick film conductor impedance, in some applications, can cause high loss. Hopkins also published a separate paper discussing appropriate trace thickness and width for thick film power hybrid circuits. High frequency operation was considered, above 100kHz. Those found that optimum conductor thickness of $\pi$ times the skin depth, or a thickness of approximately three times the skin depth, introduces a less than 1.2 percent increase in resistance.
This value holds true for square conductors where the width is much greater than the thickness and fringing effects and corner current crowding is negligible [HOP88].

A high frequency hybrid power transformer design was developed by Gradzki [GRA88]. This design used a ferrite substrate, thick film windings, and an attached ferrite E-core. The transformer was designed to operate at 6 MHz and 40 watts. The design was implemented in a power supply in which the input was 50 volts and the output was 5 volts. The maximum efficiency achieved in this design was 71 percent. While design and operation was verified, no attention was given to electrical properties of the remaining circuit on the ferrite substrate for mechanical rigidity of the transformer.

Miwa reports on a 50W, 5MHz, 40V input, 5V output DC to DC converter [MIW89]. This circuit used prefired ceramic with copper thick film conductors. This paper covers the processing steps necessary to print copper thick film traces on prefired ceramic. Copper offers the benefit of having lower trace resistance and therefore lower power loss but at the expense of higher processing costs. Unlike silver and gold thick film conductors that can be fired in air, copper must be fired in a nitrogen atmosphere. The paper goes on to explain how copper thick film traces improve operation and reduce loss.

A paper by Satyanarayana presents an overview of the design and manufacturing considerations for power hybrid design [SAT89]. Issues such as current density, trace resistance, voltage isolation, and thermal resistance are covered. While not technically extensive, the paper describes the pertinent issues for design. Likewise Hopkins has a similar publication [HOP89b].
2.7. Conclusions

The explosion of wireless and portable communication products into the electronics market has put a large demand on the requirements of their respective passives. The semiconductor sector has been successfully miniaturizing circuits with a steady trend that appears will continue in the near future. In contrast, the support components have yet to reach a miniaturization rate comparable to that of the semiconductor sector. The passive components are an integral part to any piece of electronics equipment and therefore has become a limiting factor to overall circuit size reduction. Research and development are necessary in this area to help eliminate the growing gap between the semiconductor and passive component miniaturization rates.

For ISs and IPCs to succeed, they must be as convenient to use, cheaper, and at least as reliable as present SMT components. It is convenient to replace a SMT component with another during the manufacturing of a circuit if it is determined that it has drifted or fails to meet specifications. Using SMT components, it is relatively simple to develop a single circuit to perform multiple functions by simply changing out a few passives. For instance, making a radio receiver for both US and European markets. Simple adjustments of the LC tank circuit elements can adjust for the frequency standard differences.

Introduction of integrated passives into SMPS design will help to close the miniaturization gap between integrated circuits and respective power supplies. The research presented will develop solutions to the miniaturization problem, both through integrated passives and control module technology, expanding on the work previously developed by others in the industry.
3. Capacitors

This chapter will discuss the formation of thick film capacitors, intended for use in Switched Mode Power Supplies (SMPS), on prefired Aluminum Oxide (Al₂O₃) and prefired Aluminum Nitride (AlN). Described is the test coupon composed of an array of thick film resistors and capacitors used to characterize the materials and processes. Functional device formation was developed through an iterative manufacturing process of the test coupon. Several process variations were conducted until the passives obtained the desired characteristics. The passives thus developed are subjected to electrical and thermal evaluation.

3.1. Thick Film Processing

This section will contain a brief overview of processing steps required to generate a thick film circuit on a prefired piece of ceramic. This review is intended to familiarize the reader with the basic steps of thick film processing and by no means is meant to be an exhaustive coverage of the process.

A prefired ceramic substrate thick film circuit consists of a base layer prefired ceramic with successive layers of the paste material deposited one layer at a time until the complete circuit has been fabricated. Each layer consists several processing steps: screen printing, drying, firing.

The screen printing process is very similar method is used for the generation of patterns on T-shirts. This method developed by ancient Egyptians, has since been redefined for use in modern electronics [LIC88]. In electronics, the screen printing process begins with a stainless steel or polyester fine mesh screen. A photo sensitive polymer emulsion is applied to the screen and the desired pattern is then photo developed. This leaves open areas in the screen. The screen is
mounted into a screen printer which consists of a base plate to hold the ceramic substrate, an apparatus to hold the screen in place over the substrate, and a squeegee which contacts the screen.

The purpose of the screen printer is to force the paste through the openings in the screen and deposit it upon the substrate below. Depending upon the electronic elements desired, metal traces, crossovers, capacitor dielectric, and resistors, are accomplished by applying the appropriate paste for the layer on top of the screen. The squeegee is then pulled across the top of the screen forcing the paste into the open areas and down onto the substrate.

The paste, or sometimes referred to as ink, is still in its viscous state. After printing a single layer, the substrate is allowed to settle at the room temperature for 10 to 20 minutes. The settling time allows some of the organic solvents to evaporate. It also allows any surface irregularities time to smooth over. Next, the paste is dried at 120deg. Celsius to 150deg. Celsius for 10 to 20 minutes. This Drying further removes the organic solvents. If these organic solvents are not removed slowly or completely, nonfunctional circuits will result.

The final processing step, for each layer, is to fire the substrate. This is typically done in a belt furnace consisting of several zones. Typical peak temperature in the center of the oven is 850 degrees Celsius; The actual temperature profile will be specified by the manufacture of the paste. These profiles consist of a suggested ramp up and ramp down temperature rate. This slow ramp up temperature allows the remaining organic binders to be removed. High temperature allows the particles in the paste to bind with the ceramic substrate. The ceramic part is allowed to remain at the peak temperature for approximately 10 minutes. The substrate is then allowed to cool slowly back down to room temperature. This slow cooling rate helps to reduce internal stresses from building up in a ceramic during the cooling process.
Each successive layer of the thick film circuit is printed, dried, and fired. Due to planarization problems, the number of layers is usually limited to 5 to 10. Figure 3.1 shows a cross section of the typical processing steps. Figure 3.2 shows a typical cross section of a completely fabricated thick film circuit. The lowest layer is the substrate. For this application the substrate will either be aluminum oxide or aluminum nitride. The substrates used in this research were 25mils thick. This figure shows the typical metal, dielectric, metal, and resistor thick film circuit. Also shown are surface mount components that are solder attached (a semiconductor die and a chip capacitor) after the thick film processing is complete.

Figure 3.1. Typical Thick Film Circuit Fabrication Process.
- a. Substrate
- b. Metal 1: Print, Dry, Fire.
- c. Dielectric: Print, Dry, Print, Dry, Fire.
- d. Metal 2: Print, Dry, Fire.
- e. Resistor: Print, Dry, Fire.
- g. Component Attach: Reflow Solder.
- h. Wire bond Die Components.
3.2. Materials

To achieve integral components on AlN, new materials were investigated because of the relative immaturity of AlN usage as a thick film substrate. Thick film pastes were obtained from both Ferro and Electro-Science Laboratories (ESL). The pastes obtained from Ferro were developed for use on AlN but a high K dielectric paste was not available. This would limit the passive component integration to resistors only. ESL pastes were developed for use on Al$_2$O$_3$, but the use of a passivation layer of low K dielectric, first printed on the substrate and then proceeding with a normal development process, was investigated. The passivation would allow for the use of ESL pastes which carry a high dielectric value paste.

The passivation layer is required to keep the AlN substrate from oxidizing and forming an aluminum oxide surface and to limit the amount of nitrogen from bubbling up through the successive layers of the thick film circuit. A passivation layer will increase the thermal resistance from the heat producing devices to the heat sink [BAN93]; However, techniques which allow direct placement of major heat producing devices in contact with the AlN substrate can eliminate this problem.

Chapter 3
Figure 3.3 shows a cross-section of a thick film circuit on aluminum nitride a complete passivation layer. The passivation layer is completely printed over the entire substrate, and as a result, the effective thermal conductivity of the substrate will be reduced. In Figure 3.4, only the elements in which was blistering occurs, the printed capacitors and the printed resistors, are protected with an underlying passivation layer. This allows a lower thermally resistive path for the heat generating components, such as, the semiconductor devices.

**Figure 3.3. Thick Film Circuit Cross-section on AlN with Passivation Layer.**

**Figure 3.4. Thick Film Circuit Cross-section on AlN with Partial Passivation Layer.**
3.3. Test Array

To determine the characteristics of the thick film pastes on AlN, an array of resistors and capacitors was printed on both Al₂O₃ and on AlN with a passivation layer and on Al₂O₃ without a passivation layer. The passivation of one of the Al₂O₃ groups will act as a control group for the passivated AlN group. Figure 3.5 shows the AutoCAD® drawing of the test array, consisting of eight resistors and three capacitors. Table 3.1 shows the geometries of these elements.

Resistor pastes are available in sheet resistivities ranging from 10Ω/sq. to 1MΩ/sq, typically in factors of 10 (i.e., 10Ω/sq., 100Ω/sq., 1000Ω/sq....). Proportional mixing of pastes allows for sheet resistivities in intermediary ranges. A resistor may be formed by using a paste with the closest sheet resistivity to the desired element value and then the geometry may be adjusted to obtain the exact value within tolerance. These test substrate geometries were chosen for their relevance to SMPS circuitries. Further discussion of the resistor geometries and fabrication can be found in the next chapter.
Three capacitors were incorporated into the test coupon. The dimensions of these capacitors can be found in Table 3.1. SMPS circuitries require relatively large value capacitors with large voltage breakdown. Because of the typical thick film processing steps, a three layer planar capacitor (metal, dielectric, metal) is common. In contrast to a multilayer ceramic surface mount chip capacitor, a planar integral substrate capacitor will occupy a large amount of surface area.
area. It is for this reason that the capacitors on the test coupon occupy a large portion of the substrate. As dielectric thick film pastes improve and the dielectric constants of these pastes increase, the area required will diminish.

The dielectric constant of a particular thick film dielectric paste is directly correlated to the firing temperatures of all the layers. Breakdown voltage of the capacitor is correlated to the dielectric layer thickness; several printings may be required to form a single layer of desired thickness. For a parallel plate capacitor:

\[
C = \frac{\varepsilon_0 \varepsilon_r A}{t}
\]  

(3.1)

Where,

\[\begin{align*}
\varepsilon_0 & = \text{absolute permittivity of free space.} \\
\varepsilon_r & = \text{dielectric constant of material between plates (K).} \\
A & = \text{area of the plates.} \\
t & = \text{distance between plates.}
\end{align*}\]

Equation 3.1 assumes that fringing effects are negligible in turn which assumes that the plate area is large compared to the distance between them. For electrical testing, the larger the area to perimeter ratio of the test capacitor the smaller the effect due to fringing. Also, when conducting tests with an impedance meter, a larger impedance of the element being tested will lower the percentage of error due to parasitics caused by the leads, probe and contact resistance.

The ESL capacitor dielectric paste has a published dielectric constant of \(K = 6000\) when fired at 900 degrees Celsius. As processing will show this high temperature should be avoided and as a result lower dielectric values result. Regardless, the test coupon was designed of typical SMPS values based on the published values. Once variations are known, adjustments to actual values can be conducted when implementing the elements into specific applications. For a
dielectric constant $K = 6000$, the test coupon will yield capacitors of the values: 50.9nF, 15.3nF, and 126nF for C1, C2, and C3 respectively.

### 3.4. Test Coupon Fabrication

It has been determined that passive component functionality and values on aluminum nitride are much more process dependent than on alumina. Many test trials were necessary to realize acceptable capacitors. The processing of the passivation layer is critical for acceptable capacitor formation. As can be seen in Figure 3.6, capacitor blistering on AlN was a large problem in the first trials. Final trials obtained acceptable capacitor values on AlN (with a passivation layer) without blistering.

![Figure 3.6. Test Resistor/Capacitor Arrays.](image)

*Left - $\text{Al}_2\text{O}_3$ Test Array (Good)*
*Right - AlN with underlayer (Blistered Capacitors and Metal)*

The next four subsections of this chapter are four of the processing trials that were conducted. It was discovered that two passivation layers, equaling a thickness of 1mil, is required to prevent blistering. It was also determined that the greater number of firings also increases blistering. Since more firings, one after each print, helps to increase yield, a trade-off must be
made. Firing the passivation layers after each print or co-firing all the passivation layers also affects the values of the resistors and capacitors, but a fire of the top most passivation layer must be performed before the first layer of metal is applied.

In the next four subsections, the design values and the resultant obtained values of the components are shown in Tables 3.2 through 3.6. The design value was determined from paste data sheets provided by the manufacturer. For resistors, this constitutes the sheet resistivity and the thickness. For capacitors, the value is determined by the dielectric constant $K$ and the dielectric thickness deposited. Variations from the design value, in the resistors, are usually due to the thickness variations. The variation in the capacitors is due to dielectric thickness variation and also very dependent on the firing temperature, which effects the dielectric constant. The ESL dielectric paste increases in $K$ as the firing temperature is increased. Once again, a trade off occurs; more oxidation of the substrate is expected to occur at higher temperatures, thus more blistering. The many capacitor shorts seen in the early trials are due to thin capacitor dielectric deposition. Three printings for a total thickness of 1.46 mil (37$\mu$m) are necessary to avoid this problem. It should also be noted that the thicker the dielectric the lower the capacitor value but the higher the breakdown voltage.

It has been determined that a high resistivity (100k$\Omega$/sq.) and low resistivity (10$\Omega$/sq.) DuPont paste can be successfully incorporated with the ESL passivation underlayer on aluminum nitride. Resistor values varied from expected values but, the resulting resistor values are predictable. Once again, these values correlated to the printed thickness and the surface geometry of the passivation layer on which they are printed.
3.4.1. Test Circuit Development -- Trial #1

Ten test circuits were developed (3 AlN and 7 Al₂O₃). The second layer of capacitor dielectric blistered during firing. The procedure for the circuit development was as follows:

Substrate Preparation

Ultrasonic Cleaning - 10 minutes in soap & 10 minutes in rinse

Screen Production

<table>
<thead>
<tr>
<th>Layer</th>
<th>Mesh Size</th>
<th>Wire Dia.</th>
<th>Emulsion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric underlayer</td>
<td>325</td>
<td>1.1 mil (27.9μm)</td>
<td>CDF4 -- 40μm</td>
</tr>
<tr>
<td>Metal 1</td>
<td>325</td>
<td>1.1 mil (27.9μm)</td>
<td>CDF4 -- 40μm</td>
</tr>
<tr>
<td>Capacitor Dielectric</td>
<td>325</td>
<td>1.1 mil (27.9μm)</td>
<td>CDF4 -- 40μm</td>
</tr>
<tr>
<td>Metal 2</td>
<td>325</td>
<td>1.1 mil (27.9μm)</td>
<td>CDF4 -- 40μm</td>
</tr>
<tr>
<td>Resistor</td>
<td>280</td>
<td>1.2 mil (27.9μm)</td>
<td>CDF4 -- 40μm</td>
</tr>
</tbody>
</table>

Procedure

➤ Print dielectric underlayer on AlN -- ESL D-4907 Lot#: 2514-23
  • Leveling time -- 10 minutes
  • Drying -- 10 minutes @ 125°C
  • Fire -- peak 850°C for 10 to 12 minutes at peak

➤ Print metal 1 layer on AlN and Al₂O₃ -- ESL D-9912 Lot#: 2530-11
  • Leveling time -- 10 minutes
  • Drying -- 10 minutes @ 125°C
  • Fire -- peak 850°C for 10 to 12 minutes at peak
  AlN metal thickness -- 15μm (fired thickness)
  Al₂O₃ metal thickness -- 18μm (fired thickness)

➤ Print first dielectric layer on AlN and Al₂O₃ -- ESL D-4206 Lot#: 2511-32
  • Leveling time -- 10 minutes
  • Drying -- 10 minutes @ 125°C
  AlN metal + dielectric thickness -- 22μm (dried thickness)
  Al₂O₃ metal + dielectric thickness -- 32μm (dried thickness)
  • Fire -- peak 850°C for 10 to 12 minutes at peak
  AlN metal + dielectric thickness -- 25μm (fired thickness)
  Al₂O₃ metal + dielectric thickness -- 25μm (fired thickness)

➤ Print second dielectric layer on AlN and Al₂O₃ -- ESL D-4206 Lot#: 2511-32
  • Leveling time -- 10 minutes
  • Drying -- 10 minutes @ 125°C
AlN metal + dielectric thickness -- 40µm (dried thickness)
Al₂O₃ metal + dielectric thickness -- 37µm (dried thickness)
- Fire -- peak 850°C for 10 to 12 minutes at peak
  <-- Blistering occurred in the dielectric layer on the AlN

Table 3.2. Resistor/Capacitor Values for Trial #1.

<table>
<thead>
<tr>
<th>Substrate Number</th>
<th>1  AlN</th>
<th>2  Al₂O₃</th>
<th>3  AlN</th>
<th>4  Al₂O₃</th>
<th>5  AlN</th>
<th>Design Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor 1</td>
<td>71.3k</td>
<td>70.1k</td>
<td>76.5k</td>
<td>79.4k</td>
<td>83.3k</td>
<td>50k</td>
</tr>
<tr>
<td>Resistor 2</td>
<td>48.9k</td>
<td>56.6k</td>
<td>49.9k</td>
<td>54.8k</td>
<td>58.7k</td>
<td>50k</td>
</tr>
<tr>
<td>Resistor 3</td>
<td>1.13M</td>
<td>1.14M</td>
<td>1.09M</td>
<td>1.17M</td>
<td>1.11M</td>
<td>1.12M</td>
</tr>
<tr>
<td>Resistor 4</td>
<td>13.4k</td>
<td>17.8k</td>
<td>12.8k</td>
<td>14.7k</td>
<td>14.6k</td>
<td>10k</td>
</tr>
<tr>
<td>Resistor 5</td>
<td>12.4k</td>
<td>15.1k</td>
<td>12.7k</td>
<td>14.3k</td>
<td>15.0k</td>
<td>10k</td>
</tr>
<tr>
<td>Resistor 6</td>
<td>10.3k</td>
<td>11.9k</td>
<td>11.0k</td>
<td>11.8k</td>
<td>12.4k</td>
<td>10k</td>
</tr>
<tr>
<td>Resistor 7</td>
<td>320k</td>
<td>341k</td>
<td>300k</td>
<td>336k</td>
<td>306k</td>
<td>350k</td>
</tr>
<tr>
<td>Capacitor 1</td>
<td>b</td>
<td>16.4n</td>
<td>b</td>
<td>17.4n</td>
<td>b</td>
<td>50.9n</td>
</tr>
<tr>
<td>Capacitor 2</td>
<td>b</td>
<td>5.10n</td>
<td>b</td>
<td>5.50n</td>
<td>b</td>
<td>15.3n</td>
</tr>
<tr>
<td>Capacitor 3</td>
<td>b</td>
<td>35.2n</td>
<td>b</td>
<td>37.5n</td>
<td>b</td>
<td>126n</td>
</tr>
</tbody>
</table>

Table 3.3. Resistor/Capacitor Values for Trial #1 (Continued).

<table>
<thead>
<tr>
<th>Substrate Number</th>
<th>6  Al₂O₃</th>
<th>7  Al₂O₃</th>
<th>8  Al₂O₃</th>
<th>9  Al₂O₃</th>
<th>10 Al₂O₃</th>
<th>Design Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor 1</td>
<td>90.3k</td>
<td>87.5k</td>
<td>73.6k</td>
<td>87.4k</td>
<td>83.1k</td>
<td>50k</td>
</tr>
<tr>
<td>Resistor 2</td>
<td>60.1k</td>
<td>60.9k</td>
<td>51.8k</td>
<td>57.3k</td>
<td>52.0k</td>
<td>50k</td>
</tr>
<tr>
<td>Resistor 3</td>
<td>1.29M</td>
<td>1.25M</td>
<td>1.18M</td>
<td>1.20M</td>
<td>1.13M</td>
<td>1.12M</td>
</tr>
<tr>
<td>Resistor 4</td>
<td>16.0k</td>
<td>19.1k</td>
<td>16.5k</td>
<td>18.8k</td>
<td>14.2k</td>
<td>10k</td>
</tr>
<tr>
<td>Resistor 5</td>
<td>14.7k</td>
<td>17.7k</td>
<td>14.8k</td>
<td>16.6k</td>
<td>13.9k</td>
<td>10k</td>
</tr>
<tr>
<td>Resistor 6</td>
<td>12.5k</td>
<td>13.7k</td>
<td>11.5k</td>
<td>12.5k</td>
<td>12.4k</td>
<td>10k</td>
</tr>
<tr>
<td>Resistor 7</td>
<td>345k</td>
<td>352k</td>
<td>338k</td>
<td>351k</td>
<td>317k</td>
<td>350k</td>
</tr>
<tr>
<td>Capacitor 1</td>
<td>14.7n</td>
<td>15.6n</td>
<td>14.8n</td>
<td>16.9n</td>
<td>21.6n</td>
<td>50.9n</td>
</tr>
<tr>
<td>Capacitor 2</td>
<td>4.70n</td>
<td>4.75n</td>
<td>5.00n</td>
<td>4.98n</td>
<td>7.84n</td>
<td>15.3n</td>
</tr>
<tr>
<td>Capacitor 3</td>
<td>35.5n</td>
<td>39.3n</td>
<td>36.2n</td>
<td>40.8n</td>
<td>44.8n</td>
<td>126n</td>
</tr>
</tbody>
</table>

b -- blistered
s -- short
3.4.2. Test Circuit Development -- Trial #2

Twelve test circuits were developed (3 AlN with underlayer, 4 Al₂O₃ with underlayer and 5 Al₂O₃). The capacitors on the substrates with an underlayer do not perform electrically. The procedure for the circuit development was as follows:

Substrate Preparation

Ultrasonic Cleaning - 10 minutes in soap & 10 minutes in rinse

Screen Production

<table>
<thead>
<tr>
<th>Layer</th>
<th>Mesh Size</th>
<th>Wire Dia.</th>
<th>Emulsion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric underlayer</td>
<td>325</td>
<td>1.1 mil (27.9µm)</td>
<td>CDF4 -- 40µm</td>
</tr>
<tr>
<td>Metal 1</td>
<td>325</td>
<td>1.1 mil (27.9µm)</td>
<td>CDF4 -- 40µm</td>
</tr>
<tr>
<td>Capacitor Dielectric</td>
<td>325</td>
<td>1.1 mil (27.9µm)</td>
<td>CDF4 -- 40µm</td>
</tr>
<tr>
<td>Metal 2</td>
<td>325</td>
<td>1.1 mil (27.9µm)</td>
<td>CDF4 -- 40µm</td>
</tr>
<tr>
<td>Resistor</td>
<td>280</td>
<td>1.2 mil (27.9µm)</td>
<td>CDF4 -- 40µm</td>
</tr>
</tbody>
</table>

Procedure

➤ Print dielectric underlayer on AlN and on five Al₂O₃ -- ESL D-4907 Lot#: 2514-23
  • Leveling time -- 10 minutes
  • Drying -- 20 minutes @ 125°C
  • Fire -- peak 850°C for 10 to 12 minutes at peak

➤ Print second dielectric underlayer on AlN and on five Al₂O₃ -- ESL D-4907 Lot#: 2514-23
  • Leveling time -- 10 minutes
  • Drying -- 20 minutes @ 125°C

➤ Print metal 1 layer on AlN and all Al₂O₃ -- ESL D-9912 Lot#: 2530-11
  • Leveling time -- 10 minutes
  • Drying -- 20 minutes @ 125°C

➤ Print first dielectric layer on AlN and all Al₂O₃ -- ESL D-4206 Lot#: 2511-32
  • Leveling time -- 10 minutes
  • Drying -- 20 minutes @ 125°C
  • Fire -- peak 850°C for 10 to 12 minutes at peak
    AlN metal thickness -- 10µm (fired thickness)
    Al₂O₃ metal thickness -- 10µm (fired thickness)
    AlN metal + dielectric thickness -- 30µm (fired thickness)
    Al₂O₃ metal + dielectric thickness -- 30µm (fired thickness)
Print second dielectric layer on AlN and all Al$_2$O$_3$ -- ESL D-4206 Lot#: 2511-32
- Leveling time -- 10 minutes
- Drying -- 20 minutes @ 125°C
- Fire -- peak 850°C for 10 to 12 minutes at peak

Print second metal layer on AlN and all Al$_2$O$_3$ -- ESL D-9912 Lot#: 2530-11
- Leveling time -- 10 minutes
- Drying -- 20 minutes @ 125°C

Print resistor layer on AlN and Al$_2$O$_3$ -- DuPont 1940-D 100KΩ/sq
- Leveling time -- 10 minutes
- Drying -- 20 minutes @ 125°C
- Fire -- peak 850°C for 10 to 12 minutes at peak
  Al$_2$O$_3$ resistor thickness -- 17µm (fired thickness)
  Al$_2$O$_3$ (with underlayer) resistor thickness -- 15µm (fired thickness)
  AlN metal + dielectric thickness -- 14µm (fired thickness)

Table 3.4. Resistor/Capacitor Values for Trial #2.

<table>
<thead>
<tr>
<th>Substrate Number</th>
<th>1 Al$_2$O$_3$</th>
<th>2 Al$_2$O$_3$</th>
<th>3 Al$_2$O$_3$</th>
<th>4 Al$_2$O$_3$</th>
<th>5 Al$_2$O$_3$</th>
<th>Design Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor 1</td>
<td>1.28M</td>
<td>1.30M</td>
<td>1.30M</td>
<td>1.27M</td>
<td>1.37M</td>
<td>500k</td>
</tr>
<tr>
<td>Resistor 2</td>
<td>1.41M</td>
<td>1.42M</td>
<td>1.37M</td>
<td>1.38M</td>
<td>1.41M</td>
<td>500k</td>
</tr>
<tr>
<td>Resistor 3</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>11.2M</td>
</tr>
<tr>
<td>Resistor 4</td>
<td>163k</td>
<td>161k</td>
<td>160k</td>
<td>164k</td>
<td>158k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 5</td>
<td>285k</td>
<td>281k</td>
<td>260k</td>
<td>263k</td>
<td>252k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 6</td>
<td>304k</td>
<td>304k</td>
<td>299k</td>
<td>290k</td>
<td>285k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 7</td>
<td>11.3M</td>
<td>11.6M</td>
<td>11.5M</td>
<td>11.3M</td>
<td>11.0M</td>
<td>3.5M</td>
</tr>
<tr>
<td>Capacitor 1</td>
<td>16.4n</td>
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<td>15.9n</td>
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</tr>
<tr>
<td>Capacitor 2</td>
<td>5.35n</td>
<td>4.57n</td>
<td>5.20n</td>
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<td>5.30n</td>
<td>15.3n</td>
</tr>
<tr>
<td>Capacitor 3</td>
<td>39.7n</td>
<td>38.2n</td>
<td>37.8n</td>
<td>36.2n</td>
<td>44.8n</td>
<td>126n</td>
</tr>
</tbody>
</table>

b -- blistered
s -- short

Chapter 3
### Table 3.5. Resistor/Capacitor Values for Trial #2 (Continued).

<table>
<thead>
<tr>
<th>Substrate Number</th>
<th>6 Al₂O₃⁺</th>
<th>7 Al₂O₃⁺</th>
<th>8 Al₂O₃⁺</th>
<th>9 Al₂O₃⁺</th>
<th>10 AlN</th>
<th>11 AlN</th>
<th>12 AlN</th>
<th>Design Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor 1</td>
<td>475k</td>
<td>472k</td>
<td>422k</td>
<td>425k</td>
<td>444k</td>
<td>454k</td>
<td>431k</td>
<td>500k</td>
</tr>
<tr>
<td>Resistor 2</td>
<td>810k</td>
<td>810k</td>
<td>761k</td>
<td>806k</td>
<td>785k</td>
<td>754k</td>
<td>753k</td>
<td>500k</td>
</tr>
<tr>
<td>Resistor 3</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>11.2M</td>
</tr>
<tr>
<td>Resistor 4</td>
<td>72.1k</td>
<td>77.5k</td>
<td>68.2k</td>
<td>63.6k</td>
<td>74.1k</td>
<td>68.2k</td>
<td>80.1k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 5</td>
<td>115k</td>
<td>116k</td>
<td>102k</td>
<td>105k</td>
<td>100k</td>
<td>112k</td>
<td>121k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 6</td>
<td>157k</td>
<td>157k</td>
<td>145k</td>
<td>138</td>
<td>143k</td>
<td>154k</td>
<td>158k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 7</td>
<td>7.74M</td>
<td>7.57M</td>
<td>7.63M</td>
<td>7.56M</td>
<td>7.47M</td>
<td>7.81M</td>
<td>7.91M</td>
<td>3.5M</td>
</tr>
<tr>
<td>Capacitor 1</td>
<td>533p</td>
<td>540p</td>
<td>414p</td>
<td>s</td>
<td>s</td>
<td>476p</td>
<td>s</td>
<td>50.9n</td>
</tr>
<tr>
<td>Capacitor 2</td>
<td>s</td>
<td>160p</td>
<td>126p</td>
<td>148p</td>
<td>118p</td>
<td>136p</td>
<td>181p</td>
<td>15.3n</td>
</tr>
<tr>
<td>Capacitor 3</td>
<td>1.38n</td>
<td>1.35n</td>
<td>s</td>
<td>s</td>
<td>1.03n</td>
<td>s</td>
<td>1.45n</td>
<td>126n</td>
</tr>
</tbody>
</table>

b -- blistered
s -- short

Chapter 3 43
3.4.3. Test Circuit Development -- Trial #3

Three test circuits were developed (2 AlN with underlayer, 1 Al₂O₃ with underlayer). The procedure for the circuit development was as follows:

Substrate Preparation

Ultrasonic Cleaning - 10 minutes in soap & 10 minutes in rinse

Screen Production

<table>
<thead>
<tr>
<th>Layer</th>
<th>Wire Dia. (µm)</th>
<th>Emulsion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric underlayer</td>
<td>325</td>
<td>CDF4 -- 40µm</td>
</tr>
<tr>
<td>Metal 1</td>
<td>325</td>
<td>CDF4 -- 40µm</td>
</tr>
<tr>
<td>Capacitor Dielectric</td>
<td>325</td>
<td>CDF4 -- 40µm</td>
</tr>
<tr>
<td>Metal 2</td>
<td>325</td>
<td>CDF4 -- 40µm</td>
</tr>
<tr>
<td>Resistor</td>
<td>280</td>
<td>CDF4 -- 40µm</td>
</tr>
</tbody>
</table>

Procedure

➤ Print dielectric underlayer on AlN and Al₂O₃ -- ESL D-4907 Lot#: 2514-23
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C
   • Fire -- peak 850°C for 10 to 12 minutes at peak

➤ Print second dielectric underlayer on AlN and Al₂O₃ -- ESL D-4907 Lot#: 2514-23
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C
   • Fire -- peak 850°C for 10 to 12 minutes at peak

➤ Print metal 1 layer on AlN and Al₂O₃ -- ESL D-9912 Lot#: 2530-11
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C

➤ Second print of metal 1 layer on AlN and Al₂O₃ -- ESL D-9912 Lot#: 2530-11
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C
   • Fire -- peak 850°C for 10 to 12 minutes at peak

➤ Print first dielectric layer on AlN and Al₂O₃ -- ESL D-4206 Lot#: 2511-32
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C
   • Fire -- peak 850°C for 10 to 12 minutes at peak
Al₂O₃ metal thickness -- 10µm (fired thickness)
Al₂O₃ metal + dielectric thickness -- 24µm (fired thickness)
AlN metal + dielectric thickness -- 27µm (fired thickness)

➤ Print second dielectric layer on AlN and Al₂O₃ -- ESL D-4206  Lot#: 2511-32
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C

➤ Print third dielectric layer on AlN and Al₂O₃ -- ESL D-4206  Lot#: 2511-32
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C
   • Fire -- peak 850°C for 10 to 12 minutes at peak
     Al₂O₃ metal + dielectric thickness -- 45µm (fired thickness)
     AlN metal + dielectric thickness -- 45µm (fired thickness)

➤ Print second metal layer on AlN and Al₂O₃ -- ESL D-9912  Lot#: 2530-11
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C

➤ Print resistor layer on AlN and Al₂O₃ -- DuPont 1940-D  100KΩ/sq
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C
   • Fire -- peak 850°C for 10 to 12 minutes at peak
### Table 3.6. Resistor/Capacitor Values for Trial #3.

<table>
<thead>
<tr>
<th>Substrate Number</th>
<th>1 AIN</th>
<th>2 AIN</th>
<th>3 Al$_2$O$_3^*$</th>
<th>Design Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor 1</td>
<td>393k</td>
<td>415k</td>
<td>425k</td>
<td>500k</td>
</tr>
<tr>
<td>Resistor 2</td>
<td>730k</td>
<td>740k</td>
<td>764k</td>
<td>500k</td>
</tr>
<tr>
<td>Resistor 3</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>11.2M</td>
</tr>
<tr>
<td>Resistor 4</td>
<td>58.8k</td>
<td>54.7k</td>
<td>49.5k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 5</td>
<td>102k</td>
<td>96.0k</td>
<td>95.8k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 6</td>
<td>144k</td>
<td>145k</td>
<td>142k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 7</td>
<td>7.56M</td>
<td>7.61M</td>
<td>7.73M</td>
<td>3.5M</td>
</tr>
<tr>
<td>Capacitor 1</td>
<td>6.63n</td>
<td>4.67n</td>
<td>4.26n</td>
<td>50.9n</td>
</tr>
<tr>
<td>Capacitor 2</td>
<td>2.74n</td>
<td>2.33n</td>
<td>1.64n</td>
<td>15.3n</td>
</tr>
<tr>
<td>Capacitor 3</td>
<td>8.17n</td>
<td>10.1n</td>
<td>7.60n</td>
<td>126n</td>
</tr>
</tbody>
</table>

b -- blistered  
s -- short
3.4.4. Test Circuit Development -- Trial #4

Three test circuits were developed (2 AlN with underlayer, 1 Al$_2$O$_3$ with underlayer). The procedure for the circuit development was as follows:

**Substrate Preparation**

Ultrasonic Cleaning - 10 minutes in soap & 10 minutes in rinse

**Screen Production**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Mesh Size</th>
<th>Wire Dia.</th>
<th>Emulsion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric underlayer</td>
<td>325</td>
<td>1.1 mil (27.9μm)</td>
<td>CDF4 -- 40μm</td>
</tr>
<tr>
<td>Metal 1</td>
<td>325</td>
<td>1.1 mil (27.9μm)</td>
<td>CDF4 -- 40μm</td>
</tr>
<tr>
<td>Capacitor Dielectric</td>
<td>325</td>
<td>1.1 mil (27.9μm)</td>
<td>CDF4 -- 40μm</td>
</tr>
<tr>
<td>Metal 2</td>
<td>325</td>
<td>1.1 mil (27.9μm)</td>
<td>CDF4 -- 40μm</td>
</tr>
<tr>
<td>Resistor</td>
<td>280</td>
<td>1.2 mil (27.9μm)</td>
<td>CDF4 -- 40μm</td>
</tr>
</tbody>
</table>

**Procedure**

➤ Print dielectric underlayer on AlN and Al$_2$O$_3$ -- ESL D-4907 Lot#: 2514-23
  • Leveling time -- 10 minutes
  • Drying -- 20 minutes @ 125°C

➤ Print second dielectric underlayer on AlN and Al$_2$O$_3$ -- ESL D-4907 Lot#: 2514-23
  • Leveling time -- 10 minutes
  • Drying -- 20 minutes @ 125°C
  • Fire -- peak 850°C for 10 to 12 minutes at peak

➤ Print metal 1 layer on AlN and Al$_2$O$_3$ -- ESL D-9912 Lot#: 2530-11
  • Leveling time -- 10 minutes
  • Drying -- 20 minutes @ 125°C

➤ Second print of metal 1 layer on AlN and Al$_2$O$_3$ -- ESL D-9912 Lot#: 2530-11
  • Leveling time -- 10 minutes
  • Drying -- 20 minutes @ 125°C
  • Fire -- peak 850°C for 10 to 12 minutes at peak

➤ Print first dielectric layer on AlN and Al$_2$O$_3$ -- ESL D-4206 Lot#: 2511-32
  • Leveling time -- 10 minutes
  • Drying -- 20 minutes @ 125°C
  • Fire -- peak 850°C for 10 to 12 minutes at peak
  AlN metal + dielectric thickness -- 35μm (fired thickness)
Print second dielectric layer on AlN and Al₂O₃ -- ESL D-4206 Lot#: 2511-32
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C
Print third dielectric layer on AlN and Al₂O₃ -- ESL D-4206 Lot#: 2511-32
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C
   • Fire -- peak 850°C for 10 to 12 minutes at peak
      AlN metal + dielectric thickness -- 47µm (fired thickness)

Print second metal layer on AlN and Al₂O₃ -- ESL D-9912 Lot#: 2530-11
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C

Print resistor layer on AlN and Al₂O₃ -- DuPont 1940-D 100KΩ/sq
   • Leveling time -- 10 minutes
   • Drying -- 20 minutes @ 125°C
   • Fire -- peak 850°C for 10 to 12 minutes at peak

Table 3.7. Resistor/Capacitor Values for Trial #4.

<table>
<thead>
<tr>
<th>Substrate Number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>Design Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor 1</td>
<td>380k</td>
<td>397k</td>
<td>366k</td>
<td>500k</td>
</tr>
<tr>
<td>Resistor 2</td>
<td>760k</td>
<td>692k</td>
<td>718k</td>
<td>500k</td>
</tr>
<tr>
<td>Resistor 3</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>&gt;20M</td>
<td>11.2M</td>
</tr>
<tr>
<td>Resistor 4</td>
<td>51.7k</td>
<td>48.9k</td>
<td>51.6k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 5</td>
<td>91.5k</td>
<td>88.3k</td>
<td>93.5k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 6</td>
<td>132k</td>
<td>135k</td>
<td>133k</td>
<td>100k</td>
</tr>
<tr>
<td>Resistor 7</td>
<td>7.43M</td>
<td>7.56M</td>
<td>7.46M</td>
<td>3.5M</td>
</tr>
<tr>
<td>Capacitor 1</td>
<td>12.2n</td>
<td>10.5n</td>
<td>9.19n</td>
<td>50.9n</td>
</tr>
<tr>
<td>Capacitor 2</td>
<td>3.62n</td>
<td>3.36n</td>
<td>3.20n</td>
<td>15.3n</td>
</tr>
<tr>
<td>Capacitor 3</td>
<td>35.4n</td>
<td>31.6n</td>
<td>29.9n</td>
<td>126n</td>
</tr>
</tbody>
</table>

b -- blistered
s -- short
3.5. Dielectric Breakdown Experiment

Half the capacitors from the four trials were used in the dielectric breakdown test. Only half the capacitors were used since the test is destructive in nature. This test was conducted by biasing the capacitor in 50 volt increments. The voltage was slowly ramped up in 50 volt increments and held at this value for a minimum of ten seconds. A breakdown was considered to have occurred if a physical short was generated or a momentary arc was generated (a burn spot in the top electrode was usually observed). Voltage breakdown resulted from these measurements ranged from 230V to 450V in these experiments. Table 3.8 illustrates the results of the measurements. The current through the capacitor is shown at each voltage level tested. If breakdown occurred before a 50 volt increment, the value at breakdown is presented.
<table>
<thead>
<tr>
<th>Trial</th>
<th>Substrate</th>
<th>Cap</th>
<th>50V</th>
<th>100V</th>
<th>150V</th>
<th>200V</th>
<th>250V</th>
<th>300V</th>
<th>350V</th>
<th>400V</th>
<th>450V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 -</td>
<td>2 -</td>
<td>1</td>
<td>4.0mA</td>
<td>10mA@90V</td>
<td></td>
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</tr>
<tr>
<td>1 -</td>
<td>2 -</td>
<td>2</td>
<td>0.5mA</td>
<td>1.2mA</td>
<td>B@150V</td>
<td></td>
<td></td>
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<tr>
<td>1 -</td>
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<td>3</td>
<td>9.0mA@50V</td>
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</tr>
<tr>
<td>4 -</td>
<td>3 -</td>
<td>1</td>
<td>3.0mA</td>
<td>8.0mA</td>
<td>10mA@110V</td>
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</tr>
<tr>
<td>4 -</td>
<td>3 -</td>
<td>2</td>
<td>0.5mA</td>
<td>1.2mA</td>
<td>2.5mA</td>
<td>B@170V</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>4 -</td>
<td>3 -</td>
<td>3</td>
<td>10mA@50V</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>4 -</td>
<td>3 -</td>
<td>2</td>
<td>1.5mA</td>
<td>3.8mA</td>
<td>B@150V</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>2 -</td>
<td>2 -</td>
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<td>0.5mA</td>
<td>1.2mA</td>
<td>2.2mA</td>
<td>B@160V</td>
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</tr>
<tr>
<td>2 -</td>
<td>2 -</td>
<td>3</td>
<td>4.5mA</td>
<td>10mA@93V</td>
<td></td>
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</tr>
<tr>
<td>3 -</td>
<td>1 -</td>
<td>1</td>
<td>0.2mA</td>
<td>0.2mA</td>
<td>0.4mA</td>
<td>0.4mA</td>
<td>B@250V</td>
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<td></td>
</tr>
<tr>
<td>3 -</td>
<td>1 -</td>
<td>2</td>
<td>0.1mA</td>
<td>0.2mA</td>
<td>0.3mA</td>
<td>0.4mA</td>
<td>0.6mA</td>
<td>B@260V</td>
<td></td>
<td></td>
<td></td>
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<td>3 -</td>
<td>1 -</td>
<td>3</td>
<td>0.1mA</td>
<td>0.1mA</td>
<td>0.2mA</td>
<td>0.2mA</td>
<td>B@230V</td>
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<td>3 -</td>
<td>1</td>
<td>0.1mA</td>
<td>0.1mA</td>
<td>0.1mA</td>
<td>0.2mA</td>
<td>0.2mA</td>
<td>0.2mA</td>
<td>B@350V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 -</td>
<td>3 -</td>
<td>2</td>
<td>0.1mA</td>
<td>0.1mA</td>
<td>0.1mA</td>
<td>0.2mA</td>
<td>0.2mA</td>
<td>0.2mA</td>
<td>0.2mA</td>
<td>B@450V</td>
<td></td>
</tr>
<tr>
<td>3 -</td>
<td>3 -</td>
<td>3</td>
<td>0.1mA</td>
<td>0.1mA</td>
<td>0.2mA</td>
<td>0.2mA</td>
<td>0.2mA</td>
<td>0.2mA</td>
<td>B@350V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 -</td>
<td>1 -</td>
<td>1</td>
<td>0.8mA</td>
<td>1.6mA</td>
<td>2.8mA</td>
<td>5.2mA</td>
<td>B@250V</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>4 -</td>
<td>1 -</td>
<td>2</td>
<td>0.1mA</td>
<td>0.2mA</td>
<td>0.3mA</td>
<td>0.5mA</td>
<td>B@220V</td>
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</tr>
<tr>
<td>4 -</td>
<td>1 -</td>
<td>3</td>
<td>4.0mA@50v</td>
<td>9.3mA@100V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 -</td>
<td>2 -</td>
<td>1</td>
<td>0.3mA</td>
<td>0.6mA</td>
<td>1.2mA</td>
<td>2.0mA</td>
<td>B@218V</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>4 -</td>
<td>2 -</td>
<td>2</td>
<td>0.1mA</td>
<td>0.2mA</td>
<td>0.3mA</td>
<td>B@196V</td>
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<td>3</td>
<td>2.4mA</td>
<td>6.1mA</td>
<td>10mA@130V</td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

* AlN substrate, no asterisk denotes Al₂O₃
3.6. Thermal Coefficient Experiment

Half the capacitors from the first four trials were used in this Thermal Coefficient of Capacitance (TCC) measurement experiment. Four substrates were attached to a copper heat sink and then placed in an environmental chamber with temperature control. The capacitance was measured over a range of frequencies at six specific temperatures. The results are tabulated below in Table 3.9 through Table 3.13. Two sets of data follow: capacitance variation with frequency (temperature constant) and capacitance variation with temperature (frequency constant).

These measurements were taken using a HP4192a Hewlett-Packard Impedance Analyzer. The substrates were placed in a Sun environmental chamber. The temperature on the chamber was set and the substrates were allowed to reach steady state. The resistors and the capacitors were then measured at specific frequencies. The results at each individual frequency was recorded. Temperature was then incremented and the frequency measurement process was repeated.

In the next section, a computer program was generated using LabView™. This program allowed for many more data points to be calculated and recorded. Since this process was performed electronically, less chance of error is probable. These numerical results are represented graphically in three dimensions. Nonetheless, a numerical results taken manually are presented in the tables below for future reference.

As expected, the capacitance decreases as the frequency increases. This agrees with the paper published by ESL [BLE92], who manufacturers the dielectric paste use in this study. The capacitance also decreases as the frequency increases up to 200kHz. At frequencies above 400kHz, the capacitance begins to increase. These two effects are common to most commercial capacitors and is due to self resonance.
### Table 3.9. Capacitor Thermal Values.

**Thermal Experiment**

values in nF

<table>
<thead>
<tr>
<th>Temperature = 16°C</th>
<th>500Hz</th>
<th>1kHz</th>
<th>5kHz</th>
<th>10kHz</th>
<th>50kHz</th>
<th>100kHz</th>
<th>200kHz</th>
<th>300kHz</th>
<th>400kHz</th>
<th>500kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trial 2 - Substrate 3 - Cap 3</td>
<td>37.98</td>
<td>37.98</td>
<td>33.04</td>
<td>33.04</td>
<td>29.68</td>
<td>29.26</td>
<td>29.25</td>
<td>29.52</td>
<td>29.83</td>
<td>30.14</td>
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* AlN substrate, no asterisk denotes Al₂O₃

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**Chapter 3**

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* AlN substrate, no asterisk denotes Al₂O₃
Table 3.11. Capacitor Thermal Values (Continued).

TCC
values in %

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* AlN substrate, no asterisk denotes Al₂O₃
Table 3.12. Capacitor Thermal Coefficient Values.

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<td>-3</td>
<td>-3.12</td>
<td>-2.98</td>
<td>-2.81</td>
<td>-3.18</td>
<td>-3.23</td>
</tr>
<tr>
<td>Trial 4 - Substrate 2 - Cap 3*</td>
<td>-3.57</td>
<td>-3.06</td>
<td>-2.91</td>
<td>-3.25</td>
<td>-3.88</td>
<td>-3.98</td>
<td>-4.03</td>
<td>-4.13</td>
<td>-4.13</td>
<td>-4.09</td>
</tr>
<tr>
<td><strong>Temperature = 100°C</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Trial 2 - Substrate 3 - Cap 3</td>
<td>-4.96</td>
<td>-4.8</td>
<td>-4.26</td>
<td>-4.21</td>
<td>-4.51</td>
<td>-4.68</td>
<td>-4.84</td>
<td>-4.96</td>
<td>-5.06</td>
<td>-5.16</td>
</tr>
<tr>
<td>Trial 2 - Substrate 4 - Cap 3</td>
<td>-5.05</td>
<td>-4.88</td>
<td>-4.27</td>
<td>-4.15</td>
<td>-4.39</td>
<td>-4.55</td>
<td>-4.66</td>
<td>-4.66</td>
<td>-4.58</td>
<td>-4.44</td>
</tr>
<tr>
<td>Trial 3 - Substrate 2 - Cap 3*</td>
<td>-4.31</td>
<td>-4.12</td>
<td>-3.61</td>
<td>-3.83</td>
<td>-3.91</td>
<td>-4.01</td>
<td>-3.93</td>
<td>-3.84</td>
<td>-4.01</td>
<td>-4.03</td>
</tr>
<tr>
<td>Trial 4 - Substrate 2 - Cap 3*</td>
<td>-4.31</td>
<td>-3.91</td>
<td>-3.59</td>
<td>-3.82</td>
<td>-4.34</td>
<td>-4.47</td>
<td>-4.56</td>
<td>-4.57</td>
<td>-4.55</td>
<td>-4.48</td>
</tr>
<tr>
<td><strong>Temperature = 125°C</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Trial 2 - Substrate 3 - Cap 3</td>
<td>-5.1</td>
<td>-5.01</td>
<td>-4.66</td>
<td>-4.6</td>
<td>-4.76</td>
<td>-4.88</td>
<td>-5.01</td>
<td>-5.1</td>
<td>-5.18</td>
<td>-5.26</td>
</tr>
<tr>
<td>Trial 2 - Substrate 4 - Cap 3</td>
<td>-5.09</td>
<td>-4.98</td>
<td>-4.58</td>
<td>-4.47</td>
<td>-4.57</td>
<td>-4.69</td>
<td>-4.79</td>
<td>-4.82</td>
<td>-4.81</td>
<td>-4.78</td>
</tr>
<tr>
<td>Trial 3 - Substrate 2 - Cap 3*</td>
<td>-4.4</td>
<td>-4.3</td>
<td>-3.98</td>
<td>-4.12</td>
<td>-4.17</td>
<td>-4.23</td>
<td>-4.19</td>
<td>-4.14</td>
<td>-4.26</td>
<td>-4.27</td>
</tr>
<tr>
<td>Trial 4 - Substrate 2 - Cap 3*</td>
<td>-4.78</td>
<td>-4.52</td>
<td>-4.2</td>
<td>-4.31</td>
<td>-4.69</td>
<td>-4.8</td>
<td>-4.89</td>
<td>-4.94</td>
<td>-4.96</td>
<td>-4.96</td>
</tr>
</tbody>
</table>

* AlN substrate
no asterisk denotes Al₂O₃
3.7. Test Results, A Graphical Representation

The second half of the capacitors from the first four trials were used to determine these elements’ behavior as a function of frequency and temperature. The substrates were attached to a copper heat sink and then placed in an environmental chamber with temperature control. The capacitance was measured over a range of frequencies at 17 specific temperatures ranging from -25°C to +130°C.

3.7.1. LabView™ Data Acquisition

LabView™ is an object-oriented programming language specifically developed to interface with laboratory equipment and instrumentation. LabView™ will run on a PC and will interface equipment with a serial port, parallel port, or a General Purpose Interface Bus (GPIB); the equipment under control must also have one of these type of interfaces. The program has a graphical user interface in where blocks, which represent specific programming segments, many be interconnected. Once the desired programming blocks are interconnected, the program runs as a virtual machine. The user interface appears as a set of dials, buttons, meters, graphs, and data input boxes. The interface can even be set up to look similar to the device or instrument under control. Screen shots if the LabView™ interface are in Appendix A. The benefit of this type of program is to allow complete automation of an instrument or a group of instruments. All data is recorded electronically thus reducing the probability of error. This data may be directly imported into a spreadsheet such as Excel. Large amounts data, that previously would have been time prohibitive to collect, can be collected in a relatively short amount of time. Calibration procedures can also be conducted on a large scale.
3.7.2. Impedance Meter Calibration

Calibration is required due to the inherent series resistance and inductance and parallel capacitance and resistance in the test leads of the impedance meter. These parasitics are depicted in Figure 3.7. The data taken using the LabView™ program was imported into Excel. The Excel spreadsheet was then used to extract the component data from the measured data. Calibration open and short probe data is used to eliminate parasitic values from the measurement. The procedure used is as follows:

1. Open circuit the fixture.
2. The open circuit admittance in G-B is measured.
3. A short is formed by holding the probes together.
4. The short circuit impedance, in R-X is measured.
5. The shorted condition is then removed.
6. The probe is now placed across the element to be measured and the impedance in R-X is measured.
7. The compensated measured data (Rx and Xx) is given by the following equations:

$$Rx = \frac{Gm - Go}{(Gm - Go)^2 + (Bm - Bo)^2} - Ro$$

$$Xx = \frac{Bo - Bm}{(Gm - Go)^2 + (Bm - Bo)^2} - Xo$$

Where,

- \(Gm + jBm\) = measured admittance (S).
- \(Ro + jXo\) = residual impedance (Ω) - short circuit impedance.
- \(Go + jBo\) = stray admittance (S) - open circuit admittance.
- \(Rx + jXx\) = actual element impedance (Ω).

Equations 3.2 and 3.3 assume:

$$(Ro + jXo) \ll \frac{1}{Go - jBo}$$

Chapter 3
Figure 3.7. Impedance Meter Parasitics.

For the automated process using LabView™, the open circuit condition may be performed in the measurement taken over wide range frequencies. The same frequency sweep should be performed for the short circuit condition. Once the open and short circuit frequency sweeps have been performed, frequency sweep impedance measurement for the unknown device may be performed. The three sets of data can be brought into a spreadsheet where the above set of equations may be used to repeatedly calculate the calibrated device impedance for each frequency. When a temperature sweep is also involved the same process is repeated at each of the selected temperatures.

To reduce the effects of the parasitics, it is desirable that the element being measured have a large impedance as possible. Since the parasitics are usually small, the higher the impedance of the device under measurement, the smaller percentage of error caused by the parasitics in the test fixture.
3.7.3. Graphical Results Acquisition

The results form the largest test capacitor 9.65mm x 8.64mm (380 mils x 340 mils) are illustrated in Figures 3.8 through 3.12. Figures 3.8 and 3.9 show the impedance and the phase characteristics of these capacitor elements, respectively. The optimum values are obtained around 25°C with increased impedance on either side. As expected, the phase begins to shift toward zero as the frequency increases. This phenomena is due to the parasitic inductance and dipole characteristics of the dielectric paste. These two effects are common to conventional capacitors. These results also agree with previously published work by ESL for this material on Al₂O₃ [BLE92]. For clarity, the capacitance in the test capacitor is plotted in Figure 3.11. In this illustration, it is clear that temperature is more critical than frequency for operation below a frequency of 500kHz.

Figure 3.12 shows the percent change in capacitance values relative to temperature and frequency. Although the large variation over the temperature change is not unusual in power electronic circuits where there are numerous heat dissipative components, placement of these capacitors may be of critical importance where tight tolerance is required. Except at low temperatures, below zero degrees Celsius, the dissipation factor variation remains about one percent (Figure 3.10).

The HP4192a Impedance Analyzer is limited in frequency to 13MHz. At higher frequencies, the test fixture parasitics become large in comparison to impedance of the device being measured. At frequencies above 10MHz special measurement test fixtures may be required. The special fixtures typically cannot withstand extreme environments required in device testing. High frequency measurements were performed using a special probe test fixture and an HP4193
Impedance Analyzer. This meter is capable of measuring impedance up to 110Mhz. Unfortunately, the special test fixture cannot withstand the temperatures subjected to the components in the previous experiments. The high frequency characteristics were obtained, using this piece of equipment, at room temperature. Since the majority of SMPS operate under 2Mhz, this data is useful for showing general trends but is not required for design reasons. Figures 3.13 and 3.14 show the high frequency characteristics for the same capacitor at room temperature. This capacitor shows a self resonance at above 10MHz. This characteristic is better than the typical through hole component and should provide adequate operation for operation up to several megahertz.
Figure 3.8. Effect of frequency and temperature on capacitor impedance.
Figure 3.9. Effect of frequency and temperature on capacitor phase.
Figure 3.10. Effect of frequency and temperature on capacitor dissipation factor. (note reversed axis form above graphs)
Figure 3.11. Effect of frequency and temperature on capacitance.
Figure 3.12. Capacitance change with frequency and temperature.
Figure 3.13. High Frequency Characteristics of Thick Film Capacitor on AlN (25°C). 
Magnitude and Phase
Figure 3.14. High Frequency Characteristics of Thick Film Capacitor on AlN (25°C). Magnitude and Equivalent Series Resistance
3.8. Conclusions

Several process trials were conducted in order to obtain functional thick film components on AlN, but to also to optimize the passives for high voltage circuits. Variations in the number of layers that were cofired, and the number of dielectric layers were varied in order to achieve functional components. It was also determined that even though blistering did occur on several trials, that sometimes the blistering was just cosmetic and functional passives resulted.

The third trial achieved non-blistered functional capacitors on AlN with the highest breakdown voltage (at the expense of increased capacitance per area). It was also found that these capacitors achieved the least change due to frequency and temperature variations.

For the third trial, screens for each layer were prepared as listed in Table 3.14. The procedure for the thick film processing is summarized in Table 3.15. Printer squeegee pressure and speed, and screen snapoff distance assumed typical values. Leveling times were held to 10 minutes since smooth layers were desired over fine line resolution. Drying times were 20 minutes at 125°C. Firing used a belt furnace with a standard 50 minute profile, as used with Al₂O₃, with a peak temperature of 850°C, which was maintained for 10 minutes.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Mesh Size</th>
<th>Wire Dia.</th>
<th>Emulsion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passivation</td>
<td>325@ 90°</td>
<td>1.1 mil</td>
<td>40mm</td>
</tr>
<tr>
<td>Metal 1</td>
<td>325@ 90°</td>
<td>1.1 mil</td>
<td>40mm</td>
</tr>
<tr>
<td>Dielectric</td>
<td>325@ 90°</td>
<td>1.1 mil</td>
<td>40mm</td>
</tr>
<tr>
<td>Metal 2</td>
<td>325@ 90°</td>
<td>1.1 mil</td>
<td>40mm</td>
</tr>
<tr>
<td>Resistor</td>
<td>280@ 90°</td>
<td>1.2 mil</td>
<td>40mm</td>
</tr>
</tbody>
</table>
The capacitor characteristics developed are electrically comparable to X7R type multilayer ceramic capacitors. This is most likely due to the composition of the capacitor dielectric material. It is theorized from these results that the ESL capacitor dielectric material consists mainly of Barium Titanate. This material is optimized for room temperature and the dielectric constant varies greatly with temperature. Similar results were seen in the research work presented in this chapter.
4. Resistors

Chapter 4 will discuss information on thick film resistors, intended for use with switch mode power supplies, on aluminum oxide and aluminum nitride. While the processing steps necessary to generate these resistors on aluminum nitride are discussed in Chapter 3, both electrical and thermal characterization are reported in this chapter. An impedance analyzer is used to characterize the resistors from 10Hz up to 1MHz. The thermal characteristics and properties are measured for the passivated aluminum nitride using a Barnes thermal imaging unit. This chapter will discuss the experiment setup and results. The resulting thermal plots generated from these experiments are used to calculate the thermal conductivity of the passivated aluminum nitride.

4.1. Test Array

As discussed in Chapter 3, to determine the characteristics of the thick film pastes on AlN, an array of resistors was printed on both Al₂O₃ and on AlN with a passivation layer and on Al₂O₃ without a passivation layer. Eight separate resistor geometries were created on the test coupon. Table 4.1 shows the geometries for the test coupon. The resistor value may be calculated by:

$$R = \frac{L \rho_s}{W}$$  \hspace{1cm} (4.1)

Where,

- \(R\) = resistance.
- \(L\) = resistor length.
- \(W\) = resistor width.
- \(\rho_s\) = sheet resistivity of thick film paste.
Resistor pastes are available in sheet resistivities ranging from 10Ω/sq. to 1MegΩ/sq, typically in factors of 10 (i.e., 10Ω/sq., 100Ω/sq., 1000Ω/sq. ...). Proportional mixing of pastes allows for sheet resistivities in intermediary ranges. A resistor may be formed by using a paste with the closest sheet resistivity to the desired element value and then the geometry may be adjusted to obtain the exact value within tolerance.

<table>
<thead>
<tr>
<th>Element</th>
<th>Geometry (L x W)</th>
<th>Element</th>
<th>Geometry (W x L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>25 mils x 5 mils</td>
<td>R6</td>
<td>80 mils x 80 mils</td>
</tr>
<tr>
<td>R1</td>
<td>50 mils x 10 mils</td>
<td>R7</td>
<td>700 mils x 20 mils</td>
</tr>
<tr>
<td>R2</td>
<td>100 mils x 20 mils</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>1120 mils x 10 mils</td>
<td>C1</td>
<td>260 mils x 200 mils</td>
</tr>
<tr>
<td>R4</td>
<td>20 mils x 20 mils</td>
<td>C2</td>
<td>260 mils x 60 mils</td>
</tr>
<tr>
<td>R5</td>
<td>40 mils x 40 mils</td>
<td>C3</td>
<td>380 mils x 340 mils</td>
</tr>
</tbody>
</table>

A small resistor configuration, R0, was chosen to test screen printing resolution. The longer meander pattern resistors, R3 and R7, were developed to test large resistor values while also measuring the parasitic effects caused by these patterns. The three resistors R4, R5 and R6, have the same length and width and are used to test power dissipation effects. The power rating of a thick film resistor ($P_d$) may be determined by:

$$P_d = W \times L \times P_r$$

(4.2)

Where, $P_r$ is the rated power dissipation in watts/area$^2$ and is substrate dependent. For alumina 100Watts/in$^2$ is commonly used. $P_r$ is usually derated by a factor of 1.25 to 1.5 (80Watts/in$^2$ to 50Watts/in$^2$). In final circuit processing, the thick film resistor may be accurately cut to improve
tolerance, effectively reducing its width while increasing its impedance. The Pr value may be further reduced to account for resistor this trimming.

The remaining resistors, R1 and R2, have a 5:1, length to width ratio. From a design standpoint, this is the largest length to width ratio that will achieve resistor values with close, design to manufacture, tolerance. As this ratio increases, thickness of the resistor becomes nonuniform. Thickness variations in the printing process will effect the overall fired thickness; therefore, tight tolerance will be compromised. These resistors were used to test print variations on resistor tolerance.

4.2. Resistor Electrical Characterization

The impedance measurements were taken using an HP4192a Impedance Analyzer. The system was calibrated has explained in Chapter 3 and once again the data was acquired electronically using a program generated in LabView™. Frequency measurements were conducted on the resistors at room temperature. There was a negligible amount of variation in impedance and phase values in the range from DC up to 1MHz, and essentially the behavior of these elements was found to be ideal over this range.

Figure 4.1 and Figure 4.2 show impedance measurements for two resistors. The first figure shows resistor R6 from substrate No. 2 generated in the third trial. The second figure shows resistor R6 from substrate No. 2 generated in the fourth trial. In both trials, R6 has a 1:1 length to width ratio. Since a 100kΩ/sq paste was used in Trial 3 and 4, this 1:1 ratio should yield 100kΩ resistors.
Although resistive pastes are specifically made for AlN, it was found that by applying the passivation layer, of low K dielectric, the DuPont 1900 resistor series made for Al$_2$O$_3$ could be successfully printed on AlN surface. The incorporation of this series allowed the use of a high resistance paste on the order of 100k$\Omega$/sq..

Figures 4.1 and 4.2 show that the resistors have constant impedance up to 1MHz. The phase change is slight, under 10%. The integrated resistors do not have the large lead inductance of through hole components. At high frequencies the lead inductance and component parasitic capacitance will have an impedance large enough to cause the component to self resonate. The integral components have very short leads; therefore, self resonance will occur at a much higher frequency. This characteristic will become very desirable for SMPS operating at higher frequencies. The other resistors were measured and also found to have constant impedance up to 1MHz.
Figure 4.1. Resistor Impedance Characteristics as a Function of Frequency. Trial 3, Substrate 2, Resistor 6.
Figure 4.2. Resistor Impedance Characteristics as a Function of Frequency.
Trial 4, Substrate 2, Resistor 6.
4.3. Thermal Measurement

A series of thermal measurements were conducted on the test coupon using a Barnes thermal imaging system. The next three sections explain the thermal unit, the test setup, and the results.

4.3.1. Thermal Imager

The instrumentation used for the thermal measurements was a Barnes CompuTherm™ RM-50 system. This system consists of an infrared microimager, precision heated substage, PC computer, color printer, and CompuTherm™ software. This system will optically acquire a radianc scan and generate thermal analysis displays with a resolution of 16 microns and a temperature resolution of 0.1 degrees centigrade. The thermal maps that are generated are corrected for emissivity [BAR87]. The acquired thermal scans may be either stored to disk or printed on the color printer.

The first step in the measurement process is to optically scan the desired circuit, unpowered, at two known temperatures. The isothermal precision heated substage provides the means to perform this step. The circuit is heated to its first calibration temperature, typically around 40 degrees centigrade and a reference radianc scan is taken. The circuit is then heated to its second calibration temperature, typically around 90 degrees centigrade, and a second reference radianc scan is taken. From these two reference calibration scans, the CompuTherm™ software will compute the emissivity of the circuit. Emissivity correction is critical in thermal scans in order to provide accurate temperature maps.
The emissivity of an object is related to the radiance of the object. The radiance ($\mathcal{R}$) of an object is defined as the rate per unit surface area at which energy is radiated. In relation to the surface temperature of an object:

$$\mathcal{R} = e\sigma T^4 \quad (4.3)$$

Where,

- $\mathcal{R}$ = radiance (W/m$^2$).
- $e$ = emissivity.
- $\sigma$ = Stefan-Boltzmann constant ($5.67 \times 10^{-8}$ W/m$^2$K$^4$).
- $T$ = surface temperature (K).

The emissivity of a material is always between zero and one. A perfect black body would have an emissivity of one and a perfectly reflective body would have an emissivity of zero. Because an object such as a circuit will have numerous objects on its surface, all with different emissivities, to acquire an accurate temperature scan from a radiance scan, the emissivities must be known.

Many thermal imaging systems cannot perform a calibration scan and the use of emissivity dots are required. Emissivity dots are small black paper circles that are attached using adhesive to the components to be measured. The black dots have a known emissivity; therefore, the temperature of the dots can be calculated with one radiance scan. One problem with the emissivity dots is that the dots themselves are not perfect thermal conductors. The temperature of the dot and the surface being measured may be slightly different, but this error is typically small. The bigger disadvantage is that only the temperature of the dots can be calculated. In microelectronic circuits, there may be components which dots cannot be attached, such as bare die.
Another method used commonly is to apply a thermally conductive black paint. Once again, the emissivity of the paint is known and only one radiance scan is required. The benefit of the paint method is that the entire circuit temperature can be observed from the scan and not just small areas within the dots. The problem with the paint method is that the paint can affect the overall thermal conductivity of the device being measured, as a result, some accuracy may be compromised. The Barnes imaging system performs two reference scans in order to calculate emissivity. This allows the entire surface to be thermally mapped without the use of emissivity correcting paints.

Once the emissivity has been calculated, the isothermal unit is set to the desired test temperature and the circuit is then powered. A radiance scan is then acquired. From this radiance scan and the previously generated emissivity scan, a temperature analysis and display is calculated. The temperature scan is represented with 16 colors. Each color represents a temperature range that is user selectable from 0.1 degrees centigrade to 12.5 degrees centigrade. The computer display may be used to target specific area of the scan for numerical representation. Four cursors are available to target specific areas. These cursors may also be used to box an area of interest. The program will calculate the maximum, minimum, and average temperatures for the boxed area.

4.3.2. Experimental Procedure

This section discusses the experimental procedure performed on the test coupon based on alumina without a passivation layer and in the test coupon on the passivated aluminum nitride. The steps and methods described below apply to both coupons.

The last section explained the Barnes thermal unit used in these experiments. Figure 4.3 shows a rendering of the thermal apparatus setup. The Barnes thermal unit was equipped with a
6.35 mm field of view lens. This translates to a 0.15 mm spatial resolution of the scanned image. The isothermal unit is a bipolar temperature controller made by Electronic Connector Division. This unit allows the circuit to either be thermoelectrically heated or cold to a constant temperature.

Figure 4.3. Thermal Imager Experimental Setup. From left to right: DC power supply, thermoelectric cooler/heater control, thermocouple meter, Barnes thermal imager, PC computer

The test coupon was mounted onto the isothermal stage using a thermal grease on the back side of the substrate and pressure clamps. It is estimated that a 0.2mm to 0.3mm layer of thermal grease resided between the isothermal stage and the ceramic substrate. A K type thermal couple was also attached to the isothermal stage in the same manner. An Omega thermocouple meter was used to read the temperature readings from the thermal couple.

The Barnes unit must be supplied with liquid nitrogen before power is applied to the unit. The thermal head could be severely damaged if the imager is powered before applying the liquid nitrogen. Both the imager and controlling PC are then turned on and adjusted for a radiance scan. Two lenses are mounted on the Barnes unit, one lens is used for acquiring radiance scans, while
the other allows the user to center the test object in the imagers field of view and bring it into focus. The circuit height must be adjusted to bring into focus.

The first reference temperature was set at 40 degrees centigrade and the entire circuit was given enough time to reach steady state. The temperature of the isothermal unit was checked against the reading of the thermocouple. At steady state, the first reference scan was performed on the unpowered test coupon and then electronically stored. The isothermal unit was then set to 90 degrees centigrade and the circuit was allowed to reach thermal steady state. Again the reference scan was acquired from the unpowered test coupon and stored. From the two reference scans, CompuTherm\textsuperscript{TM} calculated the emissivity for the test coupon.

The radiance scan 40 degrees Centigrade is then used as a reference temperature scan. Along with the emissivity correction and this radiance reference scan, CompuTherm\textsuperscript{TM} sets the reference temperature. This procedure allows CompuTherm\textsuperscript{TM} to produce temperature plots for the powered test coupon. The heating stage then can be set to the desired operating temperature.

The power is then applied to the resistor of interest on the test coupon. The DC power supply, voltage meter, and current meter are used to determine the amount power dissipated in the resistor. When desired power is reached, the test coupon is allowed to reach thermal steady state. The radiance scan is acquired. This radiance scan can then be converted to a temperature plot.

### 4.3.3. Experimental Results

A 10Ω/sq. DuPont 1900 series paste was used to evaluate the thermal management issue. A low resistance paste was used in order that relatively low voltages were required for thermal
power dissipation measurements. R5, a 1.02mm x 1.02mm (40mils x 40mils) 10Ω resistor was thermally mapped for various power levels ranging from ¼ watt to 8 watts. The maps were acquired on a Barnes Infrared Micro Imager. The substrate was placed on an isothermal heater set at 25°C.

The emissivity plots of the Al₂O₃ and AlN test coupons are shown in Figures 4.4 and 4.5, respectively. The plots are displayed in 16 colors, with each color representing a 1/16 increment in emissivity; Zero on the bottom in dark gray and one represented at the top in white. In both figures, the resistor is centered within the plot and has a relatively high emissivity. The large metal pad is located on the right and has a relatively low emissivity which is due to its reflective nature. The metal traces, on either end of the resistor, are clearly seen; they are dark gray in nature and look like square brackets around resistor. The surrounding substrate area for the Al₂O₃ has a lower emissivity than for the AlN due to the passivation layer on the aluminum nitride.

Figures 4.6 through 4.18 show the thermal maps taken with the Barnes thermal imager and calculated with the CompuTherm™ software. The thermal maps show resistor R5 on alumina and aluminum nitride for several different power levels. The aluminum nitride was tested at: 0.25 watts, 0.50 watts, 1.0 watts, 1.5 watts, 2.0 watts, 3.0 watts, and 5.1 watts. The alumina was tested at: 0.25 watts, 0.50 watts, 1.0 watts, 1.5 watts, 2.0 watts, and 3.1 watts. Comparing Figures 4.10 and 4.17, the same resistor thermal map for 2 watts dissipation of the resistor on Al₂O₃ and AlN with passivation layer, even with the passivation layer, the improved characteristics of AlN are clearly illustrated.

At 2 watts, the average center temperature for the resistor based on Al₂O₃ is 115°C. A large amount of heat spreading can be seen surrounding the resistor. In contrast, the resistor produced on AlN with a passivation layer that has an average center temperature of 65°C with
little spreading across the substrate. More generalized hot spots can be seen on the AlN resistor due to thickness variations of the resistor paste. These variations can be attributed to surface roughness of the passivation layer.
Figure 4.4. Emissivity measurement of thick film resistor on $\text{Al}_2\text{O}_3$. 

<table>
<thead>
<tr>
<th>Emissivity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.938 - 1.000</td>
<td></td>
</tr>
<tr>
<td>0.875 - 0.938</td>
<td></td>
</tr>
<tr>
<td>0.813 - 0.875</td>
<td></td>
</tr>
<tr>
<td>0.750 - 0.813</td>
<td></td>
</tr>
<tr>
<td>0.688 - 0.750</td>
<td></td>
</tr>
<tr>
<td>0.625 - 0.688</td>
<td></td>
</tr>
<tr>
<td>0.563 - 0.625</td>
<td></td>
</tr>
<tr>
<td>0.500 - 0.563</td>
<td></td>
</tr>
<tr>
<td>0.438 - 0.500</td>
<td></td>
</tr>
<tr>
<td>0.375 - 0.438</td>
<td></td>
</tr>
<tr>
<td>0.313 - 0.375</td>
<td></td>
</tr>
<tr>
<td>0.250 - 0.313</td>
<td></td>
</tr>
<tr>
<td>0.188 - 0.250</td>
<td></td>
</tr>
<tr>
<td>0.125 - 0.188</td>
<td></td>
</tr>
<tr>
<td>0.063 - 0.125</td>
<td></td>
</tr>
<tr>
<td>0.000 - 0.063</td>
<td></td>
</tr>
</tbody>
</table>
Figure 4.5. Emissivity measurement of thick film resistor on AlN with passivation layer.
Figure 4.6. Thermal measurement of thick film resistor on AlN with passivation layer. (0.25 watts dissipation)
Figure 4.7. Thermal measurement of thick film resistor on AlN with passivation layer.
(0.50 watts dissipation)
Figure 4.8. Thermal measurement of thick film resistor on AlN with passivation layer.
(1.0 watts dissipation)
Figure 4.9. Thermal measurement of thick film resistor on AlN with passivation layer.
(1.5 watts dissipation)
Figure 4.10. Thermal measurement of thick film resistor on AlN with passivation layer.
(2.0 watts dissipation)
Figure 4.11. Thermal measurement of thick film resistor on AlN with passivation layer.
(3.0 watts dissipation)
Figure 4.12. Thermal measurement of thick film resistor on AlN with passivation layer.
(5.1 watts dissipation)
Figure 4.13. Thermal measurement of thick film resistor on Al$_2$O$_3$.
(0.25 watts dissipation)
Figure 4.14. Thermal measurement of thick film resistor on $\text{Al}_2\text{O}_3$.
(0.50 watts dissipation)
Figure 4.15. Thermal measurement of thick film resistor on Al₂O₃.
(1.0 watts dissipation)
Figure 4.16. Thermal measurement of thick film resistor on $\text{Al}_2\text{O}_3$.
(1.5 watts dissipation)
Figure 4.17. Thermal measurement of thick film resistor on Al₂O₃.
(2.0 watts dissipation)
Figure 4.18. Thermal measurement of thick film resistor on Al₂O₃.
(3.1 watts dissipation)
4.4. Thermal Conductivity

It was demonstrated in the last section that AlN has an undecided thermal conduction advantage, even with the passivation. This section will demonstrate how much. Due to the high thermal conductivity of the substrate and the isothermal stage mounted to the under side of the substrate, conduction can be assumed to be much larger than convection. By using a two dimensional thermal model and assuming that the material is thermally isotropic, the thermal conductivity can be calculated from the thermal maps. This will determine the thermal conductivity of the AlN and passivation layer combined. While the properties of AlN are known, this research will quantify the thermal degradation caused by the passivation layer.

The thermal model used is shown in Figure 4.19. The thermal heat source is the resistor on the top surface. The voltage and current in the resistor are known; therefore, the power dissipated is also known. The heat generated by the resistor flows down into the ceramic. As the heat propagates down through each layer it will spread. An explanation of how this heat flow can be computed by a Fourier analysis can be found in [NGU96].

![Figure 4.19. Thermal Spreading Structure.](image)

The heat flow in a material is the thermal conductivity of the material multiplied by the area times the temperature gradient. This is represented as:
\[ Q = \frac{kA}{t} \Delta T \]  \hspace{1cm} (4.4)

Where,

- \( Q \) = amount of heat or power dissipated (watt).
- \( t \) = thickness of material (m).
- \( A \) = surface area (m\(^2\)).
- \( k \) = thermal conductivity (W/mK).
- \( \Delta T \) = temperature difference (K).

The thermal resistance of a material can be expressed as:

\[ \theta = \frac{\Delta T}{Q} = \frac{t}{kA} \]  \hspace{1cm} (4.5)

and has the units of (Kelvin/W). Many times the thermal model is compared to an electrical model. In such a case, current is equivalent to heat flow (\( I \equiv Q \)), temperature is equivalent to voltage (\( \Delta T \equiv V \)), and resistance is equivalent to thermal resistance (\( \theta \equiv R \)). Now using Ohm’s law, \( V = I \ast R \), or \( R = V / I \), we get an equivalent to Equation 4.5. When multiple materials are used, the thermal resistances add. For the total thermal resistance (\( \theta_{total} \)) of \( n \) number of material layers:

\[ \theta_{total} = \sum_{i=1}^{n} \theta_i \]  \hspace{1cm} (4.6)
The thermal structure for the alumina substrate is shown in Figure 4.20 and the equivalent thermal resistance model is shown in Figure 4.21. The structure and resistance model for AlN is shown in Figures 4.22 and 4.23, respectively.

**Figure 4.20. Thermal Structure on Al$_2$O$_3$.**

**Figure 4.21. Thermal Resistance Model for R5 on Al$_2$O$_3$.**
For the alumina case, it is assumed that the resistor evenly dissipates power supplied to it. Or in other words, there is a power source of known value applied to the top of the alumina. There are then two thermal resistances, $\theta_1$ and $\theta_2$. The subscript 1 refers to the ceramic layer and the subscript 2 refers to the thermal grease layer. Solving for the total thermal resistance in the structure:
\[ \theta_{\text{total}} = \theta_1 + \theta_2 \]  

(4.7)

Plugging in Equation 4.5 into Equation 4.7,

\[ \theta_{\text{total}} = \frac{t_1}{k_1A_1} + \frac{t_2}{k_2A_2} \]  

(4.8)

Substituting in the dimensions for the area of dissipation,

\[ \theta_{\text{total}} = \frac{t_1}{k_1(l_1 \times w_1)} + \frac{t_2}{k_2(l_2 \times w_2)} \]  

(4.9)

In Equation 4.9, \( l_i \) and \( w_i \) are the length and width of the equivalent heat source on the top surface of each material due to the heat spread in each material.

The heat flow through a material is defined by the temperature on either side of the material, divided by the thermal resistance of the material. For the alumina, thermal grease structure, the temperature on the top (\( T_2 \)) and bottom surfaces (\( T_1 \)) are known. where,

\[ Q = \frac{\Delta T_{\text{total}}}{\theta_{\text{total}}} = \frac{T_2 - T_1}{T_2 - T_1} \]  

(4.10)

plugging in Equation 4.10 into Equation 4.9,

\[ \frac{T_2 - T_1}{Q} = \frac{t_1}{k_1(l_1 \times w_1)} + \frac{t_2}{k_2(l_2 \times w_2)} \]  

(4.11)
Since the dimension of the resistor is known and the average temperature for the resistor is known, then \( l_2 \) and \( w_2 \) for the second layer (thermal grease) can be calculated. The thickness and thermal conductivity of the thermal grease is known. The thermal conductivity of the alumina \( (k_1) \) can be calculated by solving Equation 4.11 for the thermal conductivity of alumina \( (k_1) \),

\[
k_1 = \frac{t_1}{\left( \frac{T_2 - T_1}{Q} - \frac{t_2}{l_2 \times w_2 \times k_2} \right) (l_1 \times w_1)} \tag{4.12}
\]

\( l_2 \) and \( w_2 \) can be calculated using the spreading angle. Commonly the spreading angle \( (\alpha) \) is taken to be 45 degrees. In reality the spreading angle changes from material to material depending if the heat is flowing from a highly thermally conductive material to a lower thermally conductive material or visa versa. For heat flowing from a high thermally conductive material to a material of lower thermal conductivity, the spreading angle will be larger than 45 degrees. The spreading angle will be less than 45 degrees for heat flowing from a low thermally conductive material to a higher thermally conductive material. If the materials are of the same thermal conductivity, then the angel will be exactly 45 degrees. The spreading angle from one material to the next is found to be [NGU96]:

\[
a = \arctan \frac{k_1}{k_2} = \arctan \frac{(l_2 - l_1)/2}{t} \tag{4.13}
\]
Rearranging, solving for $l_2$,

$$l_2 = l_1 + 2t_1 \tan(a)$$  \hspace{1cm} (4.14)

Likewise for the width, assuming isothermal materials, the heat spread will be the same in all directions. As a result,

$$w_2 = w_1 + 2t_1 \tan(a)$$  \hspace{1cm} (4.15)

From Equation 4.12, 4.14 and 4.15,

$$k_1 = \frac{t_1}{\left( \frac{T_2 - T_1}{Q} - \frac{t_2}{(l_1 + 2t_1) \times (w_1 + 2t_1) \times k_2} \right) (l_1 \times w_1)}$$  \hspace{1cm} (4.16)

Knowing the other parameters, this equation can be solved for $k_1$, the thermal conductivity of alumina. The test circuit parameters shown in Table 4.2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_1$</td>
<td>25 mils</td>
<td>thickness of substrate</td>
</tr>
<tr>
<td>$t_2$</td>
<td>4 mils</td>
<td>thickness of thermal grease</td>
</tr>
<tr>
<td>$k_2$</td>
<td>2.13 w/mK</td>
<td>thermal conductivity of thermal grease</td>
</tr>
<tr>
<td>$l_1$</td>
<td>40 mils</td>
<td>length of resistor</td>
</tr>
<tr>
<td>$w_1$</td>
<td>40 mils</td>
<td>width of resistor</td>
</tr>
<tr>
<td>T1</td>
<td>25 deg. C</td>
<td>temperature of isothermal cooler</td>
</tr>
<tr>
<td>T2</td>
<td>variable</td>
<td>temperature of resistor</td>
</tr>
<tr>
<td>Q</td>
<td>variable</td>
<td>power dissipated in resistor</td>
</tr>
</tbody>
</table>

Table 4.2 Thermal Experiment Parameters.
The same procedure may be carried out to determine the thermal conductivity of the AlN and passivation layer combination. The results of these calculations are shown in Table 4.3. The data shows that the thermal conductivity is two to three times better for AlN with passivation as compared to alumina.

**Table 4.3 Calculated Alumina and Passivated AlN Thermal Properties.**

<table>
<thead>
<tr>
<th>Material</th>
<th>Power (Watts)</th>
<th>Average Resistor Temperature (°C)</th>
<th>Calculated Thermal Conductivity (W/m°C)</th>
<th>Calculated Thermal Conductivity (W/in°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al₂O₃</td>
<td>0.25</td>
<td>33.33</td>
<td>25.13</td>
<td>0.63</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>0.50</td>
<td>41.67</td>
<td>25.06</td>
<td>0.63</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>1.00</td>
<td>60.83</td>
<td>25.94</td>
<td>0.65</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>1.50</td>
<td>83.33</td>
<td>21.23</td>
<td>0.53</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>3.00</td>
<td>154.58</td>
<td>18.56</td>
<td>0.47</td>
</tr>
<tr>
<td>AlN⁺</td>
<td>0.50</td>
<td>35.00</td>
<td>56.58</td>
<td>1.44</td>
</tr>
<tr>
<td>AlN⁺</td>
<td>1.00</td>
<td>45.00</td>
<td>59.78</td>
<td>1.52</td>
</tr>
<tr>
<td>AlN⁺</td>
<td>1.50</td>
<td>54.17</td>
<td>61.78</td>
<td>1.57</td>
</tr>
<tr>
<td>AlN⁺</td>
<td>3.00</td>
<td>83.83</td>
<td>59.48</td>
<td>1.51</td>
</tr>
<tr>
<td>AlN⁺</td>
<td>5.10</td>
<td>125.00</td>
<td>59.13</td>
<td>1.50</td>
</tr>
</tbody>
</table>

* passivation layer

**4.5. Conclusions**

Thick film resistors were successfully developed for use on aluminum nitride. The process steps for the formation of the resistors was discussed in Chapter 3, while the characterization of the resistors and the thermal properties were developed in Chapter 4. The research found that the resistors were nearly ideal over the frequency range of 10 Hz to 1 MHz. Small lead inductance reduces the parasitics which in turn increases the self resonant frequency.

Using the resistors, the thermal properties of the AlN with passivation layer were compared to the thermal properties of Al₂O₃. A 40 mil by 40 mil resistor was powered to several different power levels. Thermal maps were generated for the resistor at each power level. From
these thermal maps, the thermal conductivity of the substrate material was determined. Because
the passivation layer degrades the thermal properties of AlN, the research quantified the relation.

It was determined that the passivated AlN had a thermal advantage over Al₂O₃ of two to
three times. This can make a significant difference when a circuit is designed for Al₂O₃ and is
operating at an unacceptable heat level. The thick film processes generated in this research can be
applied to the design. A two to three times thermal advantage can mean the difference between a
functional and nonfunctional design. Passivation does not have to be applied to the entire surface.
Heat generating components can also be directly coupled to the substrate, thus gaining a thermal
advantage of up to seven times that of Al₂O₃.
5. Electrostatic Discharge of Thick Film Components

Electrostatic Discharge (ESD) tests have been conducted on both thick film resistors and thick film capacitors on Al\textsubscript{2}O\textsubscript{3}. The devices were characterized before the ESD test by measuring the impedance over a range of frequencies. The ESD test was then conducted and the devices measured again. The ESD test that was conducted was based on MIL-STD-833. Figure 5.1 shows the test setup. The device was attached and ten high voltage pulses were applied to each device. The measurements taken before and after the electrostatic discharge are compared to determine if any damage has occurred.

The results of these tests are shown in Figures 5.2 through 5.10. It has been determined that the ESD had little effect on these devices: a 0.1%-0.2% change was typical over most of the frequency range for the resistors and less then a 1% change for the capacitors.

The resistors tested were from a set of substrates on Al\textsubscript{2}O\textsubscript{3}. The resistor was in its untrimmed state. The deviation from ideal at higher frequencies is due to the trace parasitics of the layout. These deviations at higher frequencies can also be attributed to probe placement. The exact placement of the measurement probe in the impedance measurements is difficult; as a result, the higher frequency measurements may differ by a small amount.

The capacitors tested were from the set of original test circuits on Al\textsubscript{2}O\textsubscript{3}. Capacitor 1 from the test array was used for these tests.
Figure 5.1. ESD Test Setup.
Figure 5.2. Resistor 22, Substrate 1 ESD Measurements.
Figure 5.3. Resistor 22, Substrate 2 ESD Measurements.
Figure 5.4. Resistor 22, Substrate 3 ESD Measurements.
Figure 5.5. Resistor 22, Substrate 4 ESD Measurements.
Figure 5.6. Resistor Percent Change ESD Measurements.
Figure 5.7. Capacitor 1, Substrate 7 ESD Measurements.
Figure 5.8. Capacitor 1, Substrate 8 ESD Measurements.
Figure 5.9. Capacitor 1, Substrate 9 ESD Measurements.
Figure 5.10. Capacitor Percent Change ESD Measurements.
6. Inductors and Transformers

This chapter will cover the research that was conducted on miniaturization of inductors and transformers. Three approaches were attempted. The first, method discusses the fabrication of an inductor using a prefired ceramic and plating techniques to form spiral inductors, the second method investigates thick film ferrite pastes. The third method investigates planar magnetics using LTCC and an attached ferrite core.

6.1. Planar Inductor Fabrication

The original intention of this research was to use a 4x4 in$^2$, 40mil thick Al$_2$O$_3$ substrate with 7 individual inductor configurations and 78 interconnecting vias. Vias would be drilled with a diamond tip bit and then thick film metallization applied using standard screen printing techniques. A porous vacuum chuck would be used during printing if the thick film paste did not adequately fill the vias.

It was during the via milling process that it was determined that smaller substrates would have to be used. The diamond drill bits would quickly dull while milling the abrasive Al$_2$O$_3$ surface. Once the bit became dull, the chance of cracking the ceramic increased exponentially. The bits varied widely in the ability to withstand degradation under milling. It was found that 2 to 10 vias could be milled with one bit, but any particular bit could fail at any time thus potentially fracturing the ceramic. This would render the entire substrate unusable.

A smaller substrate was used, 2x2 in$^2$, to improve yield. It would be better to lose one quarter of the design with twenty vias then lose a 4x4 in$^2$ substrate while milling the last hole.
A method of plating, masking and etching was chosen for low cost prototyping. A trial and error method was implemented to achieve the best results for this particular application.

Several methods of plating, masking, and etching were attempted. The methods below were inadequate because the photoresist could not adequately protect the vias from etching. The vias were designed almost as large as the indicator traces and this did not allow for good adhesion for the photoresist in these areas. Also, the predrilling of the vias needed for plated through holes did not allow for even coating of liquid photoresist. A brief explanation of each method and the results are given below. Table 6.1. shows the outcome of the two techniques plus the results of some less preferred techniques that were attempted in order to achieve the desired results.

6.1.1. Method One

1. Drill vias in substrate
2. Plate substrate with copper.
3. Apply, expose, and develop laminate photoresist.
4. Etch substrate.

**Method One Problem**

Potoresist laminate would wash away from vias leaving partially etched vias. One solution would be smaller vias.

6.1.2. Method Two

1. Drill vias in substrate
2. Plate substrate with copper.
3. Apply, expose, and develop liquid photoresist.
4. Etch substrate.

**Method Two Problem**

Liquid potoresist would not spin coat evenly. The predrilled vias would cause a meniscus to form around each via causing nonuniform coating. This nonuniformity would not expose and develop properly.
Table 6.1. Summary of Plate, Mask and Etch Techniques.

<table>
<thead>
<tr>
<th>Method</th>
<th>Side 1</th>
<th>Side 2</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>liquid</td>
<td>liquid</td>
<td>vias cause uneven coating.</td>
</tr>
<tr>
<td>2</td>
<td>liquid</td>
<td>tape</td>
<td>soft bake reacts with tape, vias disrupt resist.</td>
</tr>
<tr>
<td>3</td>
<td>liquid</td>
<td>fully exposed laminate</td>
<td>laminate can’t take softbake.</td>
</tr>
<tr>
<td>4</td>
<td>laminate</td>
<td>laminate</td>
<td>holes too large, resist washes away.</td>
</tr>
<tr>
<td>5</td>
<td>laminate</td>
<td>fully exposed laminate</td>
<td>holes too large, resist washes away.</td>
</tr>
</tbody>
</table>

6.1.3. Method Three

The final method used that successfully achieved plated inductors on Al₂O₃ was a method of masking, drilling, and plating. This technique is a liftoff technique where the metal plating process has poor adhesion to the photoresist and can be easily removed leaving behind the inductor traces. This process avoids the etching process which was eroding the plated vias in the first trials. A detailed process of this method follows.

1. Spin on liquid photoresist on one side.
2. Let dry (air) for 10min.
3. Spin on liquid photoresist on second side.
4. Soft bake at 90deg. C for 30min.
5. Photo expose side one in darkroom UV unit for 5min.
6. Photo expose side two in darkroom UV unit for 5min.
   (Note: expose immediately after spin and softbake.)
7. Drill holes in substrate.
   (Note: place paper towel between substrate and glass to prevent scratching of photoresist.)
   4min. part B Transene RTM process.
   4min. part C Transene RTM process.
   2 to 3 min. part D Transene RTM process.
   Repeat if necessary halving times in B and C.
9. Remove excess nickel from photoresist.
10. Strip of photoresist.
11. Gently wet sand with 600 grit if excess nickel on the photoresist remains. Strip off and extra photoresist.
12. Electroplate copper at 0.3 amps moving clip every 5 min. until an even coating of copper is achieved.
13. Once a thin layer of copper is achieved over the entire pattern, Slowly increase the current to achieve faster plating.
14. Polish by wet sanding with 330 grit and finishing with 600 grit.

### 6.2. Thick Film Ferrite Characterization

This section will discuss the characterization of a thick film ferrite paste developed for planar inductor formation on prefired alumina. Processing temperature at 850 degrees centigrade and 930 degrees centigrade was also investigated. The paste is to be used with a typical thick film process of printing, drying, and firing. The characterization of the ferrite paste was done by initially printing twenty-five substrates with an inductor array. The process is given below.

- Fifty 2" by 2", 96% Alumina substrates were cleaned by ultrasonic cleaning deionised water. The cleaned substrates were then printed, dried and fired in the following sequence:
  - An array of sixteen spiral inductors was used in the fabrication of seventy five substrates.
    - 25 substrates -- metal spiral
    - 25 substrates -- metal spiral sandwiched between a top and bottom layer of ferrite fired at 850°C
    - 25 substrates -- metal spiral sandwiched between a top and bottom layer of ferrite fired at 930°C

- The inductor array consists of:
  - 4 three turn spirals
  - 4 four turn spirals
  - 4 five turn spirals
  - 4 six turn spirals

- A layer of ferrite paste was printed. A settling time of 15 minutes was allowed under a laminar flow hood. The substrates were then dried at 120°C for 15 more minutes.

- The substrates were then split into two groups of twenty five and fired.
Group 1 -- 25 substrates fired at 850°C peak (first ferrite layer).
Group 2 -- 25 substrates fired at 930°C peak (first ferrite layer).

- All the substrates are then printed with a layer of ESL conductor paste 9912 lot# 2554-24. The substrates are then kept under the laminar flowhood for 15 minutes and dried in an oven at 120°C for 15 more minutes. The substrates are then fired.

  Group 1 -- fired at 850°C peak (metal layer).
  Group 2 -- fired at 930°C peak (metal layer)
- The substrates were then printed with a layer of the ferrite paste under experimentation, and dried at 120°C for 15 minutes. The substrates are fired separately, Group 1 at 850°C and Group 2 at 930°C.

- 25 substrates were printed, dried and fired with a layer of conductor paste only in order to make a comparative study with the substrates printed with the ferrite paste.

Once the printing was complete, the inductance of the metal spirals, with and without the ferrite paste, was measured with an HP-4193A impedance meter. The impedance and phase data were measured from 400KHz to 100MHz using a logarithmic sweep. The data from the HP-4193A impedance meter was obtained through a GPIB interface using LabVIEW®.

Probe open and short data were obtained in a similar manor.

1. Open circuit the fixture.
2. The open circuit impedance and phase is measured from 400KHz to 100MHz.
3. A short is formed by holding the probe against a metal plane.
4. The short circuit impedance and phase is measured from 400KHz to 100MHz.
5. The shorted condition is then removed.
6. The probe is now held on the device to be measured and the frequency is swept.

A MATLAB® program was then used to extract the probe parasitics, using the open and short data, from measured data. The permeability of the magnetic material can be determined by the following formula as given by [KAS92].
\[
\mu = \frac{L_{\text{magnetic}}}{2L_{\text{metal}} - L_{\text{magnetic}}} 
\]  

(6.1)

The permeability was calculated at each frequency and then plotted. MathCAD\textsuperscript{®} was used to confirm measured data with theoretical calculations, and are in Appendix B.

- Due to assumption number four, the measurements from the six turn spirals were used in the evaluation of the permeability.

### Table 6.2. Spiral Inductors Geometries and Values.

<table>
<thead>
<tr>
<th>Inductor Turns (n)</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Radius (Ri)</td>
<td>10 mls</td>
<td>10 mls</td>
<td>10 mls</td>
<td>10 mls</td>
</tr>
<tr>
<td>Outer Radius (Ro)</td>
<td>70 mls</td>
<td>90 mls</td>
<td>110 mls</td>
<td>130 mls</td>
</tr>
<tr>
<td>Conductor Width (W)</td>
<td>10 mls</td>
<td>10 mls</td>
<td>10 mls</td>
<td>10 mls</td>
</tr>
<tr>
<td>Breadth of Coil (c)</td>
<td>60 mls</td>
<td>80 mls</td>
<td>100 mls</td>
<td>120 mls</td>
</tr>
<tr>
<td>Average Radius (a)</td>
<td>40 mls</td>
<td>50 mls</td>
<td>60 mls</td>
<td>70 mls</td>
</tr>
<tr>
<td>Calculated Inductance</td>
<td>0.014(\mu)H</td>
<td>0.029(\mu)H</td>
<td>0.053(\mu)H</td>
<td>0.066(\mu)H</td>
</tr>
</tbody>
</table>

\[
L = \frac{0.8a^2n^2}{6a + 10c}
\]
Figure 6.1. Impedance and Phase of Thick Film Spiral Inductors. 3, 4, 5, and 6 Turn Spirals on Alumina
Figure 6.2. Impedance and Phase of Thick Film Spiral Inductors. 3, 4, 5, and 6 Turn Spirals on Alumina
Spiral Inductor ESR Frequency Variation
3, 4, 5, and 6 turns

Figure 6.3. Impedance and Phase of Thick Film Spiral Inductors.
3, 4, 5, and 6 Turn Spirals on Alumina
Spiral Inductor ESR Frequency Variation
3, 4, 5, and 6 turns

Figure 6.4. Impedance and Phase of Thick Film Spiral Inductors.
3, 4, 5, and 6 Turn Spirals on Alumina
Spiral Inductor Impedance and Phase Frequency Variation
3, 4, 5, and 6 turns

Figure 6.5. Impedance and Phase of Thick Film Spiral Inductors with Ferrite fired at 850 deg. C.
3, 4, 5, and 6 Turn Spirals on Alumina with Ferrite

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Figure 6.6. Quality Factor of Thick Film Spiral Inductors with Ferrite fired at 850 deg. C. 
3, 4, 5, and 6 Turn Spirals on Alumina with Ferrite
Figure 6.7. Equivalent Series Resistance of Thick Film Spiral Inductors with Ferrite fired at 850 deg. C. 3, 4, 5, and 6 Turn Spirals on Alumina with Ferrite
Figure 6.8. Inductance of Thick Film Spiral Inductors with Ferrite fired at 850 deg. C. 
3, 4, 5, and 6 Turn Spirals on Alumina with Ferrite
### Spiral Inductor Impedance and Phase Frequency Variation

3, 4, 5, and 6 turns

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Impedance (Ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00E+05</td>
<td>-9.00E+01</td>
</tr>
<tr>
<td>1.00E+06</td>
<td>-7.00E+01</td>
</tr>
<tr>
<td>1.00E+07</td>
<td>-5.00E+01</td>
</tr>
<tr>
<td>1.00E+08</td>
<td>-3.00E+01</td>
</tr>
<tr>
<td></td>
<td>-1.00E+01</td>
</tr>
<tr>
<td></td>
<td>1.00E+01</td>
</tr>
<tr>
<td></td>
<td>3.00E+01</td>
</tr>
<tr>
<td></td>
<td>5.00E+01</td>
</tr>
<tr>
<td></td>
<td>7.00E+01</td>
</tr>
<tr>
<td></td>
<td>9.00E+01</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Phase (Degrees)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00E+05</td>
<td>-9.00E+01</td>
</tr>
<tr>
<td>1.00E+06</td>
<td>-7.00E+01</td>
</tr>
<tr>
<td>1.00E+07</td>
<td>-5.00E+01</td>
</tr>
<tr>
<td>1.00E+08</td>
<td>-3.00E+01</td>
</tr>
<tr>
<td></td>
<td>-1.00E+01</td>
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<td></td>
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<td>3.00E+01</td>
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<td>5.00E+01</td>
</tr>
<tr>
<td></td>
<td>7.00E+01</td>
</tr>
<tr>
<td></td>
<td>9.00E+01</td>
</tr>
</tbody>
</table>

**Figure 6.9. Impedance and Phase of Thick Film Spiral Inductors with Ferrite fired at 930 deg. C. 3, 4, 5, and 6 Turn Spirals on Alumina with Ferrite**
Figure 6.10. Quality Factor of Thick Film Spiral Inductors with Ferrite fired at 930 deg. C. 3, 4, 5, and 6 Turn Spirals on Alumina with Ferrite
Figure 6.11. Equivalent Series Resistance of Thick Film Spiral Inductors with Ferrite fired at 930 deg. C. 3, 4, 5, and 6 Turn Spirals on Alumina with Ferrite
Figure 6.12. Inductance of Thick Film Spiral Inductors with Ferrite fired at 930 deg. C.
3, 4, 5, and 6 Turn Spirals on Alumina with Ferrite
Figure 6.13. Impedance and Phase of a Thick Film, 6 Turn Spiral Inductor on Alumina Without Ferrite, Ferrite Fired at 850 deg. C., and Ferrite Fired at 930 deg. C.
Figure 6.14. Equivalent Series Resistance of a Thick Film, 6 turn Spiral Inductor on Alumina Without Ferrite, Ferrite Fired at 850 deg. C., and Ferrite Fired at 930 deg. C.
Figure 6.15. Quality Factor of a Thick Film, 6 turn Spiral Inductor on Alumina Without Ferrite, Ferrite Fired at 850 deg. C., and Ferrite Fired at 930 deg. C.
Figure 6.16. Inductance of a Thick Film, 6 turn Spiral Inductor on Alumina Without Ferrite, Ferrite Fired at 850 deg. C., and Ferrite Fired at 930 deg. C.
Figure 6.17. Permeability of a Thick Film Ferrite Paste Based on a 6 turn Spiral Inductor on Alumina-Ferrite Fired at 850 deg. C. and Ferrite Fired at 930 deg. C.
From the measurements and calculations, the permeability of the ferrite paste was found to be between 1.3 and 1.4. This value is too small to be of any practical use in SMPS circuits. Further research would be necessary to find a suitable ferrite paste with increased permeability.

6.3. Planar Inductors with Attached Ferrite Core

Appendix C and Appendix D show a MathCAD® program that was generated to design a planar inductor on LTCC with an attached ferrite core. The losses in the windings due to the resistance of the windings proved to be large. While better results were achieved then for the printed thick film ferrite paste, the size of the overall inductor is still large.

6.4. Conclusions

While this chapter covered several methods for inductor and transformer miniaturization, none of the methods were found useful for the SMPS constructed in the latter stage of this research. Permeabilities of the thick film paste are too low, the losses in the attached ferrite planar thick film inductor would be too high.
7. Power Circuit Design

If a microcircuit dissipates more than 5 watts per square inch, then it is classified as a power circuit. Special design and fabrication techniques are needed to control device temperatures, insure reliability, and guarantee performance requirements. There are four specific areas that must be investigated in the development of a power circuit. These areas are:

- **Substrate and Metallization Selection**: Substrates with good electrical isolation, large thermal conductivities, and high mechanical strength are needed.

- **High Voltage Design**: Prevention of arcing, as well as suitable derating of components, are two major issues.

- **High Current Design**: Since $I^2R$ loss is a strong function of current, attention must be directed toward minimizing voltage drops which affect efficiency, and may also result in localized heating of circuit traces.

- **Thermal Design**: Device spacing, proper heat sink selection, as well as materials selection, are integral components of viable thermal management.

7.1. **Substrate Selection**

There are primarily five types of commercially available substrate materials that are used with power circuits: Insulated metal substrates (IMS), alumina ($\text{Al}_2\text{O}_3$), beryllia (BeO), aluminum nitride ($\text{AlN}$), and CVD Diamond. These materials are commonly used for the following reasons:

- Thermal Coefficient of Expansion (CTE) closely matches silicon.

- High thermal conductivity.

- Low dielectric constant.

- Electrical Isolation.

- The ability to provide high quality metallizations.
The toxicity of beryllia and the high cost of CVD diamond usually exclude these materials for implementation except under special circumstances. As a result, alumina and increasingly aluminum nitride are the materials of choice. The thermal conductivity of aluminum nitride (~200 watts/mK) is ten times that of alumina (~20 watts/mK), which makes it superior for heat dissipation in power circuits. Alumina is a very stable oxide while Aluminum Nitride is unstable at high temperatures. As a result, AlN is more difficult to process, since inadequate film adhesion and decomposition of the surface layers of an AlN substrate can occur. IMS boards are attractive due to the potential for low cost, however, the organic dielectric insulation is a limiting factor due to its low thermal conductivity and large CTE. These effects reduce the overall reliability of IMS boards, in addition to the inability to integrate passive components.

Depending on the circuit dimensions and the current density required, several choices of metallizations are available. The most common are: thin film, thick film, and Direct Bond Copper (DBC). Both thin and thick film allow for passive components integration, while DBC requires the use of passive components in surface mounted packages. Thick film offers the advantages of allowing a high current carrying capability, small inexpensive passive component integration with the capability of mass production. Thin films are more versatile, however, power circuits require thick conductors which can be difficult to obtain with conventional thin film techniques. In addition, the costs associated with thin films are normally higher due to the requirement for vacuum deposition systems.

Based on these facts thick film and DBC are two ideal candidates for miniature power supply fabrication. DBC offers the highest thermal conductivity, with very thick conductors, and is ideal for very high power circuits. Thick film is versatile and inexpensive, while offering the
greatest potential for the integration of passive components. As a result, this research effort will focus on thick film and DBC solutions.

7.2. High Voltage Design

Voltages in excess of 100 volts for a microcircuit are classified as high voltage circuits due to the small dimensions used. High voltage practices must be implemented in power circuits in order to avoid breakdown. The underrated voltage breakdown of the four materials listed in the previous section, are tabulated below in Table 7.1, along with other key properties.

<table>
<thead>
<tr>
<th>Material</th>
<th>CTE (ppm/K)</th>
<th>Breakdown Voltage (volts/mil)</th>
<th>Thermal Conductivity (W/mK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlN</td>
<td>3.0 - 4.5</td>
<td>600</td>
<td>100-170</td>
</tr>
<tr>
<td>Al2O3 (96%)</td>
<td>6.4</td>
<td>600</td>
<td>29</td>
</tr>
<tr>
<td>AlSiC (60% Al)</td>
<td>12.6</td>
<td></td>
<td>240</td>
</tr>
<tr>
<td>AlSiC (63% SiC)</td>
<td>7.9</td>
<td></td>
<td>175</td>
</tr>
<tr>
<td>Aluminum</td>
<td>24</td>
<td></td>
<td>226</td>
</tr>
<tr>
<td>Be-BeO MMC</td>
<td>6.8</td>
<td>770</td>
<td>240</td>
</tr>
<tr>
<td>Copper</td>
<td>17</td>
<td></td>
<td>393</td>
</tr>
<tr>
<td>Cu-Mo</td>
<td>7.2</td>
<td></td>
<td>197</td>
</tr>
<tr>
<td>Cu-W (20% Cu)</td>
<td>7.0</td>
<td></td>
<td>248</td>
</tr>
<tr>
<td>Diamond</td>
<td>0.8 - 2.0</td>
<td>8,570</td>
<td>1000 - 2000</td>
</tr>
<tr>
<td>Graphite-Cu MMC</td>
<td>0 - 2.0</td>
<td></td>
<td>356</td>
</tr>
<tr>
<td>Gold</td>
<td>3.1</td>
<td></td>
<td>317</td>
</tr>
<tr>
<td>Invar</td>
<td>5.3</td>
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<tr>
<td>Kovar</td>
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<td>Molybdenum</td>
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<td>Silicon</td>
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<td>429</td>
</tr>
<tr>
<td>Silver</td>
<td>50</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In comparison, the breakdown voltage of air at 1 atmosphere is 58 volts/mil ac and 84 volts/mil dc. As a result, the operating environment of the circuit (in air) is the limiting factor. So with an added margin of safety, all conductor widths should be designed with 40 volts/mil (or

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lower) spacing. This distance also applies to all conductor spacing including wirebond to wirebond, and wirebond to chip, so that special care must be taken when using crossovers.

7.3. High Current Design

High current design is necessary to insure that conductors and wirebonds do not fuse open, to reduce thermal resistance, and to minimize conductor voltage drop. The damage caused by large amounts of current in a conductor may not be immediately detected. Metal migration can occur over time as a large current can pull atoms of the metal along and then deposit them further down the current path.

To minimize the voltage drops, shorter wider conductors should be used. Additional pins and wirebonds should be used where needed. Smaller loops on wirebonds will also help reduce voltage drops. Larger diameter bond wires and thicker conductor metallization can also be employed although these may be restricted to the materials, equipment, and techniques available. The current that can be delivered along a conductive path is dependent on the type of conductor metal and on the material in which the conductor is in contact. Normally a current density of $6 \times 10^5$ Amps/cm² (for Au on Alumina) is determined to be the absolute maximum, however, trace widths are normally dictated by the available space and minimum voltage drop which can be tolerated. The result is that very rarely will the maximum current density ever be approached in reliable designs.
7.4. Thermal Design

The three mechanisms of heat removal in a hybrid circuit are conduction, convection, and radiation. The majority of heat is removed through conduction; therefore, it is important to attach components to the substrate using a thermally conductive compound. Since the current design uses packaged components, solder is the prefired attachment media. Solder offers good electrical conductivity, and thermal conductivity, while providing a strong physical connection. A very large number of solders exist, however, selection of the most appropriate material is usually based on electrical and thermal conductivity as well as material compatibility issues.

Placement is also very important to heat removal. The substrate edge acts as a mirror to heat, so components that generate large amounts of heat should not be placed in these areas. In addition, based on computer simulations, the typical power dissipation of each component can be determined. This information is then used to place components such that the dissipated thermal energy is spaced as evenly as possible over the entire substrate, rather than localized in one area. Design tradeoffs must balance the electrical gains provided by close component spacing with the thermal requirement of maximum possible separation.

7.5. Conclusions

Three areas compete: voltage, current, and thermal issues are not mutually exclusive. In a switch mode power supply design, all these issues compete against each other. Thermal issues may restrict close placement of power dissipating components. This causes the design layout to consume the larger area. Current issues have the opposite effect. It is desired to have components, particularly those carrying high currents, in close proximity to each other. In other words, short
and fat interconnect traces. Also, voltage issues require minimum space requirements between traces and devices. Voltage breakdown or arching can occur if proper spacing is not implemented. Once again, this restricts how close in proximity traces can be laid out. In the next several chapters, these restrictions will become apparent.
8. SMPS Circuit Miniaturization on PCB and DBC

Research efforts realized three versions of a SMPS boost circuit, two Direct Bond Copper (DBC) on Al₂O₃ and one DBC on AlN. Research also realized passive components for power circuit applications that could be used in the miniaturization of the boost circuit. Three additional versions of the miniaturized boost were developed using thick film technology. The thick film research also realized a daughter board for a half-bridge control circuitry of the fluorescent lamp ballast. This chapter reviews the ballast miniaturization efforts. This chapter will discuss miniaturization efforts on DBC and PCB while the next chapter will discuss miniaturization efforts related to thick film.

8.1. Switch Mode Power Supply Description

Switch Mode Power Supplies (SMPS) process electrical power by abruptly turning on and off voltages and/or currents. Semiconductor devices such as MOSFETs, IGBTs, and diodes are used as electrical switches. In most cases, an Application Specific Integrated Circuit (ASIC) is used to control the timing of these semiconductor switches. The occurrence of the abrupt transients in these types of circuits generate large amounts of Electromagnetic Interference (EMI). The constant switching of current and voltage in the semiconductor devices cause switching losses in these devices and generate excessive heat as a direct result.

As many SMPS operate in an off-line mode (no isolation transformer between the power lines and the circuit), proper filtering of EMI must be incorporated into the circuit design to prevent leakage of interference to the power mains. Filtering must also be provided on the output of the SMPS to filter the load from the same interference. Off-line operation also means that high

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voltages will be present within the circuit even if the output produces low voltage levels. A
generalized block diagram for a typical SMPS consists of three basic elements; filtering,
switching, and control. Each section of the SMPS may require vastly different electrical and
thermal requirements on the passive components.

8.2. Boost Circuit with Power Factor Correction

The boost circuit is one of the most common type of switched mode power supply
topologies. The function of this type of circuit is to drive the output voltage to a higher level than
the corresponding input voltage. In order to test different methods for miniaturization of power
supplies, a typical boost circuit topology was chosen and then different methodologies and
technologies were applied to the same design. Figure 8.1 shows the basic topology for this type of
circuit.

One of the problems with the new generation of switched mode power supplies is the EMI
that is injected onto the power lines. Another problem is that large current spikes are generated by
the typical nonlinear electronic power supply. The concept of Power Factor Correction (PFC) is
introduced to help reduce the EMI issue as well as the peak currents drawn by the power
supplies. The concept behind power factor corrected circuit is that the switching is performed the
precise intervals in order to produce current and voltage reforms that make the circuit appear
purely resistive. What this translates to is a sinusoidal input current and a sinusoidal input voltage
that are both in phase with each other. The power factor of one is ideal while a power factor of
zero translates to a completely reactive load.

In this research, a control IC manufactured by Motorola was chosen. The IC, MC34262,
is a active power factor controller designed for off-line power converter applications. This power
converter IC operates in a critical conduction mode of operation. The application design around this IC is a boost converter with power factor correction. The input voltage will be standard United States 120 volts line voltage and the output will be adjustable from 250 volts to 280 volts. The converter is designed to deliver 60 watts to a resistive load.

8.3. Printed Circuit Board Boost Circuit - Through Hole Version

The original Printed Circuit Board (PCB) version of the boost circuit was produced as a starting point. This version was a conventional PCB circuit utilizing through hole components, shown in Figure 8.3. This circuit acts as a baseline for all the future developments of the boost circuit. The base operation frequency of this circuit is 50kHz and was designed to operate off the line at 120V AC and boost to 270V DC.

8.4. DBC Conductor Pattern Generation

The first step in the conductor pattern generation is to plot the AutoCAD® rendering of the metal on to a sheet of Rubylith®. If photo reduction is necessary (plot not 1 to 1), the Rubylith® is selectively removed to produce a positive image of the metallization. This image is then photo reduced to produce a negative 1 to 1 mask.

To help prevent the copper metallization from oxidizing, a gold or nickel platting is recommended. The process used for these experiments was nickel electroplating and was conducted as follows. The substrate with copper was thoroughly cleaned while the Watts® nickel plating solution was heated to 57°C. The negative terminal of a current supply was attached to the substrate and the positive terminal to a stainless steel shim stock. Once the substrate and stock
were immersed in the solution (plates were not touching), a 20mA current was applied. Once an even coating of nickel formed, the substrate was removed and rinsed clean of plating solution. A metal polish can be used to increase luster, but all traces of polish must be removed before the next step. An electroless system of platting can also be used; in which case, plating is conducted after the etching is complete. The electroless process protects the edges of the metal traces as well as the top surface, in contrast to electroplating that just protects the top surface.

A Kepro® circuit development system was used to produce the metallization patterns. The DBC substrate coated with nickel was heated to 100°C and then coated with photoresist (both sides). The preheat helped to adhere the photoresist to the metal surface. The protective layer was removed from the top and the mask aligned. Exposure took six minutes per side in the UV unit.

The photoresist was developed using Sodium Bicarbonate (NaHCO₃). The progress of pattern generation was checked in 30 second increments until a dark pattern was generated. A small scratch test was applied to a unexposed area to make sure the photoresist had been completely removed from these areas.

Once fully developed the developer was washed away with de-ionised water. The metal was then etched in one minute intervals with Ferric Chloride (FeCl₃). In between intervals, the pattern was checked for completeness. Once the pattern was fully etched and rinsed, the protective photoresist backing was removed from the backside. The exposed photoresist on both sides was removed with acetone.
8.5. Direct Bond Copper Boost Circuit - Version #1

The first generation of the boost circuit was developed with 12mil (304.8 µm) thick Direct Bond Copper (DBC) on a 25mil (635 µm) thick alumina substrate. For this material, a current density of 25 kAmps/in² was used to calculate the minimum conductor width for a peak current of 4 amps. In this case, the minimum width was 13.3 mils (337.8 µm). This width was small when compared to the accuracy of etching 12 mil thick copper; therefore, the minimum width was limited by this restriction. It was determined that conductors should be as wide as possible to reduce voltage drops; therefore, the width limit was only required as an absolute minimum. The conductors should be made as wide as possible, leaving a minimum distance between conductors defined by process restriction and or high voltage breakdown. This value was determined in the simulations to be greater than 7.5 mils (190.5 µm).

The first generation DBC on alumina component layout is shown in Figure 8.2 and the metallization pattern in Figure 8.3. The substrate was 2 in x 2 in (50.8 mm x 50.8 mm) and is not drawn to scale in these figures. This initial effort was not intended to result in any miniaturization but rather as a test vehicle to evaluate and eliminate any design and testing problems that may have resulted from the use of new surface mount components. Figure 8.4 is a photo of the first generation circuit next to the PCB version (2.5 in x 2.5 in x 1.25 in).

8.6. Direct Bond Copper Boost Circuit - Version #2

The second generation boost was developed with 12mil thick Direct Bond Copper (DBC) on a 25mil thick Aluminum Nitride (AlN) substrate. Because AlN has about seven times the thermal conductivity of alumina, once again, the minimum conductor width required for a peak
current of 4 amps was overshadowed by limitations in etching. The same conductor to conductor spacing was required. Figure 8.5 and Figure 8.6 show the component layout and metallization pattern, respectively. The size of the AlN substrate is 2in x 1.4in (50.8mm x 35.6mm). Figure 8.7 shows the second generation DBC circuit on AlN. The inductor in this version was changed (decreased in value) to increase the base line operating frequency from 50kHz to 250kHz. This change helped to decrease the height of the circuit as well as reduce the surface area.
Figure 8.1. Boost Circuit Schematic - Version #1.
Figure 8.2. First Generation Component Layout.
Figure 8.3. First Generation Metallization Pattern.
Figure 8.4. Original FR-4 Through Hole Version and First Generation on Alumina DBC.
Figure 8.5. Second Generation Component Layout.
Figure 8.6. Second Generation Metallization Pattern.
Figure 8.7. Second Generation DBC SMT Version on AlN.
8.6.1. Conducted EMI

In the United States the FCC governs the amount of Electromagnetic Interference (EMI) that can be conducted onto the power lines. The widely accepted, and most stringent of the regulatory standards, is the German VDE.

The frequency switching in a SMPS must be properly filtered before it reaches the power line mains. If not properly filtered, this interference may find its way into other electronic devices on the power mains. If the receiving device is a television or radio, operation can be severely degraded. It is the purpose of the regulation agencies to help limit the amount of noise on the power mains, thus reducing the burden on electronics manufacturers to prefilter the power from the main supply.

SMPS with their high switching frequencies can generate large amounts of conducted EMI if not properly filtered. In the efforts to miniaturize a SMPS it is important to determine the level of EMI, and modify the layout and package requirements if necessary to help reduce the EMI level. In this research, the initial levels were measured so the effect of operational frequency increases, surface mount components, and the effect of parasitics could be quantified.

The total conducted EMI can be separated into two components, common mode noise and differential mode noise. Differential mode noise exists on the supply power lines, while the common mode noises exist on the power lines as one conductive path and on the earth ground as the other conducted path [ARR95]. The main switching components, and inductive and resistive parasitics cause the differential mode noise to increase. Capacitive coupling to the earth ground will increase the common mode noise. Heat sinks can be a large source of common mode noise because of the capacitive structure formed, metal heat sink plate, insulator, device package metal
plate. Reduction efforts can be separated and therefore it is important to measure both types of EMI.

8.6.2. Conducted EMI Equipment and test setup

Three types of line EMI measurements were conducted: differential mode, common mode, and total. The test set up is shown in Figures 8.7 through 8.10. The EMI measurements were taken in compliance with EMI test regulations. The measurements were taken inside a EMI and RFI shielded room. Line Impedance Stabilization Networks (LISN) are used to provide a known impedance (50 Ohms) of the power lines. The networks also filter out any noise that is already on the line. With different LISN blocks, the total, differential mode, and common mode noise may be measured. The equipment list is as follows,

Power Supply: Lambda LLS9300
Output 0-300V@2.8A

Power Analyzer: Voltech PM3000A Universal Power Analyzer

LISN: Line Impedance Stabilization Network
Type 8028-50-ts-24-BNC
Solar Electric Company

Spectrum Analyzer: HP 8568B 100Hz-1.5GHz

LISN DMR: Line Impedance Stabilization Network
Differential Mode Rejection
Model DMRN-1
EMC Services

LISN CMR: Line Impedance Stabilization Network
Common Mode Rejection
Model CMRN-1
EMC Services

CUT: Circuit Under Test
Figure 8.8. Differential Mode Conducted EMI Test Setup.
Figure 8.9. Common Mode Conducted EMI Test Setup.
Figure 8.10. Total Conducted EMI Test Setup.
8.6.3. Conducted EMI Measurements

Figures 8.11, 8.12, and 8.13 show the measured differential mode, common mode, and the total line EMI for the through hole PCB boost circuit. Likewise, Figures 8.14, 8.15, and 8.16 show the measured differential mode common mode and the total line EMI for the second generation DBC on AlN boost circuit.

It was first noticed that the replacement of the transformer did double the operating frequency as was seen from the fundamental mode frequency, 50kHz for the PCB and 250kHz for the second generation circuit. Harmonic suppression in the second generation had been reduced because of the reduction of the filter component values when selecting surface mount counterparts. It was also determined that the input capacitor on the second generation circuit had poor frequency characteristics and needed to be replaced. This capacitor also seemed to be responsible in some part for the reduced efficiency as compared to the printed circuit board.

The increased switching frequency and the poor input capacitor characteristics account for the increased differential noise. Component parasitics and layout parasitics also contribute to the increased differential noise. Correct component selection is critical in reducing the differential noise. The common mode noise had the biggest increases. This is due to increased capacitive coupling of the switching components in respect to the ground line.
Figure 8.11. Differential Mode Noise Spectrum - PCB Version.
Figure 8.12. Common Mode Noise Spectrum - PCB Version.
Figure 8.13. Total Noise Spectrum - PCB Version.
Figure 8.14. Differential Mode Noise Spectrum - DBC Version.
Figure 8.15. Common Mode Noise Spectrum - DBC Version.
Figure 8.16. Total Noise Spectrum - DBC Version.
8.6.4. Power Factor and Efficiency Measurements

Power factor, and efficiency measurements were taken on both the PCB circuit and the AlN DBC second generation circuit. Power factor and efficiency measurements were taken on the second generation alumina DBC circuit. Although the power factor increased to .998 in the second generation device from .985 in the PCB, the efficiency dropped from 95.0% to 92.3%. The loss increased in the storage inductor as the miniaturization efforts pushed the core further into saturation. Also the faulty input capacitor was causing loss problems. In addition, a direct comparison of the PCB technology and Direct bond copper on an electrical basis is not possible since the reduced electrical performance appeared to be largely due to the performance of the different electrical components rather than the technology itself. Other supplies have constructed using this same technology and have found, in general, an increase in efficiency rather than a decrease. An example of this would be a DC to DC converter with a 3 Volt output and a total power of 100 watts. A 5% increase in efficiency was observed in DBC as compared to a printed circuit board when identical components were used in both cases.

8.7. DBC Boost Circuit Version #2 VS. FR-4

To access the advantage of ceramic substrate materials, this layout was assembled on FR-4. Figure 8.17 shows the same layout on FR-4. With all aspects being equal except the substrate material, Thermal and electrical tests were conducted. These results are shown in the next chapter where this version is compared to a thick film version.
Figure 8.17. Second Generation SMT Version on FR-4.
8.8. Conclusions

The research covered in this chapter revealed many pertinent issues. The miniaturization of a SMPS requires a complete understanding of topology, component selection, layout issues, and appropriate testing. A typical SMPS was developed from a Motorola PFC controller IC. A base level design was fabricated using FR-4 technology and through hole components. This circuit acts as a base line for comparison.

Two DBC boost circuits were fabricated using SMT components. The frequency of operation was increased in order that the physical size of the magnetic component (inductor) could be reduced. The losses increased as a result. The ceramic substrates helped to remove the heat from the inductor, but efficiency was reduced. Conducted EMI measurements demonstrated that component selection is critical as well as layout parasitics.
9. SMPS Circuit Miniaturization Using Thick Film Technology

Research also realized passive components for power circuit applications that could be used in the miniaturization of the boost circuit. Three versions of the miniaturized boost were developed using thick film technology. The thick film research also realized a daughter board for a half-bridge control circuitry. This chapter reviews the boost miniaturization efforts with respect to thick film technology.

9.1. Thick Film Boost Circuit — Version #1

The first thick film version incorporated integrated thick film resistors and capacitors developed and described in previous chapters. The schematic for the thick film version #1 is shown in Chapter 8. Four resistors and four capacitors were integrated using thick film; capacitors C2, C8, C11, C19, and resistors R1, R2, R5, R8, were integrated. The remaining passives were SMT components with the exception of C5 which was an attached through hole electrolytic capacitor.

Figure 9.1 shows the layout of the thick film boost circuit version #1. Surface area reduction was achieved from the DBC efforts. The dimensions for this version were 1.87” x 1.31” x 0.5”. The height of 0.5” was governed by the surface mount electrolytic capacitor C3. The integrated passives were placed under SMT components. For instance, C11 was placed beneath the transformer (lower left corner) and C19 was placed beneath the SMT electrolytic capacitor C3 (top right corner). The same type of placement was achieved with the integrated resistors. Figure 9.2 is a picture of the thick film version #1 boost circuit with passivation layer (blue layer) and without C5 attached.
It was found in the testing phase that C2 and C8 would breakdown due to the high voltage levels present. If these components are to be integrated in the future, more than three dielectric printings will be required to obtain the desired voltage ratings. It should be noted that this will increase the surface area required by these devices.

Further surface area reduction was limited by the size of the components; smaller devices, semiconductor die, and/or better utilization of the volume would be needed achieve the next significant reduction in surface area.

9.2. Thick Film Boost Circuit — Version #2

The second thick film version constituted a change in some of the components. To tune the control circuit more accurately, the variable resistors, R4 and R11 were changed to larger 10 turn versions. Diode D2 was replaced with one with a higher current rating. The MOSFET Q1 (IRF740) was replaced with a physically smaller MOSFET (IRFU320). A much smaller inductor (transformer) was also used, a Philips EFD15 3F3. Some of the capacitor values were also changed. The schematic for version #2 is shown in Figure 9.3.

In this version, the surface mount resistors and capacitors were placed upright on end thus utilizing more of the previously wasted volume in the upward direction while reducing the footprint of each device. The diode bridge on the input was replaced by four diodes. Less area was needed for these smaller components. If this version is to be incorporated with the rest of the ballast, the rectifier diodes are small enough to fit under the edge of the inductor thus reducing further the surface area. With this design, just the boost section, the fuse and power connector consume the upper corner and defeat any benefit of placing the diodes under the edge of the inductor. A more direct path through the main switches of the boost was achieved with this
version. D2, Q1, and R10 make a direct path across the board. The inductor was also placed directly next to D2. The majority of the IC connections are short and direct. Decoupling capacitors have been kept very close to their source. Because of the surface area lost due to reduction in the size of the inductor and considering the high voltage ratings required of capacitors C2 and C8, thick film integrated capacitors were not used in this version. Integrated resistors R1, R2, R5, and R8 were still used to achieve a size reduction.

The layout for version #2 is shown in Figure 9.4 and a version constructed on Al2O3 is shown in Figure 9.5. The overall dimensions of version #2 were 1.68” x 1.15” x 0.5”.

9.3. Boost Circuit with Thick Film Daughter board — Version #3

Version #3 incorporates a control daughter board made on a Al2O3. The daughter board consists of the following components: R1*, R2*, R4, R5*, R6, R8*, R11, R22*, C11, C12, C13, C19, D5, IC1. The * denotes integrated thick film components. Figure 9.6 shows the layout for the mother/daughter board combination. In this version, the thick film daughter board used a substrate that was thick film printed on both sides. Two different temperature solders were used in order to mount the components. A high temperature solder was used on the side with the variable resistors and the unit was reflowed on a belt reflow unit. Then, a lower temperature solder was used to attach the components on the side with the control chip and the unit was reflowed in an IR unit. In this realization, surface mount components can be mounted on both sides.

The dimensions of the daughter board were 1.075” x 0.415”. The main board dimensions were 1.15” x 1.45”. The pin spacing for the daughter board was 100mil from center to center. The mother board was designed so that it could be fabricated with PCB technology, Insulated Metal Chapter 9
Substrate (IMS), conventional thick film, or DBC technology. Figures 9.8 and 9.9 show the two sides of the daughter board.

9.3.1. IMS with Thick Film Daughter board

The boost was fabricated with a mother board consisting of an Insulated Metal Substrate (IMS) and a thick film daughter board on alumina. The bottom of Figure 9.9 shows this circuit. The process for developing the IMS mother board is as follows:

1) Clean IMS with a weak solution of HCl to remove oxide.
2) Preheat IMS to 100°C.
3) Laminate backside of board.
4) Preheat IMS to 100°C.
5) Laminate the trace side.
6) Let IMS cool for 20 minutes.
7) Expose back side.
8) Place pattern on trace side and expose trace side.
9) Peel protective coating from trace side.
10) Develop until unexposed areas have been removed.
11) Etch IMS until pattern forms.
12) Remove photoresist with stripper.

9.3.2. FR-4 with Thick Film Daughter board

The boost was also fabricated with a mother board on FR-4 and a thick film daughter board on alumina. The top of Figure 9.9 shows this circuit. The electrical measurements were taken on the mother/daughter (FR-4/Al₂O₃) board combination. The input and output characteristics are shown in Figures 9.10 and 9.11, respectively. This circuit operates as expected. The other measured electrical parameters are,

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage</td>
<td>250V</td>
</tr>
<tr>
<td>Efficiency</td>
<td>94.41%</td>
</tr>
<tr>
<td>Power Factor</td>
<td>0.990</td>
</tr>
</tbody>
</table>
Thermal testing on the combined ceramic daughter board and FR4 mother board was conducted and compared to the PCB version. This boost configuration for the mother/daughter board configuration was for 250kHz with the EFD15 3F3 inductor while the PCB FR-4 version was for 250kHz with the EFD 3F3 inductor. A thermocouple was attached to the outside of the package on several components. The units were then allowed to operate until thermal equilibrium was reached. The results from this test are contained in the Table 9.1 below. The IC on the daughter board operates much cooler; it is clear there is a large thermal advantage of the Al₂O₃ daughter board version over the PCB version. For example the steady state operating temperature of control chip was measured to be 55°C. In contrast, the control chip of the boost circuits built on FR4 with SMT components runs at 80°C. The control chip is the only component in the daughter board thermally measured. All other components measured are on FR-4; this is why the temperatures are close in value for the other components on the PCB version and the mother/daughter board combination.

### Table 9.1. Thermal Characteristics of Boost Circuits.

<table>
<thead>
<tr>
<th></th>
<th>Module 270V Output</th>
<th>IC</th>
<th>Diode D2</th>
<th>MOSFET</th>
<th>Transformer</th>
<th>Bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB</td>
<td></td>
<td>80°C</td>
<td>72°C</td>
<td>61°C</td>
<td>68°C</td>
<td>70°C</td>
</tr>
<tr>
<td>M/D Al₂O₃</td>
<td></td>
<td>55°C</td>
<td>66°C</td>
<td>66°C</td>
<td>63°C</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td>Module 250V Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M/D Al₂O₃</td>
<td></td>
<td>49°C</td>
<td>60°C</td>
<td>55°C</td>
<td>56°C</td>
<td>NA</td>
</tr>
</tbody>
</table>
9.4. Summary of Boost Circuit Reduction Efforts

To quantify the gains achieved through the research efforts, Table 9.2 gives a comparison of each boost circuit version as compared to the original though hole version.

<table>
<thead>
<tr>
<th></th>
<th>Size (in)</th>
<th>Volume (in³)</th>
<th>Volume Reduction</th>
<th>Area (in²)</th>
<th>Area Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB</td>
<td>2.5x2.5x1.25</td>
<td>7.81</td>
<td>—</td>
<td>6.25</td>
<td>—</td>
</tr>
<tr>
<td>DBC</td>
<td>1.375x2.0x0.5</td>
<td>1.375</td>
<td>82%</td>
<td>2.75</td>
<td>56%</td>
</tr>
<tr>
<td>Thick Film Version #1</td>
<td>1.875x1.3125x0.5</td>
<td>1.231</td>
<td>84%</td>
<td>2.46</td>
<td>61%</td>
</tr>
<tr>
<td>Thick Film Version #2</td>
<td>1.68x1.15x0.5</td>
<td>0.966</td>
<td>88%</td>
<td>1.93</td>
<td>69%</td>
</tr>
<tr>
<td>Mother /Daughter Board w/o C5</td>
<td>1.30x1.15x0.5</td>
<td>0.748</td>
<td>90%</td>
<td>1.50</td>
<td>76%</td>
</tr>
</tbody>
</table>

9.5. Half-Bridge Circuit Reduction Efforts

The second part of a fluorescent lamp ballast, the half-bridge, was the concentration of miniaturized using the daughter board concept. Due to the large number of passive components associated with the control circuitry, extending the daughter board concept allows for a large size reduction as well as an increased reliability rating.

A prototype perf-board half-bridge was assembled to validate the components used in the design and for electrical comparison of future versions. This prototype was tested using resistive loads as well as actual lamps as shown in Figure 9.12. This figure shows the perf-board circuit operating two 35 Watt fluorescent bulbs with the prototype board connected below. For testing purposes, a bench top supply is used to provide power to the half bridge.

A small daughter board plugs into the mother board and contains virtually all the control components in a very compact space. The daughter board consists of the control chip (MC34067)
and its supporting circuitry. The daughter board is two sided thick film circuit on Alumina. Daughter board height is 6/10 of an inch and is limited by the size of the control chip (height can be decreased by bending leads and inserting board at an angle).

A schematic of the control chip and supporting components is shown in Figure 9.13. For this first version of the half-bridge daughter board, the MOSFETs and isolation torroidal transformer were excluded. Future generations may include these components when a solution if reached for integrating the torroid into the Alumina. A layout of the circuit is illustrated in Figure 9.14.

The half-bridge daughter board is a 1.30in long by 0.60 in height thick film alumina based circuit. Thick film metallization and components were only printed on one side to aid in the assembly process, only one temperature solder is needed and a reflow solder unit can be used to attach components. Figure 9.15 shows the one sided uncut daughter board on a 2in x 2in piece of alumina. Alignment markers and trim marks can be seen along the periphery of the substrate. This board will be cut in half by a high power laser or a diamond saw. SMT components can then be solder attached by a reflow solder method, Figure 9.16. Once the SMT components are attached the two sides can be combined using a high temperature epoxy. Finally the pins can be added and soldered using ordinary solder iron techniques. Figure 9.17 shows the completed daughter board before the pins connector has be removed.

The half-bridge consists of 19 resistors, 16 (84%) are on the daughter board. Of the 16 resistors on the daughter board, 12 (75%) are screen printed. If the pots were replaced by trimmed resistors, four resistor printing could achieve 100% resistor integration. The half-bridge consists of 23 capacitors, 12 (52%) are on the daughter board. A torroid core with wirebond windings maybe possible for replacement of T1.
To test the half-birdge daughter board, a through hole version of the mother board was assembled on FR-4. Through hole parts were used for first generation of mother board. It was built to test daughter board and not for miniaturization. Larger through hole components allow for easy probing in test stage. Overall mother board is 2.06in x 2.28in. The layout for the mother board is given in Figures 9.18 and 9.19. The final assembled circuit is shown in Figure 9.20.
Figure 9.18. Boost Circuit Thick Film Layout #1.
(1.87” x 1.31” x 0.5”).
Figure 9.19. Thick Film Boost Circuit with Integrated Capacitors and Resistors Version # 1.
(1.87in x 1.31in x 0.5in).
Figure 9.20. Boost Circuit Schematic - Version #2.
Figure 9.21. Boost Circuit Thick Film Layout Version #2
(1.68in x 1.15in).
Figure 9.22. Thick Film Boost Circuit with Integrated Resistors Version #2. (1.68” x 1.15” x 0.5”).
Figure 9.23. Boost Circuit Thick Film Layout #3 Mother/Daughter Board Combination.
Figure 9.24. Boost Circuit Version #3. Daughter Board Side 1.

Figure 9.25. Boost Circuit Version #3. Daughter Board Side 2.
Figure 9.26. Boost Circuit Layout #3 Mother/Daughter Board Combination. 
FR-4 Mother Board with Alumina Daughter board on top. 
IMS Mother Board with Alumina Daughter board on Bottom.
Figure 9.27. Boost Circuit FR-4 Mother Board with Alumina Daughter board Input Characteristics.
Figure 9.28. Boost Circuit FR-4 Mother Board with Alumina Daughter board Output Characteristics.
Figure 9.29. Operating Through Hole Perf-Board version of Half-Bridge.
Figure 9.30. Half-Bridge Daughter Board Control Schematic.
Figure 9.31. Half-Bridge Daughter Board Circuit Thick Film Layout #1.
Figure 9.32. Uncut Thick Film Half-Bridge Daughter Board with Integrated Resistors.
Figure 9.33. Thick Film Half-Bridge Daughter Board with SMT Components Attached.
Figure 9.34. Thick Film Half-Bridge Daughter Board with Both Halves and Pins Attached.
Figure 9.35. Half-Bridge Through Hole Mother Board Layout Top Side.
Figure 9.36. Half-Bridge Through Hole Mother Board Layout Bottom Side.
Figure 9.37. Half Bridge Circuit with Alumina Daughter Board.
9.6. Conclusions

This chapter validates the use of thick film in modern switched mode power supply design. The thick film components generated in on AlN were incorporated into a boost circuit design. Mother/Daughter board design was also validated. Large area reductions are possible through the use of integral passive components. In this research an area reduction of up to 76% was achieved. The use of daughter boards allows benefit of the integral components as well as the improved thermal properties of the substrate for select components. This will allow low cost designs to be developed while taking advantage of the ceramic properties. To validate the design, a half bridge circuit was also produced. Integration of the resistors was near 100%, thus improving on cost as well as reliability.
10. Conclusions and Future Directions

Thick film passive components have been successfully integrated on prefired AlN substrates and optimized for use with power electronic circuits. Using a passivation layer of low K dielectric, 1 mil in thickness, both resistor and dielectric pastes normally used for Al₂O₃ prefired substrates, may be applied on an AlN surface. Capacitors with densities of 120pF/mm² were characterized over a range of temperatures and frequencies. The capacitors were found to be optimized for 25°C operation and have a heavy temperature dependence from -25°C to 130°C and little frequency dependence up to 500kHz.

The thick film resistors proved to have little frequency dependence up to 500kHz. Thermally, the passivated resistors demonstrated superior heat dissipation on the passivated AlN as compared to the Al₂O₃. When 1.92W/mm² was applied to test resistors, the Al₂O₃ resistor’s average center temperature operated at 115°C. The average center temperature of an equivalent resistor on AlN operated at 65°C. The improved thermal properties of AlN and the ability of passive integrated components have made thick film power circuits a viable option.

This research addressed the miniaturization of a boost stage power supply with emphasis on Copper Cladded Aluminum Nitride (AlN) substrates and on prefired Aluminum Nitride substrates with thick film passive components integration. Three key issues; electrical characterization, thermal analysis and simulation, and materials characterization, were examined in order to achieve this goal. To exploit the benefits of AlN, parallel experiments were conducted on alumina (Al₂O₃) substrates to establish a reference in order to quantify the real gains accomplished with AlN use. Guidelines for the design, implementation, and the steps necessary to integrate...
these passive components on prefired alumina (Al₂O₃) and aluminum nitride (AlN) ceramic surfaces for power supply circuit applications were developed.

Electrical analysis and simulation were conducted to determine critical signal paths. Materials issues were also explored. The use of aluminum nitride, as a thick film ceramic substrate, and the resulting issues concerning compatible inks, were investigated. The thermal properties of passive components was studied. Due to the large amount of heat generated by power circuitry, the passive components were analyzed with regard to tolerance and degeneration over a certain range of temperatures (comprising the range of -25°C to 130°C).

Research efforts involved using the process guidelines to fabricate a well understood Switched Mode Power Supply (SMPS) circuit. This power supply circuit was selected since it has marketable applications. Optimizing the circuit design layout with consideration of thermal management issues, electrical properties, and materials issues, the power supply was constructed first on prefired Al₂O₃ and then on prefired AlN surfaces. The resulting circuits were tested and evaluated on a comparative basis.

Research showed that reductions of 57% in the overall area can be achieved, while reductions in overall volume can be as large as 83%. These gains resulted in an increase in EMI levels, however, these levels were largely due to the reduced size of the filter capacitance, which could be increased to trade a small increase in size for reduced EMI. Power factor for the miniaturized circuits (Avg.: 99.85%) was found to be better than the printed circuit board (98.5%), while efficiency was slightly lower for the miniaturized circuits with an average of 92.5%, compared to 95% for the PCB version. These electrical differences, particularly the reduced efficiency and the increased EMI were attributed to the change in the switching frequency from 50kHz to 250kHz and from the change in type of components; some of the SMT passive
components used did not meet the electrical characteristics of the through hole components that they replaced. For example, it was determined that the performance of the input capacitance used on the surface mount boards was greatly inferior to the element used in the PCB version.

In addition, the research demonstrated that passive components were feasible. Virtually all resistors, and a range of capacitances up to several tens of nanofarads with breakdown voltages up to 450 Volts are possible to achieve. The results also indicate that passive components are feasible on AlN surface as well, provided suitable passivation of the AlN surface is achieved, prior to depositing these layers.

Three generations of the boost circuit were formed using thick film technology. The first version of the boost circuit using thick film technology was generated using integrated passive capacitors and resistors. The capacitors were characterized over a range of temperatures and frequencies and found to be highly temperature dependent. The resistors were tested over a range of frequencies from DC up to 500kHz, and found to be essentially frequency independent. This first thick film version obtained a volume reduction of 84% and a surface area reduction of 61% over the original through hole PCB version.

The second thick film version used many components in smaller packages. Miniaturization was obtained from the package size reductions and by the use of integrated thick film resistors. An 88% volume reduction and a 69% surface area reduction were obtained in version #2.

The third thick film version consisted of a mother/daughter board combination. The daughter board consisted of the control circuitry for the boost circuit. Five integrated thick film resistors were included on the daughter board. Surface mount components were applied to both sides of the daughter board by using two different temperature solders and processing each side
separately. The mother board was developed so that a variety of substrates could be used: PCB, IMS, conventional thick film, or DBC technology.

As power supply miniaturization progresses, many of these methods can be implemented. The future of power supply miniaturization will bring smaller device packaging; for example, chip scale power packages and power flip chip packages. This will not only help to reduce the area and volume required by the switching components, but will also help to reduce the size of the control daughter boards. The use of microcontrollers in small packages along with the daughter board concept will facilitate miniaturization. The use of a microcontroller will allow one daughter board to be easily reconfigured for multiple applications. This reprogramming could complement the use of integrated passives; the program could be modified instead of tweaking a passive component.

With higher levels of passive component integration, the use of prefired AlN as a thick film substrate, and the control board concept, Switchmode Power Supply miniaturization can begin to close the ever increasing miniaturization gap between the circuits and their respective power supplies.
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Figure A.1. LabView™ Interface for HP4192a Impedance Meter
Figure A.2. LabView™ Graphical Program Frame for HP4192a Impedance Meter
Figure A.3. LabView™ Interface for HP4193 Impedance Meter
Appendix B
The permeability of the magnetic material can be determined using the Jacobial elliptic functions as formulated in [KAS92]. The following is a program, written in MathCAD®, uses these functions to calculate the permeability of a ferrite paste with spiral metal thick film conductors.

The inductance of each spiral is constant with frequency; therefore, this value was taken and used in the MathCAD® calculations to double check the permeability value. Equation (vii) is used to determine the total inductance. Lext1 is the external inductance of the inductor and is determined by equation (v) and Lmut1 represents the mutual inductance between the turns and is determined by equation (vi). Lo refers to the inductance of the spiral conductor on nonmagnetic material. The value of these inductances are then incorporated in equation (viii) to determine the value of alpha, which in turn yields the value of permeability using equations (ix) and (x).

The MathCAD® equations assume the following:

1. The spiral layer is a single layer.
2. The conductor is a round wire.
3. The spacing between turns in negligible.
4. The inductor has a large number of turns.
5. 0.2a < conductor width < 2a.
Permeability of Thick Film Printed Ferrite Determined by Method of Spiral Inductors

Conversion Factor

\[ \text{mil} := \frac{1}{1000} \text{ in} \]

Measured Metal Spiral Inductance

\[ L_0 := 1.86 \times 10^{-6} \text{ henry} \]

Measured Ferrite Spiral Inductance

\[ L_{\text{mag}} := 2.15 \times 10^{-6} \text{ henry} \]

Number of Turns

\[ N := 6 \]

Spiral Radii

\[ R_1 := 15 \text{ mil} \quad R_3 := 55 \text{ mil} \quad R_5 := 95 \text{ mil} \]

\[ R_2 := 35 \text{ mil} \quad R_4 := 75 \text{ mil} \quad R_6 := 115 \text{ mil} \]

Conductor Width

\[ W := 10 \text{ mil} \]

Thickness of Ferrite

\[ t_{\text{mag}} := 2 \text{ mil} \]

\[ \mu_0 := 4 \pi \times 10^{-7} \text{ henry per m} \]

\[ n := 1 \ldots N \quad m := 1 \ldots N - 1 \quad l := 1 \ldots 100 \]

\[ K_2_n := \sqrt[2]{\frac{R_n - \left( R_n - \frac{W}{2} \right)}{2R_n - \frac{W}{2} + (2l - t_{\text{mag}})^2}} \]

\[ K_3_n := \sqrt[2]{\frac{2R_n - \frac{W}{2}}{R_n - R_m + (2l - t_{\text{mag}})^2}} \]

\[ F(\phi, k) := \int_{0}^{\phi} \frac{1}{\sqrt{1 - k^2 \sin(\alpha)^2}} \, d\alpha \]

\[ E(\phi, k) := \int_{0}^{\phi} \sqrt{1 - k^2 \sin(\alpha)^2} \, d\alpha \]

Appendix B
\[ L_{ext} := \mu_0 \sum_{n=1}^{N} \sqrt{\left(2R_n - \frac{W}{2}\right)^2 + (2n-1)\ell_{mag}} \left[ 1 - \left(\frac{K_n}{2}\right)^2 \right] \left[ F\left(\frac{\pi}{2}, K_2 \right) - E\left(\frac{\pi}{2}, K_2 \right) \right] \] -----(v)

\[ L_{mut} := 2\mu_0 \sum_{n=1}^{N-1} \sum_{m=n+1}^{N} \sqrt{(R_n - R_m)^2 + (2n-1)\ell_{mag}} \left[ 1 - \left(\frac{K_n}{2}\right)^2 \right] \left[ F\left(\frac{\pi}{2}, K_3 \right) - E\left(\frac{\pi}{2}, K_3 \right) \right] \] -----(vi)

\[ L_q := L_{ext} + L_{mut} \] -----(vii)

\[ a := 1.50 \quad b := 0.02 \quad a^b = g \]

\[ \begin{array}{cccc}
F\left(\frac{\pi}{2}, K_2 \right) & E\left(\frac{\pi}{2}, K_2 \right) & F\left(\frac{\pi}{2}, K_3 \right) & E\left(\frac{\pi}{2}, K_3 \right) \\
1.573 & 1.569 & 1.583 & 1.557 \\
1.581 & 1.561 & 1.604 & 1.538 \\
1.597 & 1.545 & 1.626 & 1.519 \\
1.622 & 1.524 & 1.643 & 1.499 \\
1.648 & 1.499 & 1.673 & 1.478 \\
1.680 & 1.472 & 1.698 & 1.458 \\
\end{array} \]

\[ \text{Find } a^b \text{ when } \text{ans}=g. \]

\[ \text{ans}(a) := \left[ (1 + a \cdot b) \cdot \ell_{mag} + \sum_{n=1}^{10} (a \cdot b)^{2n+1} \right] - \sum_{m=1}^{10} (a \cdot b)^{2m-1} \] -----(viii)

Zero from Graph

\[ \alpha := 0.15 \]

\[ \text{ans}(a) \]

\[ \frac{\mu_0 - \mu_0^*}{\mu_0 + \mu_0^*} \] -----(ix)

\[ \mu_0 := (\alpha \cdot \mu_0 + \mu_0^*) \] -----(x)

\[ \mu_0 = 1.7 \times 10^{-6} \text{ kg m coul}^{-2} \]

\[ \mu_r := \frac{\mu_0}{\mu_0^*} \]

\[ \mu_r = 1.353 \] Permeability of Ferrite

Appendix B 232
\[ \mu_{\text{easy}} := \left( \frac{L_{\text{mag}}}{2L_0 - L_{\text{mag}}} \right) \quad (x_i) \quad \mu_{\text{easy}} = 1.369 \]
Boost Circuit Planar Transformer Calculations

Philips E22 Core Size and Plate - LTCC

Initial Design Values

L := 170\mu\text{H} \quad \text{Transformer Inductance}
Po := 60\text{-watt} \quad \text{Output Power}
\eta := .9 \quad \text{Power Supply Efficiency -- estimated}
Vacmin := 110\text{-volt} \quad \text{Boost Circuit Input Voltage}
D := .5 \quad \text{Boost Circuit Duty Cycle -- average}
Vo := 270\text{-volt} \quad \text{Boost Circuit Output Voltage}

Constants and Conversion Factors

\text{mil} := \frac{1}{1000} \quad \text{Conversion Factor}
\mu := 10^{-6} \quad \text{Conversion Factor}
\mu := 10^{-6} \quad \text{Conversion Factor}
\rho := 0.174\cdot10^{-7} \quad \text{Resistivity of Copper}

\mu_r := 1 \quad \text{Relative Permeability}
\mu_o := 4\pi\cdot10^{-7} \frac{\text{henry}}{\text{m}} \quad \text{Permeability of Free Space}

Power Supply Calculations for Boost Circuit

Io := \frac{Po}{Vo} \quad \text{Io = 0.222\text{-amp} \quad Boost Circuit Output Current}
Ipeak := \frac{2\sqrt{2\cdot Po}}{\eta\cdot Vacmin} \quad \text{Ipeak = 1.714\text{-amp} \quad Boost Circuit Peak Output Current}

ts := 20\cdot10^{-6}\text{-sec} \quad \text{Power Supply Switching Factor (MC34262 Chip)}

Lp := \frac{ts\cdot(\sqrt{2\cdot Vacmin})^2}{2\cdot Po} \quad \text{Lp = 3.63\cdot10^3 \mu\text{H} \quad Inductor Value by data sheet}
\[\text{ton} := \frac{2 \cdot P_o \cdot L}{\eta \cdot V_{\text{min}}^2}\]  
\text{toff} := \frac{\text{ton}}{V_o} \sqrt{2 \cdot V_{\text{min}} \sin \left(\frac{\pi}{2} \cdot \frac{1}{2}\right)} - 1
\]

\[\text{ton} = 1.87 \times 10^{-6} \text{ sec}\]
\[\text{toff} = 1.28 \times 10^{-6} \text{ sec}\]

\[F_s := \frac{1}{\text{ton} + \text{toff}}\]  
\[F_s = 316.34 \text{ kHz}\]  
\text{Boost Circuit Operating Frequency - approx}\n
\[\text{Irms} := \frac{1}{1 - D} \cdot \text{Io}\]  
\[\text{Irms} = 0.444 \text{ amp}\]  
\text{Boost Circuit RMS Output Current}\n
\[\text{Iwire} := \frac{P_o}{\eta \cdot V_{\text{min}}} + \frac{P_o}{V_o}\]  
\[\text{Iwire} = 0.828 \text{ amp}\]  
\text{Wire in inductor must support max average input current and output current.}\n
\[\text{Irms} := \text{Iwire}\]

**Wire Skin Depth Calculation**

\[D_{\text{skin}} := \sqrt{\frac{2 \cdot \rho}{2 \pi \cdot F_s \cdot \mu_0 \cdot \mu_r}}\]  
\[D_{\text{skin}} = 0.118 \text{ mm}\]  
\[D_{\text{skin}} = 4.647 \text{ mil}\]  
\text{Skin depth important at frequencies above about 10kHz.}\n
\[W_{\text{diam_skin}} := 2 \cdot D_{\text{skin}}\]  
\[W_{\text{diam_skin}} = 0.236 \text{ mm}\]  
\[W_{\text{diam_skin}} = 9.294 \text{ mil}\]  
\text{Cylindrical Wire Diameter maximum due to skin effect. If RMS current exceeds wire specification, use litz wire.}\n
\[W_{\text{area_skin}} := \pi \left(\frac{W_{\text{diam_skin}}}{2}\right)^2\]  
\[W_{\text{area_skin}} = 0.044 \text{ mm}^2\]  
\text{Wire crosssectional area}\n
**Rectangular conductor -- thick film calculations**

\[T_{\text{paste}} := 15 \text{ micron}\]  
\text{Trace Thickness < 2 x Dskin}\n\[D_{\text{skin}} = 118.037 \text{ micron}\]

\[W_{\text{space}} := 20 \text{ mil}\]  
\text{Trace Spacing -- 40 volts/mil breakdown}\n
\text{Appendix C}\n
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$P_d := 25.81 \cdot \frac{\text{watt}}{\text{in}^2}$ for Al2O3 design value (not Max) per MIL-H-38534
80 for BeO -- approx 70
25.81 max

$P_d = 0.08 \cdot \frac{\text{watt}}{\text{cm}^2}$

$\rho_{\text{metal}} := 0.02 \cdot \text{ohm}$
Dupont 6134 15microns thick

$\rho := \rho_{\text{metal}} \cdot \text{Tpaste}$
$\rho = 3 \cdot 10^{-7} \cdot \text{ohm} \cdot \text{m}$

$W_{\text{rect\_width\_min}} := \frac{\text{I}_{\text{rms}}}{\sqrt{P_d/\rho_{\text{metal}}}}$
$W_{\text{rect\_width\_min}} = 163.036 \cdot \text{mil}$
Rectangular conductor minimum width

$W_{\text{rect\_area}} := W_{\text{rect\_width\_min}} \cdot \text{Tpaste}$
Rectangular conductor cross-sectional area

$W_{\text{rect\_area}} = 0.062 \cdot \text{mm}^2$

$J_{\text{m\_rect}} := \frac{\text{I}_{\text{rms}}}{W_{\text{rect\_width\_min}} \cdot \text{Tpaste}}$
$J_{\text{m\_rect}} = 1.333 \cdot 10^3 \cdot \frac{\text{amp}}{\text{cm}^2}$
Current density in a rectangular wire

$J_{\text{m}} := J_{\text{m\_rect}}$

$W_{\text{width}} := W_{\text{rect\_width\_min}}$

$W_{\text{area}} := W_{\text{rect\_area}}$

**Transformer Size and Material Calculations**

**For 3F3 Ferrite Material**

$\mu_r := 1800$
Permiability from Data Sheet

$B_{\text{sat}} := 0.450 \cdot \text{tesla}$
Magnetic Saturation from Data Sheet

$P_v := 140 \frac{\text{kw}}{\text{m}^3}$
Core Power loss - estimated from data sheet graph based on frequency, temp, and Bm.
**Area Product**

\[ K_f := 0.5 \]

Winding Window Fill Factor -- The amount of the winding window that can be used. Insulation, bobbin area, gaps between bobbin and core, etc. All lower the % of winding area that is usable.

\[ B_m := \frac{B_{sat}}{2} \]

Engineering Design Factor -- 50% Reduction in Available Magnetism

\[ B_m = 0.225 \text{ tesla} \]

\[ A_{eff} := \frac{L_{peak} - I_{rms}}{K_f J_m B_m} \]

\[ A_{eff} = 160.904 \text{ mm}^4 \]

Area Product → \( A_e \cdot A_w \)

**Philips E22 Core Size and Plate**

\[ l_e := 26.1 \text{ mm} \]

Equivalent Magnetic Path Length Through Core

\[ A_e := 78.5 \text{ mm}^2 \]

Equivalent Core Cross Sectional Area

\[ A_w := 78.5 \text{ mm}^2 \]

Equivalent Cross Sectional Area of Winding Window

\[ V_e := 2040 \text{ mm}^3 \]

Equivalent Volume

\[ m := 4 \text{ gm} \]

Mass of core and plate

\[ C_{core} := 15.8 \text{ mm} \]

Core Dimentions

\[ D_{core} := 3.2 \text{ mm} \]

\[ E_{core} := 16.8 \text{ mm} \]

\[ F_{core} := 5 \text{ mm} \]

\[ \text{Gap}_\text{leg} := D_{core} \]

Length of core leg to be gapped

\[ L_{turn} := 2 \cdot (E_{core} + C_{core}) \]

\[ L_{turn} = 65.2 \text{ mm} \]

Average length of wire per turn

\[ W_{Wmax} := \frac{E_{core} - F_{core}}{2} \cdot 0.9 \]

\[ W_{Wmax} = 5.31 \text{ mm} \]

Max wire winding width -- 90%

\[ W_{Hmax} := D_{core} \cdot 0.9 \]

\[ W_{Hmax} = 2.88 \text{ mm} \]

Max wire winding hieght -- 90%

\[ A_e \cdot A_w = 6.162 \times 10^3 \text{ mm}^4 \]

\[ A_{eff} = 160.904 \text{ mm}^4 \]

\( A_{eff} < A_e \cdot A_w \) Core Must have this property

*Appendix C*
\[ N := \frac{I_{\text{peak}}}{B_{\text{m}} A e} \quad N = 16.499 \]

Number of Windings required

\[ g := \frac{\mu_0 \cdot A e - N^2}{L} - \frac{l e}{\mu e} \quad g = 0.143 \text{mm} \]

\[ g = 5.648 \text{mil} \]

Air Gap Required to Minimise Core Saturation. Also want gap < 50 mils to minimise EMI.

\[ g = 0.143 \text{mm} \quad \sqrt{\frac{A e}{10}} = 0.886 \text{mm} \]

\[ g < \sqrt{A e}/10 \quad \text{To keep fringing to a minimum so it wont effect the inductance value} \]

**Calculate Fringing Effects**

\[ F := 1 + \frac{g}{A e} \ln \left( \frac{2 \cdot \text{Gap}_{\text{leg}}}{g} \right) \text{mm} \quad F = 1.007 \]

Fringing flux factor. Inductance is increased by this factor.

\[ N_{\text{fringe}} := \frac{L}{F} \frac{I_{\text{peak}}}{B_{\text{m}} A e} \quad N_{\text{fringe}} = 16.385 \]

Number of Windings required taking into account fringing.

\[ N := \text{ceil}(N_{\text{fringe}}) \quad N = 17 \]

Number of turns - rounded up

**Determine the Percentage of the Winding Window Used**

\[ T_{\text{tcc}} := 3 \text{-mil} \]

Thickness of LTCC

\[ N_{\text{turns}_{\text{layer max}}} := \text{floor} \left( \frac{W_{\text{max}} - \text{Wspace}}{W_{\text{width}} + \text{Wspace}} \right) \quad N_{\text{turns}_{\text{layer max}}} = 1 \]

Maximum number of turns per layer - rounded down

\[ N_{\text{layer max}} := \text{floor} \left( \frac{W_{\text{Hmax}} - T_{\text{tcc}}}{(T_{\text{paste}} + T_{\text{tcc}})} \right) \quad N_{\text{layer max}} = 30 \]

Maximum layers - rounded down

\[ N_{\text{turns max}} := N_{\text{turns}_{\text{layer max}}} \cdot N_{\text{layer max}} \quad N_{\text{turns max}} = 30 \]

Maximum number of turns

\[ N_{\text{turns max}} = 30 \quad N = 17 \quad N_{\text{turns max}} < N \]

\[ \text{Layers} := \text{ceil} \left( \frac{N}{N_{\text{turns}_{\text{layer max}}}} \right) \quad \text{Layers} = 17 \]

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Calculate Losses

\[ R := \frac{L_{\text{turn}} \cdot N \cdot \rho}{W_{\text{area}}} \quad R = 5.353 \text{\ ohm} \quad \text{Wire resistance} \]

\[ Q := \frac{2\pi \cdot F_s \cdot L}{R} \quad Q = 63.121 \quad \text{Q if inductor} \]

\[ P_w := \text{Irms}^2 \cdot R \quad P_w = 3.673 \text{\ watt} \quad \text{Power loss in wire} \]

\[ B_{\text{m\_max\_approx}} := \frac{\mu_0 \cdot N \cdot I_{\text{peak}}}{g + \frac{L e}{\mu e}} \quad B_{\text{m\_max\_approx}} = 0.232 \text{\ tesla} \quad \text{Maximum Flux density} \]

\[ B_{\text{m\_avg\_approx}} := \frac{L \cdot I_{\text{peak}} \cdot \text{Irms}}{K_f J_m A_e \cdot A_w} \quad B_{\text{m\_avg\_approx}} = 5.875 \times 10^{-3} \text{\ tesla} \quad \text{Average Flux Density} \]

\[ P_{\text{core}} := P_v \cdot V_e \quad P_{\text{core}} = 0.286 \text{\ watt} \]

\[ P_{\text{total}} := P_{\text{core}} + P_w \quad P_{\text{total}} = 3.958 \text{\ watt} \quad \text{Total Inductor loss} \]
Boost Circuit Planar Transformer Calculations

Philips E32 Core Size and Plate- LTCC

Initial Design Values

L := 170\mu H

Transformer Inductance

Po := 60-watt

Output Power

\( \eta := 0.9 \)

Power Supply Efficiency -- estimated

Vacmin := 110-volt

Boost Circuit Input Voltage

D := 0.5

Boost Circuit Duty Cycle -- average

Vo := 270-volt

Boost Circuit Output Voltage

Constants and Conversion Factors

\text{mil} := \frac{1}{1000}\text{in}

Conversion Factor

\text{micron} := 10^{-6}\text{m}

Conversion Factor

\rho := 0.174\times10^{-7}\text{ohm-m}

Resistivity of Copper

\mu r := 1

Relative Permeability

\mu o := 4\pi \times10^{-7}\frac{\text{henry}}{\text{m}}

Permeability of Free Space

Power Supply Calculations for Boost Circuit

\( I_0 := \frac{P_o}{V_o} \)

\( I_0 = 0.222\text{amp} \)

Boost Circuit Output Current

\( I_{peak} := \frac{2\sqrt{2\cdot P_o}}{\eta \cdot V_{\text{acmin}}} \)

\( I_{peak} = 1.714\text{amp} \)

Boost Circuit Peak Output Current

\( ts := 20\times10^{-6}\text{sec} \)

Power Supply Switching Factor (MC34262 Chip)

\( L_p := \frac{ts \cdot (\sqrt{2} \cdot V_{\text{acmin}})^2}{2 \cdot P_o} \)

\( L_p = 3.6\times10^3\ \mu\text{H} \)

Inductor Value by data sheet

Appendix D
\[ t_{on} := \frac{2 \cdot P_o \cdot L}{\eta \cdot V_{acmin}^2} \]
\[ t_{off} := \frac{t_{on}}{V_o} \cdot \sqrt{2 \cdot V_{acmin} \cdot \sin\left(\frac{\pi}{22}\right)} \]
\[ F_s := \frac{1}{t_{on} + t_{off}} \]

\[ t_{on} = 1.87 \times 10^{-6} \text{ sec} \]
\[ t_{off} = 1.28 \times 10^{-6} \text{ sec} \]
\[ F_s = 316.34 \text{ kHz} \]

\[ I_{rms} := \frac{1}{1 - D} \cdot I_o \]
\[ I_{rms} = 0.444 \text{ amp} \]

\[ I_{wire} := \frac{P_o}{\eta \cdot V_{acmin}} + \frac{P_o}{V_o} \]
\[ I_{wire} = 0.828 \text{ amp} \]

\[ I_{rms} = I_{wire} \]

**Wire Skin Depth Calculation**

\[ D_{skin} := \sqrt{\frac{2 \cdot \rho}{2 \pi \cdot F_s \cdot \mu_o \cdot \mu_r}} \]
\[ D_{skin} = 0.118 \text{ mm} \]
\[ D_{skin} = 4.647 \text{ mil} \]

\[ W_{diam\_skin} := 2 \cdot D_{skin} \]
\[ W_{diam\_skin} = 0.236 \text{ mm} \]
\[ W_{diam\_skin} = 9.294 \text{ mil} \]

\[ W_{area\_skin} := \pi \cdot \left(\frac{W_{diam\_skin}}{2}\right)^2 \]
\[ W_{area\_skin} = 0.044 \text{ mm}^2 \]

**Skin depth important at frequencies above about 10kHz.**

**Cylindrical Wire Diameter maximum due to skin effect. If RMS current exceeds wire specification, use litz wire.**

**Rectangular conductor -- thick film calculations**

\[ T_{paste} := 15 \text{ micron} \]
\[ T_{paste} < 2 \times D_{skin} \]
\[ D_{skin} = 118.037 \text{ micron} \]

\[ W_{space} := 20 \text{ mil} \]
\[ W_{space} < 40 \text{ volts/mil breakdown} \]

*Appendix D* 243
Pd := 25.81 \frac{\text{watt}}{\text{in}^2} \quad \text{for Al}_2\text{O}_3 \text{ design value (not Max) per MIL-H-38534}

80 for BeO -- approx 70
25.81 max

Pd := 0.028 \frac{\text{watt}}{\text{cm}^2}

\rho_{\text{metal}} := 0.02 \text{ ohm}

Dupont 6134 15microns thick

\rho := \rho_{\text{metal}} \cdot \text{Tpaste}

\rho = 3 \cdot 10^{-7} \text{ ohm} \cdot \text{m}

W_{\text{rect\_width\_min}} := \frac{\text{I}_{\text{rms}}}{\sqrt{\frac{\text{Pd}}{\rho_{\text{metal}}}}}

W_{\text{rect\_width\_min}} = 275.582\text{mil}

\text{Rectangular conductor minimum width}

W_{\text{rect\_area}} := W_{\text{rect\_width\_min}} \cdot \text{Tpaste}

\text{Rectangular conductor cross-sectional area}

W_{\text{rect\_area}} = 0.105 \text{mm}^2

J_{\text{m\_rect}} := \frac{\text{I}_{\text{rms}}}{W_{\text{rect\_width\_min}} \cdot \text{Tpaste}}

J_{\text{m\_rect}} = 788.866\text{amp/cm}^2

\text{Current density in a rectangular wire}

J_{\text{m}} := J_{\text{m\_rect}}

W_{\text{width}} := W_{\text{rect\_width\_min}}

W_{\text{area}} := W_{\text{rect\_area}}

\textbf{Transformer Size and Material Calculations}

\textbf{For 3F3 Ferrite Material}

\mu_e := 1800 \quad \text{Permiability from Data Sheet}

\text{Bsat} := 0.450\text{tesla} \quad \text{Magnetic Saturation from Data Sheet}

P_v := 140\frac{\text{kW}}{\text{m}^3} \quad \text{Core Power loss - estimated from data sheet graph based on frequency, temp, and Bm.}

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Area Product

\[ K_f := 0.5 \]

Winding Window Fill Factor -- The amount of the winding window that can be used. Insulation, bobbin area, gaps between bobbin and core, etc. All lower the % of winding area that is usable.

\[ B_m := \frac{B_{sat}}{2} \]

Engineering Design Factor -- 50% Reduction in Available Magnitism

\[ B_m = 0.225 \text{tesla} \]

\[ A_{eff} := \frac{I_{peak} \cdot I_{rms}}{K_f \cdot J_m \cdot B_m} \]

\[ A_{eff} = 271.978 \text{mm}^4 \]

Area Product -> \( A_e \cdot A_w \)

Philips E32 Core Size and Plate

\[ l_e := 35.9 \text{mm} \]

Equivalent Magnetic Path Length Through Core

\[ A_e := 129 \text{mm}^2 \]

Equivalent Core Cross Sectional Area

\[ A_w := 129 \text{mm}^2 \]

Equivalent Cross Sectional Area of Winding Window

\[ V_e := 4560 \text{mm}^3 \]

Equivalent Volume

\[ m := 10 \text{gm} \]

Mass of core and plate

\[ C_{core} := 20.32 \text{mm} \]

\[ D_{core} := 3.18 \text{mm} \]

Core Dimentions

\[ E_{core} := 24.9 \text{mm} \]

\[ F_{core} := 6.35 \text{mm} \]

\[ \text{Gap}_\text{leg} := D_{core} \]

Length of core leg to be gapped

\[ L_{turn} := 2 \cdot (E_{core} + C_{core}) \]

\[ L_{turn} = 90.44 \text{mm} \]

Average length of wire per turn

\[ W_{W_{max}} := \frac{E_{core} - F_{core} + 0.9}{2} \]

\[ W_{W_{max}} = 8.347 \text{mm} \]

Max wire winding width -- 90%

\[ W_{H_{max}} := D_{core} \cdot 0.9 \]

\[ W_{H_{max}} = 2.862 \text{mm} \]

Max wire winding hieght -- 90%

\[ A_e \cdot A_w = 1.66 \times 10^4 \text{mm}^4 \]

\[ A_{eff} = 271.978 \text{mm}^4 \]

\[ A_{eff}<A_e \cdot A_w \text{ Core Must have this property} \]

Appendix D
\[ N := \frac{I_{\text{peak}}}{B_m A_e} \quad N = 10.04 \quad \text{Number of Windings required} \]

\[ g := \frac{\mu_0 A_e N^2}{L} - \frac{1e}{\mu e} \quad g = 0.076\text{mm} \]

\[ g = 2.999\text{mil} \quad \text{Air Gap Required to Minimise Core Saturation.} \]
\[ \text{Also want gap < 50 mils to minimise EMI.} \]

\[ g = 0.076\text{mm} \quad \sqrt{\frac{A_e}{10}} = 1.136\text{mm} \]

\[ g < \sqrt{A_e}/10 \quad \text{To keep fringing to a minimum so it wont effect the inductance value} \]

**Calculate Fringing Effects**

\[ F := 1 + \frac{g}{A_e} \ln \left( \frac{2 \cdot \text{Gap}_\text{leg}}{g} \right) \text{mm} \quad F = 1.003 \quad \text{Fringing flux factor. Inductance is increased by this factor.} \]

\[ N_{\text{fringe}} := \frac{L}{F} \frac{I_{\text{peak}}}{B_m A_e} \quad N_{\text{fringe}} = 10.014 \quad \text{Number of Windings required taking into account fringing.} \]

\[ N := \text{ceil}(N_{\text{fringe}}) \quad N = 11 \quad \text{Number of turns - rounded up} \]

**Determine the Percentage of the Winding Window Used**

\[ \text{T}_{\text{ltcc}} := 3\text{-mil} \quad \text{Thickness of LTCC} \]

\[ N_{\text{turns}_\text{layer\_max}} := \left\lfloor \frac{W_{\text{max}} - \text{Wspace}}{W_{\text{width}} + \text{Wspace}} \right\rfloor \quad N_{\text{turns}_\text{layer\_max}} = 1 \quad \text{Maximum number of turns per layer - rounded down} \]

\[ N_{\text{layer\_max}} := \left\lfloor \frac{W_{\text{Hmax}} - \text{T}_{\text{ltcc}}}{\text{T}_{\text{paste}} + \text{T}_{\text{ltcc}}} \right\rfloor \quad N_{\text{layer\_max}} = 30 \quad \text{Maximum layers - rounded down} \]

\[ N_{\text{turns\_max}} := N_{\text{turns}_\text{layer\_max}} \cdot N_{\text{layer\_max}} \quad N_{\text{turns\_max}} = 30 \quad \text{Maximum number of turns} \]

\[ N_{\text{turns\_max}} = 30 \quad N = 11 \quad N_{\text{turns\_max}} < N \]

\[ \text{Layers} := \text{ceil} \left( \frac{N}{N_{\text{turns}_\text{layer\_max}}} \right) \quad \text{Layers} = 11 \]
Calculate Losses

\[ R := \frac{N \cdot \rho}{W_{\text{area}}} \quad R = 2.842 \text{ ohm} \quad \text{Wire resistance} \]

\[ Q := \frac{2\pi \cdot F_s \cdot L}{R} \quad Q = 118.873 \quad \text{Q if inductor} \]

\[ P_w := I_{\text{rms}}^2 \cdot R \quad P_w = 1.95 \text{ watt} \quad \text{Power loss in wire} \]

\[ B_{m_{\text{max approx}}} := \frac{\mu_0 \cdot N \cdot I_{\text{peak}}}{g + \frac{le}{\mu e}} \quad B_{m_{\text{max approx}}} = 0.247 \text{ tesla} \quad \text{Maximum Flux density} \]

\[ B_{m_{\text{avg approx}}} := \frac{L \cdot I_{\text{peak}} \cdot I_{\text{rms}}}{K_f \cdot J_m \cdot A_e \cdot A_w} \quad B_{m_{\text{avg approx}}} = 3.67 \times 10^{-3} \text{ tesla} \quad \text{Average Flux Density} \]

\[ P_{\text{core}} := P_v \cdot V_e \quad P_{\text{core}} = 0.638 \text{ watt} \]

\[ P_{\text{total}} := P_{\text{core}} + P_w \quad P_{\text{total}} = 2.588 \text{ watt} \quad \text{Total Inductor loss} \]
Vita

Richard W. Hoagland earned a Bachelors of Science in Electrical Engineering from Clemson University in 1991, and a Masters of Science in Electrical Engineering from Virginia Tech in 1993. As a Ph.D. candidate in Electrical Engineering at Virginia Tech, he held a Graduate Project Assistant (GPA) position with The Microelectronics Laboratories. Richard is the recipient of the IMAPS (ISHM) Educational Foundation grant for 1997 and 1998. Research interests include switched mode power supply miniaturization, analog and digital electronic design, passive component characterization, and integration of passive components on prefired aluminum nitride.