VT-STAR – Design and implementation of a test bed for differential space-time block coding and MIMO channel measurements

by

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Abstract

Next generation wireless communications require transmission of reliable high data rate services. Second generation wireless communications systems use single-input multiple-output (SIMO) channel in the reverse link, meaning one transmit antenna at the user terminal and multiple receive antennas at the base station. Recently, information theoretic research has shown an enormous potential growth in the capacity of wireless systems by using multiple antenna arrays at both ends of the link. Space-time coding exploits the spatial-temporal diversity provided by the multiple input multiple output (MIMO) channels, significantly increasing both system capacity and the reliability of the wireless link. The Virginia Tech Space-Time Advanced Radio (VT-STAR) system presents a test bed to demonstrate the capabilities of space-time coding techniques in real-time. Core algorithms are implemented on Texas Instruments TMS320C67 Evaluation Modules (EVM). The radio frequency subsystem is composed of multi-channel transmitter and receiver chains implemented in hardware for over the air transmission. The capabilities of the MIMO channel are demonstrated in a non-line of sight (NLOS) indoor environment. Also to characterize the capacity gains in an indoor environment this test bed was modified to take channel measurements. This thesis reports the system design of VT-STAR and the channel capacity gains observed in an indoor environment for MIMO channels.
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Chapter 1

1 Introduction

Evolution of wireless communication technology is driving towards supporting internet and multimedia applications. This requires developing high data rate communication over wireless channels. Use of antenna arrays in smart antenna applications has been studied in the past decade to improve capacity and range of a cellular system. Antenna arrays are usually implemented at the base station and use signal processing techniques to reduce interference. More recently use of multiple input and multiple output (MIMO) systems that is the use of multiple antennas at the transmitter as well as the receiver, was proposed which promises manifold increase in Shannon’s capacity of systems compared to a single antenna system. These include two revolutionary techniques, one based on spatial multiplexing proposed by Foschini in 1996 which tries to improve the throughput (bits/sec) and space-time coding by Tarokh in 1998 which tries to improve the bit error rate performance. The underlying assumption for such improvement is the presence of independent fading channels.

This potential in capacity improvement has motivated the research community to take channel measurements to characterize MIMO channels under indoor and outdoor wireless environments. Progress in MIMO research poses interesting challenges in the areas of modeling of mobile MIMO wireless channels, signal processing for transmit and receive algorithms, and the design of the wireless fixed or mobile networks that will incorporate MIMO links. The channel models assumed by Foschini and others are mostly unrealistic. The evaluation of channel capacity gains, which take into account the radio propagation environments with various scattering density is the key to understand the real gains of MIMO systems.

1.1 Motivation and Objectives
The basic motivation behind this thesis is to build a software programmable MIMO transceiver testbed. The test bed should help implement real time space time block coding algorithm for testing over the air. It is flexible for taking MIMO channel measurements to evaluate the achievable channel capacity gains for actual MIMO indoor propagation channels. There are
several MIMO systems under development in many universities. Most of the systems use channel sounding methods to characterize the MIMO channel. In the Virginia Tech Space-Time Advanced Radio (VT-STAR) system the orthogonal code design of space time block coding is exploited to perform channel measurements. Also building the VT-STAR system is a unique effort to characterize the performance of differential space time coding with timing and synchronization constraints as reflective of practical prototype systems.

1.2 Outline
There are two parts to this thesis; the first involves building a testbed to implement real time differential space time block coding scheme for a 2x2 (2 element receive and 2 element transmit) MIMO system and the second involves using the testbed to perform channel measurements for characterizing the achievable indoor MIMO channel capacity gains. This thesis comprises of seven chapters. The second chapter builds the theoretical background on coherent and differential space-time block coding schemes and relevance of choosing the differential scheme for the test bed. Third chapter deals with the making of VT-STAR test bed. It explains the various sub components used for the transmitter and receiver system design. The fourth chapter explains the software-hardware co-design for developing the space-time coding algorithm. Chapter five gives a literature review of the MIMO channel measurements performed and discusses the results published. In chapter six the modification of VT-STAR testbed for channel measurement is explained. The measurement campaign to characterize the indoor MIMO wireless channel and the corresponding results are discussed. Finally conclusions from the work performed and future directions for further research in MIMO with the testbed are given in Chapter seven.
Chapter 2

2 Evolution of MIMO

2.1 Introduction

Digital communication using multiple-input multiple-output (MIMO) wireless links is emerging as one of the most promising research areas in wireless communications. A MIMO wireless digital communication system uses multiple antenna elements (MEAs) both at the transmitter as well as the receiver. The signal processing at the transmitter and receiver is done in such a way that the bit error rate (BER) or the capacity (Bit/Sec/Hz) of the communication system is improved.

In most scattering environments, antenna diversity is a widely applied technique for reducing the effect of multipath fading [Jak74]. The classical approach is to use multiple antennas at the receiver and perform combining or selection and switching in order to improve the quality of the received signal. The problem with using the receive diversity approach at the mobile terminal is the cost, size, and power. The use of multiple antennas and radio frequency (RF) chains makes these terminals larger and expensive. As a result, receive diversity techniques have mostly been applied to base stations.

Some interesting transmit diversity techniques were suggested in the early nineties. A delay diversity scheme was proposed by Wittneben [Wit91], [Wit93] for base station simulcasting. Later a similar scheme was suggested by Seshadri and Winters in [Sesh93], [Win94], for a single base station in which copies of the same symbol are transmitted through multiple antennas at different times, hence creating artificial multipath. A maximum likelihood sequence estimator (MLSE) or a minimum mean squared error (MMSE) equalizer is then used to resolve multipath distortion and obtain diversity gain.

More recently information theoretic aspects of MIMO channels as compared with the Shannon capacity for Single-Input Single Output (SISO) channels were investigated by Foschini of Lucent Technologies [Fos96] and by Telatar [Tel95]. It was shown that the capacity grows
approximately linearly with the number of transmit antennas as long as the number of receive antennas is greater than or equal to the number of transmit antennas. This has led to the development of many schemes that utilize transmit-receive diversity schemes, coding schemes and advanced signal processing schemes to achieve the theoretical capacity of MIMO channels. Some of the major approaches are summarized below.

1. **Bell Labs Layered Space-Time Architecture, proposed by Foschini [Fos98].** The underlying signal processing at the receiver is based on multi-user detection techniques such that the sub-channels arriving from different transmit antennas are decoupled successively. Two main BLAST schemes were proposed in the literature. The V-BLAST scheme known as the vertical BLAST corresponds to a vertical mapping of symbols onto the space domain such that all the spatially mapped symbols are transmitted simultaneously. That is, each transmitter operates as a conventional QAM transmitter. The second scheme, known as D-BLAST, is a diagonally layered space time architecture, in which each incoming bit stream is converted to sub-streams using parallel constituent coding and mapped diagonally in space-time. The receiver follows the same principle as general BLAST to get back the sub-streams.

2. **Space-Time Trellis Codes (STTC), proposed by Tarokh et. al.[Tar98], [Nag98].** Here symbols are encoded according to the antennas through which they are simultaneously transmitted and are decoded using a maximum likelihood decoder. This scheme is very effective, as it combines the benefits of forward error correction (FEC) coding and diversity transmission to provide considerable performance gains. The cost for this scheme is additional processing, which increases exponentially as a function of bandwidth efficiency (bits/s/Hz) and the required diversity order.

3. **Space-Time Block Codes (STBC), proposed by Alamouti [Ala98].** This scheme was proposed in the hope of reducing the exponential decoder complexity of STTC scheme for the case of a 2x2 MIMO channel. This scheme was expanded by Tarokh et.al. [Tar22] for an arbitrary number of array elements to form the class of Space-Time Block Codes (STBC). These codes achieve the same diversity advantage of Maximal Ratio Receive
Combining (MRRC). STBC are defined by a mapping operation of a block of input symbols into space and time domains, creating orthogonal sequences that are transmitted from different transmit antennas. The receiver is composed of channel estimation, combining procedure (in both time and space) and Maximum Likelihood (ML) detection rule. It is assumed that the channel coherence time is greater than the length of a block. The STBC decoder has a remarkably simple structure and yet achieves the same diversity advantage as that of MRRC.

This thesis focuses on implementation aspects of the simple STBC approach for the 2x2 MIMO case. Hence we next describe the theoretical aspects simple STBC scheme for a 2x2 system in detail and a variation of the scheme called differential-STBC which was chosen for implementation to overcome stringent synchronization requirements of coherent STBC.

### 2.2 Theoretical Aspects of Space-Time Block Coding (STBC)

To understand the advantages of STBC scheme with respect to MRRC scheme, a brief explanation of the Maximal Ratio Receive Combining scheme is presented here.

#### 2.2.1 Maximal Ratio Receive Combining

Consider a 1x2 MIMO transceiver system shown in Figure 2.1. In this scheme the symbol $s_0$ transmitted at any given time is received at both the antennas after going through two different channels. The channel between transmit antenna one and receive antenna one is represented by $h_{11}$ and between transmit antenna one and receive antenna two is represented by $h_{12}$, where,

$$h_{11} = \alpha_{11} e^{j\theta_{11}} \quad (2.1)$$
$$h_{12} = \alpha_{12} e^{j\theta_{12}} \quad (2.2)$$

Here $\alpha_{11}$ and $\alpha_{12}$ are magnitudes of the distortion caused by fading which has Rayleigh distribution. $\theta_{11}$ and $\theta_{12}$ are phase distortion due to fading which is assumed to be uniformly distributed between zero to 360 degrees. Noise and interference is added at the receiver antennas as given by $n_1$ and $n_2$ respectively for antenna 1 and 2, which are Gaussian distributed.
Figure 2.1 Maximal ratio receiver combining

\[ r_1 = s_0 h_{11} + n_1 \]  

(2.3)

\[ r_2 = s_0 h_{12} + n_2 \]  

(2.4)

At the receiver each antenna has a channel estimator which estimates the values of \( h_{11} \) and \( h_{21} \) (\( \hat{h}_{11} \) and \( \hat{h}_{21} \)) to be used for MRRC scheme which is given by

\[ \tilde{s}_0 = \hat{h}_{11} r_1 + \hat{h}_{21}^* r_2 \]  

(2.5)

Maximum likelihood detection follows the combining operation to determine the signal transmitted where a decision is made on symbol \( s_i \) depending on equation 2.6 where,

\[ i = \min_k \left[ d^2 (\tilde{s}_0, s_k) \right] \]  

(2.6)

And \( d^2 (x, y) \) is the Euclidean distance between signals \( x \) and \( y \).
The MRRC scheme for 1x2 system performs better than a 1x1 system when the signal to noise ratio is high.

2.2.2 Simple Coherent Space-Time Block Coding (C-STBC)
Space-Time Block Coding is a simple transmit diversity scheme that achieves the same diversity advantage of Maximal Ratio Receive Combining. Figure 2.2 shows a 2x1 MIMO system which uses space-time block coding on the sequence to be transmitted. The receiver uses a combining scheme followed by maximum likelihood detection. This is described in detail next.

![Diagram of space-time block coding for 2x1 MIMO channel]

The transmitted sequence of symbols is coded in such a way as to form a space time block as shown in Figure 2.3. At time t symbol $s_0$ is transmitted from antenna one and $s_1$ is transmitted from antenna two. In the next symbol duration $-s_1^*$ is transmitted from antenna one and $s_0^*$ is transmitted from antenna two. It can be seen that the space-time block coding matrix is orthogonal both in space and time for the symbol duration T. The matrix representation of such a coding scheme is named as the $G_2$ scheme [Tar00].
The channel between the first transmit antenna and the first receive antenna is represented by \( h_{11} \) and between the second transmit antenna two and the first receive antenna one is represented by \( h_{21} \) where,

\[
\begin{array}{|c|c|c|}
\hline
\text{Time} & \text{Transmit Antenna 1} & \text{Transmit Antenna 2} \\
\hline
\text{Time } t & s_0 & s_1^* \\
\hline
\text{Time } t+T & -s_1^* & s_0^* \\
\hline
\end{array}
\]

**Figure 2.3** Space-time block coding on source symbol sequence

\[
h_{11}(t) = \alpha_{11}e^{j\theta_{11}} \quad (2.7)
\]

\[
h_{21}(t) = \alpha_{21}e^{j\theta_{21}} \quad (2.8)
\]

Here the channel is assumed to be static across two consecutive symbols. Therefore the received signal can be expressed as

\[
r_1 = r(t) = s_0h_{11} + s_1h_{21} + n_1 \quad (2.9)
\]

\[
r_2 = r(t+T) = -s_1^*h_{11} + s_0^*h_{21} + n_2 \quad (2.10)
\]

where, \( n_1 \) and \( n_2 \) are complex random variables representing noise and interference.

For the combining process at the receiver, the signal received is assumed to be coherent. Also assumed is the fact that channel estimation is perfect. Hence the combining scheme used is given by

\[
\tilde{s}_0 = \hat{h}_{11}^*s_1 + \hat{h}_{21}^*r_2 \quad (2.11)
\]
\[ \hat{s}_i = \hat{h}_{21}^* r_1 - \hat{h}_1^* r_2^* \]  
\hspace{1cm} (2.12)  
i.e.
\[ \hat{s}_0 = \alpha_{11}^2 s_0 + \alpha_{21}^2 s_0 + n_1 \hat{h}_{11}^* + n_2 \hat{h}_{21}^* \]  
\hspace{1cm} (2.13)  
\[ \hat{s}_1 = \alpha_{21}^2 s_1 + \alpha_{11}^2 s_1 + n_1 \hat{h}_{21}^* - n_2 \hat{h}_{11}^* \]  
\hspace{1cm} (2.14)  

It can be seen that the first two terms are magnitudes of the fade coefficients and the last two terms are noise terms which are small.

Maximum likelihood detection follows the combining scheme to determine the signals \( s_0 \) and \( s_1 \) transmitted based on equation 2.6. It can be seen that the combining scheme is different from the MRRC scheme but the diversity advantage remains the same. Now we expand the scheme to a 2x2 MIMO system as shown in Figure 2.4. In this figure the received signals at time \( t \) are given by equation 2.13 and 2.14.

![Figure 2.4 Block diagram of 2x2 MIMO STBC scheme](image-url)
\( r_1 = s_1 h_1 + s_2 h_2 + n_1 \) (at receive antenna one) \hspace{1cm} (2.15)

\( r_3 = s_1 h_3 + s_2 h_4 + n_3 \) (at receive antenna two) \hspace{1cm} (2.16)

The signals received at time \( t + T \) are given by equation 2.15 and 2.16.

\( r_2 = -s_1^* h_1 + s_2^* h_2 + n_2 \) (at receive antenna one) \hspace{1cm} (2.17)

\( r_4 = -s_1^* h_3 + s_2^* h_4 + n_4 \) (at receive antenna two) \hspace{1cm} (2.18)

\( n_1, n_2, n_3 \) and \( n_4 \) are complex Gaussian random variables representing noise and interference.

Now the combining scheme for the received signals to achieve the diversity advantage is given by

\( \hat{s}_0 = \hat{h}_1^* r_1 + \hat{h}_2^* r_2 + \hat{h}_3^* r_3 + \hat{h}_4^* r_4 \) \hspace{1cm} (2.19)

\( \tilde{s}_1 = \hat{h}_1^* r_1 - \hat{h}_2^* r_2 + \hat{h}_3^* r_3 - \hat{h}_4^* r_4 \) \hspace{1cm} (2.20)

i.e.

\( \tilde{s}_0 = (\alpha_{11}^2 + \alpha_{21}^2 + \alpha_{12}^2 + \alpha_{22}^2) s_0 + n_1 \hat{h}_{11}^* + n_2 \hat{h}_{12}^* + n_1^* \hat{h}_{21} + n_2^* \hat{h}_{22} \) \hspace{1cm} (2.21)

\( \tilde{s}_1 = (\alpha_{11}^2 + \alpha_{12}^2 + \alpha_{21}^2 + \alpha_{22}^2) s_1 + n_1 \hat{h}_{21}^* + n_2 \hat{h}_{22}^* - n_1^* \hat{h}_{11} - n_2^* \hat{h}_{12} \) \hspace{1cm} (2.22)

The output of the combining scheme is fed to the maximum likelihood detector where a decision is made based on equation 2.6. The advantage of using a 2x2 system is that the diversity order has increased by 4.

Figure 2.5 shows the simulation results for the bit error rate (BER) performance of the coherent STBC scheme compared to MRRC scheme. In these simulations the total transmitted power of transmit diversity case with STBC is assumed to be equal to the transmitted power of single element transmit power in the MRRC case. Hence there is a degradation in performance in the case of transmit diversity when compared to the same order of receive diversity with MRRC, as the received signal power from each transmit antenna in MRRC scheme is more than the transmit diversity case. The channels for the MIMO case are assumed to be mutually uncorrelated undergoing Rayleigh fading. Also the perfect knowledge of channel state information (CSI) at the receiver is assumed.
The performance of coherent STBC scheme depends on the perfect channel estimation and carrier recovery. This has led to the formulation of a differential STBC scheme which will be discussed next and is the algorithm used for implementation on hardware.

### 2.3 Differential Space-Time Block Coding (D-STBC)

C-STBC scheme places stringent requirements of accurate carrier recovery and channel state information at the receiver to compensate for instantaneous phase and allow for optimal detection. Carrier recovery and channel estimation can be performed with transmission of pilot symbols, but introduces additional overhead and complexity to the system. Instantaneous tracking of phase and channel state information is therefore a challenging task in time varying channels. Differential STBC was proposed in [Tar00], which uses the principles of differential modulation to avoid the overhead of tracking the phase and channel estimation. This is one of

![Figure 2.5 BER Vs SNR of MRRC and STBC schemes](image.png)
prime reasons for using DSTBC scheme to develop the VT-STAR test bed system. From a performance perspective any differential demodulation scheme has approximately 3dB degradation than coherent scheme. This is due to the fact that demodulation is performed by using the previously received symbol as a reference signal to the current symbol. The demodulator hence extracts the difference between consecutive phases to yield the information sequence which can lead to error propagation.

Figure 2.6 shows the block diagram for the D-STBC encoding scheme at the transmitter.

![Figure 2.6 D-STBC encoding](image)

The input bits are mapped to an M-ary PSK symbols given by equation 2.23.

\[
A = \left\{ \frac{1}{\sqrt{2}} \exp \left( \frac{i2\pi k}{M} \right) \right\}
\]  

(2.23)

A pair of M-ary symbols say \((a_1, a_2)\) are chosen as reference symbols. The M-mapping process uses these reference symbols and the two consecutive symbols \((a_3, a_4)\) input to the M-mapping to perform a change of orthogonal basis given by equation 2.24 and 2.25.

\[
A = a_3a_1^* + a_4a_2^*
\]  

(2.24)

\[
B = -a_3a_2 + a_4a_1
\]  

(2.25)
This orthogonal basis is equivalent to the column vector of the STBC block of the $G_2$ scheme as described in section 2.2.2. Since the distance between the two vectors in the new basis is equal to the original symbols a maximum likelihood detection rule can be applied to detect the new vectors $(A, B)$ and then decode them back to $(a_3, a_4)$ symbols.

Differential encoding follows M-mapping in which the vectors $(A, B)$ are mapped into consecutive symbols based on previously transmitted consecutive symbols from. This is shown in equation 2.22 and 2.23.

\begin{align*}
s_{2t+1} &= A s_{2t-1} - B s_{2t}^* \\
s_{2t+2} &= A s_{2t} - B s_{2t-1}^* 
\end{align*} \tag{2.26}

where $(s_{2t}, s_{2t-1})$ are the previously transmitted symbols from the first and second antenna respectively at time $2t-1$. Now at the current instant of time $2t+1$, $(s_{2t+1}, s_{2t+2})$ form the differentially encoded symbols for transmit antennas one and two respectively. These symbols are then space time block coded to form the $G_2$ matrix with $(s_{2t+1}, s_{2t+2})$ and $(-s_{2t+2}^*, s_{2t+1}^*)$ as the row vectors that are transmitted at time instants $2t+1$ and $2t+2$ respectively. $(s_{2t+1}, s_{2t+2})$ pair is fed back for the generation of next set of differentially encoded symbols $(s_{2t+3}, s_{2t+4})$.

Figure 2.7 shows the decoding process of D-STBC. It is assumed that the channel is flat and quasi static for the duration of 4 consecutive symbol durations. Let $r_{2t-4,n}, r_{2t,n}, r_{2t+1,n}, r_{2t+2,n}$ be the consecutive symbols received by the $n^{th}$ antenna element.

Then the received signals at antenna one can be written as.

\begin{align*}
r_{2t-1,1} &= h_{11} s_{2t-1} + h_{21} s_{2t} + n_{2t-1,1} \\
r_{2t,1} &= -h_{11} s_{2t}^* + h_{21} s_{2t-1}^* + n_{2t,1} 
\end{align*} \tag{2.28}

\tag{2.29}
where $h_{11}, h_{21}$ are corresponding channels between transmit antenna and receive antenna elements. $n_{2r-1,n}, n_{2r+1,n}, n_{2r+2,n}$ are Gaussian random variables representing noise and interference at a certain time instant on the nth antenna element. Similar equations can be written for the signals received by the second antenna element.

Now a differential decoding process similar to the STBC case is done as shown in equation 2.32 and 2.33 which gives an estimate of $A$ and $B$ transmitted vectors.

$$r_{2r+1,1} = h_{11} r_{2r+1} + h_{21} r_{2r+2} + n_{2r+1,1}$$  \hspace{1cm} (2.30)$$

$$r_{2r+2,1} = -h_{11} s_{2r+2}^* + h_{21} s_{2r+1}^* + n_{2r+2,1}$$  \hspace{1cm} (2.31)$$

$$r_{2r-1,2} = h_{12} r_{2r-1} + h_{22} r_{2r} + n_{2r-1,2}$$  \hspace{1cm} (2.32)$$

$$r_{2r,2} = -h_{12} s_{2r}^* + h_{22} s_{2r-1}^* + n_{2r,2}$$  \hspace{1cm} (2.33)$$

$$r_{2r+1,2} = h_{12} r_{2r+1} + h_{22} r_{2r+2} + n_{2r+1,2}$$  \hspace{1cm} (2.34)$$

$$r_{2r+2,2} = -h_{12} s_{2r+2}^* + h_{22} s_{2r+1}^* + n_{2r+2,2}$$  \hspace{1cm} (2.35)$$

$$\tilde{A} = r_{2r+1,1} r_{2r-1,1}^* + r_{2r+2,1} r_{2r,1}^* + r_{2r+1,2} r_{2r-1,2}^* + r_{2r+2,2} r_{2r,2}^*$$  \hspace{1cm} (2.36)$$

$$\tilde{B} = r_{2r+1,1} r_{2r,1}^* - r_{2r,1} r_{2r-1,1}^* + r_{2r+1,2} r_{2r,2}^* - r_{2r,2} r_{2r-1,2}^*$$  \hspace{1cm} (2.37)$$
Thus the decoding process does a decoupling of the symbols to give decision statistics of A and B vectors. These decision statistics are fed to the ML detector to get the estimate \( \hat{A}, \hat{B} \). The estimates are then inverse M-mapped to originally transmitted bits.

A diversity order of four is achieved here which is the same as the C-STBC scheme with two antenna elements at the receiver. It can be seen from equations 2.32 and 2.33 that no channel estimation is required to decode the symbols. Figure 2.8 shows the performance comparison of C-STBC scheme and D-STBC scheme for a flat Rayleigh faded channel with the assumption of a perfect channel state information (CSI) at the receiver for C-STBC scheme. It can be seen that the D-STBC performance is about 3dB less than the C-STBC case as expected for a differential scheme. The D-STBC scheme is also robust to phase and frequency offset errors as differential decoding depends on previously transmitted symbols. If the phase or frequency error is constant for one space time block the error cancels out. Therefore D-STBC is a reasonable choice for a prototype implementation.

### 2.4 Summary

In this chapter a basic description of Space-Time Block Coding techniques was given. The analysis of C-STBC scheme with a 2x1 system was shown to give a diversity order equal to MRRC scheme with 1x2 system. This was expanded to a 2x2 C-STBC MIMO system to show that a diversity order of four could be achieved. The performance in terms of BER versus SNR was also shown. The principles of coherent STBC extended to implement a differential STBC scheme was explained to make the implementation easier for building a prototype. The analysis for a 2x2 MIMO system using D-STBC scheme was presented. It was shown that no channel estimation was needed at the receiver. Finally a performance comparison of C-STBC scheme and D-STBC schemes was shown. The ease of implementation in terms of carrier synchronization and comparable performance makes the D-STBC scheme for the MIMO hardware prototype an ideal choice.
Figure 2.8 Performance comparisons of coherent STBC and differential STBC schemes
Chapter 3

3 System Architecture of VT-STAR

3.1 Introduction
Fast development of a prototype design requires locating subsystems that perform efficiently and integrate easily. The later property is usually the bottleneck in such an effort. In a system design effort a firm understanding of the hardware requirements and design is important to evaluate the tradeoffs in using different off the shelf components. This chapter focuses on the various hardware subsystems designed and used in VT-STAR.

An overview of the VT-STAR architecture is presented first along with prototype system specifications. The custom design of the RF front ends is described next. The functioning and interface of data converters to the baseband units are explained in the data converters section. The next section describes the baseband processing units used in the transmitter and receiver. The high speed digital signal processor (DSP) architectures are also explained.

3.2 System Architecture Overview
VT-STAR architecture, shown in Figure 3.1, is based on a 2×2 antenna element array, which allows the exploitation of transmit and receive diversity mechanisms at the signal processing level. The Radio Frequency (RF) transmit and receive front ends accommodate a multi-channel two-stage up (and down) conversion between the RF section and the baseband section. The RF center frequency is centered at 2050 MHz. The baseband bandwidth of the system is limited to 750 kHz. Digital to Analog Conversion (DAC) is performed in baseband with 4 parallel Texas Instruments (TI) THS5661 EVMs, interfaced to the TI™ TMS320C6711 DSK through custom-designed hardware. The TI™ THS5661 EVMs operate simultaneously, allowing the synchronous transmission of data through the transmitter antenna array. On the receiver side, Analog to Digital Conversion (ADC) is performed with the multi-channel TI™ THS1206 EVM, which is mated directly to the TI™ TMS320C67 EVM at the receiver via the expansion peripheral interface. Table 3.1 summarizes the systems specifications met by the prototype.
Table 3.1 Prototype system specifications

<table>
<thead>
<tr>
<th>System Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center Frequency</td>
<td>2050 MHz</td>
</tr>
<tr>
<td>Maximum Signal Bandwidth</td>
<td>750 kHz</td>
</tr>
<tr>
<td>Receiver Noise Floor</td>
<td>-110 dBm</td>
</tr>
<tr>
<td>Maximum Receiver Input Power</td>
<td>-50 dBm</td>
</tr>
<tr>
<td>Spurious-Free Dynamic Range (SFDR)</td>
<td>60 dB</td>
</tr>
<tr>
<td>Transmitter Input</td>
<td>Baseband I/Q, 35 mV RMS</td>
</tr>
<tr>
<td>Receiver Output</td>
<td>Baseband I/Q, 140 mV RMS</td>
</tr>
<tr>
<td>Transmit Power (Maximum/Nominal)</td>
<td>28 dBm / 0dBm</td>
</tr>
<tr>
<td>Transmitter/Receiver Input/Output Impedance</td>
<td>50 Ω</td>
</tr>
<tr>
<td>D-STBC Data Rate</td>
<td>4.6 kbps</td>
</tr>
<tr>
<td>Modulation</td>
<td>QPSK</td>
</tr>
<tr>
<td>Number Transmit Elements</td>
<td>2</td>
</tr>
<tr>
<td>Number Receive Elements</td>
<td>2</td>
</tr>
</tbody>
</table>

3.3 Radio Front-End

The RF section of the transmitter accepts complex baseband signals (I and Q) produced by the digital hardware and produces RF signals, which are transmitted using two separate transmit antennas. Each antenna is a vertically polarized, co-planar, quarter wavelength monopole, where
monopoles were selected because of their simple design. Antenna spacing can be varied to study the spatial correlation and investigate its impact on performance. The receiver RF section uses two antennas to receive the signals. The signals are then down-converted to a band suitable for use by the sampling hardware.

An IF of 68 MHz was selected based on the availability of I/Q demodulators. Two stages of frequency conversion allow amplification to be divided among the stages, preventing the possibility of receiver instability. The AGC is designed to be software controlled. The algorithm computes the average received power (per receive antenna branch) and the values to be sent to the variable gain amplifier. Block diagrams of the transmitter and receiver are given in Figures 3.2 and 3.3, respectively. The transmitter band pass filters (BPFs) support a bandwidth of 100 MHz. On the receiver side the first stage BPFs has a bandwidth support of 100MHz and the BPFs in the IF stage have a bandwidth less than 1.2 MHz at 3dB and less than 1.5 MHz at 50dB. This makes the RF design flexible to accommodate higher bandwidths, but at the price of sensitivity.

![Figure 3.2 Transmitter radio front end](image-url)
3.4 Data Converters

3.4.1 Digital to Analog Conversion

The transmitter design requires conversion of complex digital I and Q signals produced by the baseband unit to be converted to analog signals for transmission by the RF front end. In this section the TI™ THS5661 digital to analog converter evaluation modules used in the transmitter are described along with issues of integration in a MIMO set up.

The THS5661 is a Texas Instrument 12-bit resolution, high-speed, low-power CMOS digital-to-analog converter (DAC) [THS99]. The THS5661 supports update rates up to 100 Msp. The THS5661 supports both a straight binary and twos complement input word format, enabling flexible interfacing with digital signal processors. The digital inputs are designed to interface with the TMS320 C5000 or C6000 family of DSPs which makes it easier to build an interface with the TI DSP startup kit (DSK) used in the transmitter. Table 3.2 summarizes the important characteristics of the THS5661 DAC.
Table 3.2 characteristics of the THS5661 DAC

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Update Rate</td>
<td>100Mspls</td>
</tr>
<tr>
<td>Resolution</td>
<td>12 bits</td>
</tr>
<tr>
<td>SFDR (Nyquist at 20MHz)</td>
<td>63dBc</td>
</tr>
<tr>
<td>Setup/Hold Time</td>
<td>1ns</td>
</tr>
<tr>
<td>Differential scalable current outputs</td>
<td>2-20mA</td>
</tr>
<tr>
<td>CMOS compatible digital interface</td>
<td>3V and 5V</td>
</tr>
<tr>
<td>Modes</td>
<td>Straight binary or 2’s complement conversion</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>175mW and 25mW (mode)</td>
</tr>
</tbody>
</table>

Figure 3.4 shows the block diagram of the THS56X1 family EVM. The J1 and J3 interface are used to connect to the DSP to supply digital data and control signals from the DSK board. The analog output is taken from the Differential operational amplifier interface J7 on the board which can be connected with an SMA connector. The single mode non-inverted output of the op-amp is used in VT-STAR, with a peak-to-peak voltage range of 2V.

Figure 3.5 shows the Interface design between the DSK and the DAC. The expansion peripheral interface of the DSK supplies the digital signal input to the DAC. The input to the DAC clock is derived from the write enable output (XWE) which is the strobe signal generated before data is output from data pins of the DSP. As seen in Figure 3.6 the write enable signal is active low for one clock cycle of the DSP. In the THS5661 EVM internal edge-triggered flip-flops latch the input word on the rising edge of the input clock. Figure 3.7 shows the timing diagram for the DAC. The THS5661 provides for a minimum setup and hold times (> 1 ns), allowing for non-critical external interface timing. Conversion latency is one clock cycle. The clock duty cycle can be chosen arbitrarily under the timing constraints; however, a 50% duty cycle gives optimum dynamic performance. Now the XWE signal has a minimum setup and hold time of 6.7ns which is one clock cycle of the C6711 DSP which satisfies the setup and hold time requirement of the input clock signal for the DAC. Hence data signals from the DSK get latched to the DAC by using the write enable signal. This approach simplifies the custom interface connector design.
This facilitates the use of J1 (EMIF interface) for both data and clock on the DSK board instead of using J3 (expansion peripheral interface) to derive the clock signal and J1 for data.

**Figure 3.4** Block diagram for TI\(^\text{TM}\) THS5661 DAC EVM board [THS01]

**Figure 3.5** Interface signals used between DSK and DAC
Figure 3.6 EMIF interface signals timing diagram [EMI00]

Figure 3.7 THS5661 DAC timing diagram [THS99]
The analog output at the differential output of the DAC board is calculated by equations given below.

\[
I_{OUT1} = I_{OUT_{FS}} \times \frac{CODE}{4096} \tag{3.1}
\]

\[
I_{OUT2} = I_{OUT_{FS}} \times \frac{4095 - CODE}{4096} \tag{3.2}
\]

\[
V_{OUT1} = I_{OUT1} \times R_{LOAD} \tag{3.3}
\]

\[
V_{OUT2} = I_{OUT2} \times R_{LOAD} \tag{3.4}
\]

\[
V_{OUT_{DIFF}} = V_{OUT1} - V_{OUT2} = \left(\frac{2CODE - 4095}{4096}\right) I_{OUT_{FS}} \times R_{LOAD} \tag{3.5}
\]

where \(I_{OUT_{FS}}\) is the full-scale output current. 4096 is the maximum integer value corresponding to 12 bits. \(CODE\) is the decimal representation of the DAC data input word. Output currents \(I_{OUT1}\) and \(I_{OUT2}\) drive resistor loads \(R_{LOAD}\). Therefore for a nominal resistor load of 50 \(\Omega\), a differential output swing of 2 \(V_{PP}\) is achieved when applying a 20mA full-scale output current.

For a MIMO system it is important that synchronization is achieved across multiple boards for multiple RF chains. For the 2x2 MIMO VT-STAR system four DACs are required corresponding to two complex baseband signals. Synchronization of all the four DAC boards is carried out by making a custom circuit using a clock distribution chip. This chip takes the \(XWE\) signal as the input and distributes the signal to the CLK input of the DAC boards. Figure 3.8 shows the block diagram of this set up. In the VT-STAR system the digital input to each DAC comes from a single 32-bit word output from the DSK simultaneously. Hence this 32 bit word is divided into four 8-bit digital inputs to each of the corresponding DAC. Hence the resolution used for each DAC is 8 bits.
3.4.2 Analog-to-digital Conversion

At the receiver after down conversion and mixing to baseband analog signals, the signals have to be converted to digital baseband signals as input to the digital baseband processing unit. This conversion in VT-STAR is performed by using four-channel TI™ THS1206 ADC evaluation module (EVM). In this section the characteristics and functioning of the ADC board and its interface to the TI™ C6701 DSP EVM board is discussed.

The THS1206 is a low-power, 12-bit analog-to-digital converter (ADC) with a conversion rate of 6MSPS for single channel and 1.5 MSPS when all the four channels are used. Its main features include four analog inputs, which are switched from sampling to hold mode simultaneously, fast speed, high resolution, and high data throughput. This feature makes the device attractive for use in conversion of multiple I/Q-modulated signals. The THS1206, with its programmable interface,
is designed to be compatible with TI C6000 processors. A fast data throughput to the connected processor is achieved with an integrated FIFO. The block diagram of the THS1206 ADC is shown in Figure 3.9.

![Block diagram of THS1206](image)

**Figure 3.9** Block diagram of THS1206 [Adc00]

The THS1206 has its own 16-word 12-bit FIFO. The FIFO takes the load off the processor connected to the ADC. Data can be transferred in burst mode, greatly improving the data throughput to the processor. The digital conversion result is provided in parallel data format via data bus pins D0 – D11. There are two different conversion modes: single and continuous. In the single conversion mode, a single simultaneous conversion of up to four analog input channels can be initiated by the single-conversion start signal (CONVST). The conversion clock in the single-conversion mode is generated internally using a clock oscillator circuit. The single-conversion mode is specifically used in control applications. In the continuous-conversion mode, an external clock signal is applied to the CONV_CLK input of the THS1206. The internal clock oscillator is switched off in this mode. The continuous-conversion mode is specifically used in
applications where a block of data must be converted from analog to digital format. In the VT-STAR system the CONVST signal is provided by the DSP CLKOUT signal.

The THS1206 has an integrated FIFO which is organized as a circular buffer in order to achieve the higher data throughputs required by the DSP processor. This circular buffer can store up to 16 samples. Figure 3.10 shows the structure of the THS1206 FIFO. It is arranged so that sample reading takes place asynchronously to the sampling clock CONV_CLK. Samples are automatically written to the FIFO.

![THS1206 FIFO](image)

**Figure 3.10** THS1206 FIFO [Adc00]

Write, read, and trigger pointers are used to control the writing and reading processes. The read pointer always points to the next location to be read. The write pointer always points to the location which contains the last written sample. With a selection of multiple analog input channels, the converted values are written to the circular buffer in a predefined sequence (autoscan mode) as shown in Figure 3.10. In this way, the channel information for the reading processor is continuously maintained. A specific storage depth (trigger level) must be selected for the circular buffer. When this level is reached, the THS1206 signals the connected DSP via the digital output DATA_AV (data available) that a block of conversion values is ready to be transferred. The block size to be read is always equal to the setting of the trigger level; this is
important in order to maintain the channel information when multiple channels are selected. Consider an example for four analog input channels (AINP, AINM, BINP and BINM), as used in the VT-STAR set up, with the trigger level set to 8. The samples are written to the FIFO according to the autoscan mode where one channel input is selected sequentially and converted to digital data on each CONV_CLK cycle as shown in the FIFO diagram. The signal DATA_AV becomes active when the write pointer reaches the trigger pointer. Using DATA_AV as an interrupt, the processor is immediately able to read the eight-word block and the trigger pointer is incremented by 8 as seen in Figure 3.10. If the processor can not read the data immediately, new samples are written to the FIFO and the trigger and read pointers stay at the same location. Thus, when the write pointer returns to location 1, the four oldest data samples in the FIFO are overwritten. At this time, the read pointer and the trigger pointer are incremented by the number of selected channels (four in this example) in order to maintain the channel information.

The DSP will not be able to read the data from the THS1206 within one CONV_CLK cycle if the processor has to jump into an interrupt service routine for every conversion value. The FIFO incorporated in the THS1206 allows the processor to read the conversion values in a burst. Data reading in burst mode increases the data throughput, because the latency time of the processor is seen only once per burst. Figure 3.11 shows the timing diagram of the THS1206 FIFO operation. Hence the programmable storage depth allows for adjustment to the DSP processor and strongly reduces the burden on the processor.

![Figure 3.11 THS1206 FIFO timing diagram](Adc00)

The TI Code Composer provides a utility for setting up the parameters of THS1206. This makes the setting up of the interface to the ADC easy. The parameters can be chosen from different
drop down boxes. This utility then generates the required C files with data structures to setup the initialization and data collection routines and function calls which can be used by the DSP program.

Hence the THS1206 EVM board is a good choice for faster development of DSP prototypes using TI DSP EVM boards.

### 3.5 Digital Signal Processing Baseband Units

In this section baseband processing units used at the transmitter and receiver are discussed. TI TMS320C6000 series floating point processors were chosen as this could reduce time to implement the algorithms and also make the evaluation easier to compare with MATLAB though there is a price paid in terms of cost and speed. A DSP Starters KIT (DSK) with TI C6711 chip was used at the transmitter. This is a stand alone board which can be connected to the serial port of a computer. This was chosen to make the transmitter lighter and operable using a laptop computer. At the receiver section a TI C6701 evaluation module (EVM) is used. This EVM interfaces with a PCI slot and hence is useful in collection of measurement data on a PC. The architecture of the boards is similar hence the discussion of the architecture of the one board is done to bring out the common salient features of the board. The processors used on both the boards have identical floating point architectures except for some differences in memory and direct memory access (DMA) units. This section therefore mainly discusses the TI C6701 series floating point processor in general. The difference in the architecture of C6711 is then briefly discussed.

The C6701 EVM (C67x EVM for generality) board features a PCI interface, SBSRAM and SDRAM, a 16-bit audio codec and embedded JTAG emulation support. Connectors on the EVM board provide a DSP external memory interface (EMIF) and peripheral signals that enable it to be expanded with custom or third-party daughterboards. Figure 3.12 shows the EVM hardware block diagram.
Figure 3.12 C6701 EVM hardware block diagram

The EVM hardware is divided into 12 different sections [EVM98]:

- **C6000 DSPs** - The C67x EVM is based on the C6701 DSP, which operates up to 1337 MIPS with a CPU clock rate of 167 MHz. The EVM board uses a 133 MHz version of the C67x CPU.

- **DSP clock** - The EVM has two different onboard clock sources (33.25 MHz and 25 MHz for the C67x EVM) and two clock modes (multiply-by-1 and multiply-by-4), enabling the DSP to operate at four different clock rates.
• **External memory** - The C67x EVM provides one bank of 64K x 32, 133-MHz SBSRAM and two banks of 1M x 32, 100-MHz SDRAM. Additional asynchronous memory can be added with a daughterboard using the expansion memory interface. All external memory devices are byte-addressable.

• **Expansion interfaces** - The C67x EVM has external memory interface and external peripheral interface connectors that enable the use of custom or third-party daughterboards like the DAC and ADC boards used in VTSTAR.

• **PCI interface** - The C67x EVM includes a PCI Local Bus Revision 2.1-compliant interface that enables host access to the onboard JTAG controller, DSP host port interface (HPI) and board status/control registers.

• **JTAG emulation** - JTAG emulation support is provided using an onboard test bus controller (TBC) as well as a header to support an external XDS510 emulator.

• **Programmable logic** - The C67x EVM CPLD provides the board's glue logic and control/status registers.

• **Audio interface** - The EVMs include a CD-quality, 16-bit audio interface with stereo microphone and line-level inputs and a stereo line-level output.

• **Power supplies** - The EVMs use voltage regulators to provide 1.8V (C67x) for the DSP core; 3.3 V for the C6701 I/O memories, CPLD and debuggers; and 5 V for audio components.

• **Voltage supervision and reset control** - The EVM uses a voltage supervisor to monitor the board's voltages and provide a board reset signal.

• **LED indicators** - Three LED indicators are provided -- one green LED to indicate that power is on, and two LEDs for user-defined status.

• **User options** - The EVM supports user-defined control via 12 onboard DIP switches or with direct control by host software via the PCI bus.

More detailed information on each of the hardware sections can be found in [EVM98]. In contrast the DSK board provides 16MB of SDRAM and 128KB of Flash memory. Next the processor architecture and functionality is described which forms the heart of the baseband processing unit.
The block diagram TMS320C6701 (C6701) chip is shown in Figure 3.13. The TMS320C67x DSPs are the floating-point DSP family in the TMS320C6000E DSP platform. The C6701 device is based on the high performance advanced VelociTI very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI). The VT-STAR DSP EVM uses a C6701 which has a clock rate of 133MHz and a processing power of 1064 Mega Floating point Operations per Second (MFLOPs). This processor has 32 general-purpose registers of 32-bit word length and eight highly independent functional units.

![Figure 3.13 TMS320C6701 functional block diagram [Tms00]](image)

The CPU has eight functional units that provide four floating-/fixed-point ALUs, two fixed-point ALUs, and two floating-/fixed-point multipliers. The C6701 can produce two multiply-accumulates (MACs) per cycle for a total of 334 million MACs per second (MMACS). The functional units are divided into two sets. Each set contains four units and a register file. One set

† These functional units execute floating-point instructions.
contains functional units’ .L1, .S1, .M1, and .D1; the other set contains units .D2, .M2, .S2, and .L2. L and S are both general arithmetic and logic units (ALUs), D is a address calculation unit and M is for multiplication.

Traditionally in complex instruction set computers (CISC) complex instructions were broken down into simpler microinstructions for execution on parallel superscalar architectures. Regularity of execution using microinstructions of identical length and single cycle execution times were used in reduced instruction set computers (RISC) which evolved next. The Pentium processors use a hybrid approach of combining the CISC and RISC features to achieve superscalar design super pipelining and out-of-order execution. In VLIW architecture the compiler combines multiple simple instructions into a very long instruction. This technique moves the burden for allocating microoperations to parallel resources from the processor hardware to computer compiler software. To achieve optimum compilation from a high-level language more number of bits is needed for specialized DSP instruction set which are not available in the instruction word of traditional signal processor. The VLIW architecture provides individual control of each resource as shown in Figure 3.14. In this design a several hundred bit instructions divided into dedicated fields to control each resource separately.

![VLIW architecture with explicit control to each resource](image)

**Figure 3.14** VLIW architecture with explicit control to each resource [Ack99]
The TI VelociTI architecture allows reconfiguration of these control fields to switch among resources which is shown in Figure 3.15. The VelociTI architecture of the C6700 makes it one of the first off-the-shelf DSPs to use advanced VLIW to achieve high performance through increased instruction-level parallelism. VelociTI is a highly deterministic architecture, having few restrictions on how or when instructions are fetched, executed, or stored. It is this architectural flexibility that is key to the breakthrough efficiency levels of the TMSC6000 Optimizing C compiler. VelociTI’s advanced features include:

- Instruction packing: reduced code size
- All instructions can operate conditionally: flexibility of code
- Variable-width instructions: flexibility of data types
- Fully pipelined branches: zero-overhead branching.

![Diagram of VelociTI architecture](Ack99)

**Figure 3.15** TI VelociTI VLIW architecture with reconfiguration of control to each resource

The CPU fetches VelociTI advanced very-long instruction words (VLIW) (256 bits wide) to supply up to eight 32-bit instructions to the eight functional units during every clock cycle. The VelociTI VLIW architecture features controls by which all eight units do not have to be supplied with instructions if they are not ready to execute. The first bit of every 32-bit instruction determines if the next instruction belongs to the same execute packet as the previous instruction, or whether it should be executed in the following clock as a part of the next execute packet.
Fetch packets are always 256 bits wide; however, the execute packets can vary in size. The variable-length execute packets are a key memory-saving feature, distinguishing the C6701 CPU from other VLIW architectures.

The processing flow begins when a 256-bit-wide instruction fetch packet is fetched from a program memory. The 32-bit instructions destined for the individual functional units are “linked” together by “1” bits in the least significant bit (LSB) position of the instructions. The instructions that are “chained” together for simultaneous execution (up to eight in total) compose an execute packet. A “0” in the LSB of an instruction breaks the chain, effectively placing the instructions that follow it in the next execute packet. If an execute packet crosses the fetch-packet boundary (256 bits wide), the assembler places it in the next fetch packet, while the remainder of the current fetch packet is padded with NOP instructions. The number of execute packets within a fetch packet can vary from one to eight. Execute packets are dispatched to their respective functional units at the rate of one per clock cycle and the next 256-bit fetch packet is not fetched until all the execute packets from the current fetch packet have been dispatched. After decoding, the instructions simultaneously drive all active functional units for a maximum execution rate of eight instructions every clock cycle. While most results are stored in 32-bit registers, they can be subsequently moved to memory [TMS00].

The two register files shown in Figure 3.13 contain 16 32-bit registers each for the total of 32 general-purpose registers. The two sets of functional units, along with two register files, compose sides A and B of the CPU. The four functional units on each side of the CPU can freely share the 16 registers belonging to that side. Additionally, each side features a single data bus connected to all registers on the other side, by which the two sets of functional units can access data from the register files on opposite sides. While register access by functional units on the same side of the CPU as the register file can service all the units in a single clock cycle, register access using the register file across the CPU supports one read and one write per cycle.

Another key feature of the C6701 CPU is the load/store architecture, where all instructions operate on registers as opposed to data in memory. Two sets of data-addressing units (.D1 and .D2) are responsible for all data transfers between the register files and the memory. The data
address driven by the .D units allows data addresses generated from one register file to be used to load or store data to or from the other register file.

The C6701 DSP also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals. Program memory consists of a 64K-byte block that is user-configurable as cache or memory-mapped program space. Data memory consists of two 32K-byte blocks of RAM. The peripheral set includes two multichannel buffered serial ports (McBSPs), two general-purpose timers, a host-port interface (HPI), and a glueless external memory interface (EMIF) capable of interfacing to SDRAM or SBSRAM and asynchronous peripherals. The C6701 has a complete set of development tools which includes: a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows debugger interface for visibility into source code execution.

Figure 3.16 shows the block diagram of the C6711 DSP used in the DSK for the transmitter.

---

† In addition to fixed-point instructions, these functional units execute floating-point instructions.

**Figure 3.16** Functional block diagram of C6711 [Tms01]
This chip operates at 150MHz clock frequency with a processing power of 1200 MFLOPS. The C6711 is similar to C6701 in terms of the CPU, McBSPs, HPI, timers and the interrupt controller. The difference is in memory organization. The C6711 is a two-level cache-based device, with separate level-one program and data caches. These small, fast L1 caches are always active, and typically provide the CPU with a high (~98%) hit rate. The L2 is available for use as a level-two cache, as statically memory mapped SRAM space, or as a combination of the two. An enhanced DMA is implemented on the C6711 to provide more flexibility in programming data transfers with 16 channels. The EMIF is enhanced to allow the device to interface to additional memory types. The C6711 can interface to 8 and 16-bit wide SDRAM, SBSRAM, and asynchronous memory, in addition to the 32-bit wide memory interface capability provided by the C6701.

### 3.6 Summary
From chapter 2 it can be said that the algorithms to be implemented for D-STBC require many complex additions and multiplications and matrix operations for a MIMO system. This translates to high speed baseband processor requirement to execute the algorithms in real time. The TI C67x processors selected for the system were at the time the fastest DSP processors available off the shelf. The EVM modules with their functionalities explained make them ideal for the prototype development as they are easier to interface with TI data converter boards with plug and play software. The code composer utility with its integrated development environment (IDE) is one of the easiest debugger utilities available for development of DSP code. The optimizer available with the code composer is said to achieve 80% efficiency of hand coded assembly code. It has many plug-in features which can be used for real-time debug. The RF front end was designed for a bandwidth of 1MHz and at a carrier frequency of 2.05GHz which is in the range of frequency used for 3G and WLAN systems. The RF front end could be used for future development to interface with multiprocessor baseband units to achieve high data rates and other possible measurements. This chapter explained in detail the various subsystems used and designed for VT-STAR. The next chapter looks at the software/hardware co-design to implement transmitter receiver algorithms.
Chapter 4

4 Real-Time Implementation

4.1 Introduction
A hardware platform is desired to fully explore the details of the implementation of MIMO schemes like D-STBC. While it is possible to study the performance of these algorithms in simulation, the assumptions inherent to the simulation mean that the algorithm’s performance when applied to a real system may not match the expected behavior. Most researchers assume ideal timing and phase tracking at the receiver as well as a perfect channel estimation process for their simulations. In practical systems, however, these assumptions are not realistic. In order to explore the multiple aspects of MIMO, the aim of VT-STAR is to create a platform that allows the evaluation of the channel and implement space-time algorithms like D-STBC that take advantage of the system’s MIMO architecture. D-STBC as was explained in chapter 2 has the main advantage of making carrier phase recovery unnecessary. This difference allows for a far simpler implementation of STBC for a prototype. The design and implementation of transmitter and receiver algorithms and their performances in real time is presented in this chapter. This also includes the I/O functionalities to give a clear picture of the system. Hence this chapter can be considered as dealing with software-hardware co-design of VT-STAR.

The core algorithms, implemented on TI™ TMS320C67 EVM floating-point DSP processors, include space-time encoding along with modulation and pulse shaping at the transmitter side; matched filtering, space-time processing, automatic gain control (AGC), channel estimation, timing recovery and maximum likelihood decoding at the receiver side. The Real-Time Data Exchange (RTDX) feature of the C67 is used to offer real-time monitoring of physical layer parameters such as bit-error rate, diversity gain, constellation diagrams, AGC curves and more. A host PC, which runs a multi-threaded application to manage a MATLAB™ session, is used to display the physical layer parameters and to collect real time data.
The VT-STAR receiver has two modes of operation: continuous mode and snapshot mode. In the continuous mode, the receiver DSP operates in real-time, performs full space-time demodulation and decoding and sends relevant physical layer parameters to the host PC via the Real-Time Data Exchange (RTDX™) facility of the C67. In the snapshot mode, the receiver DSP is used as a data acquisition device. It collects raw data into buffers and dumps the buffers into the host PC’s hard drive for post-processing in MATLAB™. While the continuous mode allows for a study of the interactions between space-time decoding, timing and phase recovery and channel estimation, the snapshot mode is used to study the spatial and temporal characteristics of the MIMO channel.

This chapter begins with the signal flow graph of the transmitter. The design and implementation of each sub-block is explained in detail. The same is followed with the receiver design. In the receiver design the data collection capability using RTDX is also explained. The real time issues in terms of I/O mechanisms, clock cycles, and space-time tradeoffs with respect to DSP processing for MIMO design are the highlights of this chapter.

### 4.2 Transmitter

The component layout of the VT-STAR transmitter is shown in Figure 4.1. The transmitter is composed of three separate sections, the processing core, the data interface, and the radio hardware. The processing core is a C67-based DSK, providing the processing backbone to generate D-STBC encoded symbols that are synchronously transmitted to the dual RF chains. The data interface is composed of multiple DACs, since a single four channel commercial DAC board or EVM was not available.

The D-STBC data flow graph is shown in Figure 4.2. It commences with generation of information source sequence. A pseudo random noise (PN) generator of maximal length 31 is used to generate these source bits. As it will be seen in the receiver section these PN sequences are used in deriving the symbol timing. Four information bits generated in the sequence are first Gray encoded and mapped into two QPSK symbols. Gray encoding is performed on the source bits to get an estimate of the bit error rate (BER) at the receiver directly by counting the symbol errors. These QPSK symbols then undergo the core D-STBC processing as explained in chapter
2. The core D-STBC processing is partitioned into three different functions: M-mapping, differential encoding and STBC block coding.

**Figure 4.1** Block diagram of multi-channel transmitter

**Figure 4.2** Transmitter software flow chart
The M-mapping generates a change of constellation diagram for the incoming QPSK symbols. It performs a change of basis from the natural basis to an orthonormal design described by the following M Matrix:

\[
M = \begin{bmatrix}
a_1 & a_2 \\
-a_2^* & a_1^*
\end{bmatrix}
\]  

(4.1)

where, \((a_1, a_2)\) represents a unit norm vector and which is set to

\[
(a_1, a_2) = \left(\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{2}}\right)
\]

(4.2)

The outputs from this mapping are two complex symbols \(A\) and \(B\) that are generated as

\[
\begin{bmatrix}
A \\
B
\end{bmatrix} = M^* \begin{bmatrix}
a_3 \\
a_4
\end{bmatrix} = \begin{bmatrix}
a_3a_1^* + a_4a_2^* \\
-a_3a_2 + a_4a_1
\end{bmatrix}
\]

(4.3)

where ‘*’ refers to element-wise conjugation and \((a_3, a_4)\) represents the pair of newly generated input QPSK symbols. The differential encoder uses previously transmitted symbols and current input symbols to compute a pair of symbols to be transmitted next.

\[
\begin{align*}
s_3 &= A \cdot s_1 - B \cdot s_2^* \\
s_4 &= A \cdot s_2 + B \cdot s_1^*
\end{align*}
\]

(4.4)

where \((s_1, s_2)\) is a pair of previously transmitted symbols and \((A, B)\) are the current input symbols. The outputs from the differential encoding process are mapped by \(G_2\) mapping to form two parallel baseband complex symbol streams for two antenna branches as shown in Figure 4.3.

The \(G_2\) mapping maps block of \(k=2\) symbols \((s_3, s_4)\) to two orthogonal sequences of length \(p = 2\). \(G_2\) mapping provides an orthogonal design, which facilitates the space-time processing stage at the receiver in order to decouple the symbols and obtain an estimate for the pair \((A, B)\).

![Figure 4.3 G2 mapping](image-url)
It can be seen that all the symbols generated are complex since they have I and Q components. To implement the above discussed D-STBC processing the complex computations were carried out by splitting the complex values into constituent real and imaginary entities and doing separate computations for real and imaginary results. This was seen to reduce the computational time by more than half when compared to using complex add and subtract operations in C.

The resulting baseband complex symbols, $I_1$, $Q_1$ for antenna 1 and $I_2$, $Q_2$ for antenna 2 were individually pulse shaped by square root-raised-cosine (RRC) filters with rolloff factor of 0.35. The pulse-shaping filters are of finite impulse response (FIR) filters with 19 taps. Four filters (I and Q each for two antennas) with over-sampling factor of 3 were implemented. So each baseband channel requires 6 convolutions per STBC block. The impulse response and the frequency response of the root raised cosine filter used is shown in Figures 4.4 and 4.5 respectively.

![Impulse response](image)

**Figure 4.4** Impulse response of root raised cosine filter
The filter outputs are then formatted in the data-packing segment to match the output interface requirements. A parallel output scheme is necessary to maintain time synchronization across the antenna elements while transmitting $I_1$, $Q_1$, $I_2$, and $Q_2$. The C67 DSK has a peripheral expansion bus J3 that supports parallel I/O of a 32-bit word. Since four independent DACs have to be addressed with a single 32-bit word digital output, 32-bit wide $I_1$, $Q_1$, $I_2$, and $Q_2$ floating point samples generated after pulse shaping were truncated to 8-bit integer words, and then concatenated to form a single 32-bit wide transmitter (TX) word. The TX word containing 8-bit $I_1$, $Q_1$, $I_2$, and $Q_2$ symbols was channelized to the external DACs with the proper I/O interface design as was shown in chapter 3.

**Figure 4.5** Frequency response of root raised cosine filter
Table 4.1 shows the profiling results performed on different functions used in the transmitter code on the DSK. The cycle count shown is the maximum number of clock cycles observed over iterations through the same function. This was performed using the code composer profiling utility. The Inclusive cycle count includes the function calls within the routines being profiled. For example rrc_filter has four function calls to fir_asm and the rest is used for data packing and formatting. The exclusive cycle count excludes these function calls. “gen_stbc” includes all the functions and is taken as the function which generates one block of pulse shaped D-STBC samples.

<table>
<thead>
<tr>
<th>Function</th>
<th>Inclusive Cycle Count (Max)</th>
<th>Exclusive Cycle count (Max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>gen_stbc</td>
<td>67415</td>
<td>3989</td>
</tr>
<tr>
<td>pn_gen</td>
<td>988</td>
<td>988</td>
</tr>
<tr>
<td>qpsk_map</td>
<td>799</td>
<td>799</td>
</tr>
<tr>
<td>stbc_map</td>
<td>1387</td>
<td>1387</td>
</tr>
<tr>
<td>oversample</td>
<td>856</td>
<td>856</td>
</tr>
<tr>
<td>Pulse_shape</td>
<td>59942</td>
<td>6608</td>
</tr>
<tr>
<td>rrcfilter</td>
<td>9443</td>
<td>4557</td>
</tr>
<tr>
<td>fir_asm</td>
<td>1071</td>
<td>1071</td>
</tr>
<tr>
<td>dac_transmit</td>
<td>193</td>
<td>193</td>
</tr>
</tbody>
</table>

Figure 4.6 shows the bar graph of the relative cycle counts of each function. As can be seen the pulse shaping function takes the highest number of clock cycles and code size. The root raised cosine filters were written in assembly to optimize the code in terms of execution speed and reduce code size. It can also be seen that though “stbc_map” takes large program memory the execution is relatively fast which constitute multiple complex number additions and multiplications. Hence there is parallelism of instructions and the multiple computational units of the DSP handles these better than conventional processors as the compiler optimizes the code for VLIW architecture.
The real-time generation and transmission of D-STBC pulse shaped data samples was maintained at a constant rate at the transmitter. This was achieved through the use of hardware timer interrupt and software interrupts for function calls. The output scheme was based on a ping-pong buffer concept. Two buffers of size 624 of 32 bit words were used to store the pulse shaped STBC encoded symbols. Before transmission of the first sample both the buffers are filled up. The next hardware interrupt generated by the timer writes the stored word in the first buffer to the output port for transmission. When the transmission from first buffer is completed the buffers switch roles and the second buffer is used to transmit while the first buffer is used to fill up with new D-STBC samples. The generation of new samples is initiated by software interrupt generated after each transmission. Each software interrupt generates one STBC block which stores 6 words (I1, Q1, I2, Q2) to be stored in the buffer. After completion of transmission of one buffer, their roles are interchanged. From profiling results it is seen that generation of 1

**Figure 4.6** Profiling results of the transmitter code structure (number of DSP clock cycles).
block of pulse shaped D-STBC symbols require a maximum of 67415 DSP clock cycles which is equivalent to 451.68µs given that the C6711 DSP clock frequency is 150MHz. This means that a set of 6 TX words constituting I1, Q1, I2 and Q2 samples in each word gets stored in the buffer after every 451.68µs. Therefore time taken to store each word is about 75.28µs. A high priority hardware interrupt (HWI), driven by timer 0 (T0) with time period $T = 200$ µs, services an interrupt service routine (ISR) that accesses the transmitting buffer and transmits one 32-bit TX word to the interface board. The HWI takes a maximum of 193 clock cycles to process which is equal to 1.3µs. This means that transmitting all the words in one buffer takes more time than storing new words. The second ping pong buffer is ready to transmit before transmission of first buffer is completed. Generation of new samples does not take place until one of the buffers is free. Thus it is made sure that transmission of new words take place on every HWI and no samples are lost. The selection of transmission rate to 200 µs was done to achieve real time constraints of receiver processing and to match the ADC performance at the receiver.

Each module was tested with test vectors to assure proper input/output functionality. After completing testing of each individual module/function, the complete transmitter section on the DSP was tested by writing the output to a binary file and loading it into the MATLAB™ workspace for comparison with the simulated algorithm output. A perfect match validated the DSP implementation of the transmitter.

### 4.3 STBC Receiver

The block diagram of the receiver is shown in Figure 4.7. The receiver architecture is composed of two RF branches, multi-channel ADC, TMS320C67 DSP Evaluation Module, and host PC. The received signals are amplified, down-converted and filtered, producing baseband inphase and quadrature (I and Q) signals suitable for use by the sampling hardware. The ADC was implemented using the multi-channel TI THS1206 ADC EVM, allowing a 4-channel ADC to be mated directly to the TI C67 EVM. The DSP is used to either perform space-time decoding in the real-time mode or collect raw data as a data acquisition unit for the snapshot mode. The host PC is used for control of the DSP via TI’s code composer and for display and storage of relevant physical layer parameters. The host PC is also used for post-processing computations of raw data in MATLAB™.
The multi-channel TI THS1206 ADC EVM selected for the interface between the RF front-end and the DSP has a maximum sampling rate of 1.5 Msps/channel. This means that the hard limit for the system will be a bandwidth of 750 kHz. Note that there is another softer limit, the DSP processing power. While the hard limit on system bandwidth is 750 kHz, the processor may not be able to support the full system bandwidth, depending on the computational complexity of the coding algorithm that is implemented.

The ADC stores received samples in a variable depth (1 to 16 words) FIFO. When this FIFO fills up, the ADC generates a hardware interrupt to the DSP. An interrupt service routine (ISR) reads the samples from the FIFO to a buffer in the DSP. For the data to be received and processed continuously in real-time, the receiver uses two buffers, denoted A and B. While buffer A is filled by the ISR with new samples, the processor performs demodulation and decoding of the samples in buffer B, where this process is alternated between the two buffers. To prevent any buffer overwrite, the sampling rate is set such that the decoding process completes its operation on a given buffer before the ISR fills up the other buffer. The buffer size chosen was 624 to allow for symbol timing recovery scheme to have large number of bits available for correlation with the known PN sequence.

The VT-STAR receiver has two modes of operation: continuous mode and snapshot mode. In the former, the receiver DSP operates in real-time, performs full space-time demodulation and
decoding and sends relevant physical layer parameters to the host PC via the (RTDX™). This mode is used to demonstrate the capabilities of space-time coding and to study the interactions between space-time decoding, timing and phase recovery and channel estimation. In the snapshot mode, the receiver DSP is used as a data acquisition device. It collects raw data into buffers and dumps the buffers into the host PC’s hard drive for post-processing in MATLAB™. This mode is used to study the spatial and temporal characteristics of the MIMO channel. MIMO channel measurements are post-processed to address the achievable throughput and reliability in a variety of indoor realizations.

4.3.1 Continuous Mode
The implementation of the receiver in the continuous mode is shown in Figure 4.8. In this mode, the receiver DSP operates in real-time, performs full space-time demodulation and decoding and sends relevant physical layer parameters to the host PC via the RTDX™ facility of the C67.

![Figure 4.8 Signal flow diagram in continuous mode](image)

The raw samples stored in the buffer are input to a squared root raised cosine (SRRC) matched filter with rolloff factor 0.35 which is the same as the transmitter pulse shaping filter. The matched filter is a finite impulse response (FIR) filter with 19 taps and represents a truncated SRRC ($\pm 3$ symbols) with 3 samples per symbol. Consecutive filtered samples are stored in an array. This pointer to the array determines the correct sampling instant of the starting symbol.
Figure 4.9 shows a flow diagram of the receiver software implemented on the TI™ TMS320C67 EVMs, respectively.

To commence D-STBC decoding 2 consecutive received symbols are taken as input from the filter array by taking six consecutive samples starting from the array pointer. Differential decoding is then performed on this block of received samples by decimated filter outputs by 3 (over sampling factor). This algorithm is described by the following equations:

\[
\begin{align*}
\tilde{R}_0^j &= r^j_{r+2T} (r^j_r)^* + (r^j_{r+3T})^* r^j_{r+T}, \\
\tilde{R}_1^j &= r^j_{r+2T} (r^j_{r+T})^* - (r^j_{r+3T})^* r^j_r, \quad j = 1, 2
\end{align*}
\]

(4.5)

where \( r^j_r = \begin{bmatrix} r^j_r & r^j_{r+T} & r^j_{r+2T} & r^j_{r+3T} \end{bmatrix}^T \), \( j = 1, 2 \) denotes a receive vector of 4 consecutive symbols for antennas 1 and 2 represented by \( j \).
In order to utilize the dynamic range of the ADC effectively, an automatic gain control (AGC) algorithm is employed for each receive antenna. The norm of the vector \( \overrightarrow{R_0, R_1} \), \( j = 1, 2 \) is evaluated for receiver chains 1 and 2, respectively and average these with a 1st order Infinite Impulse Response (IIR) to obtain average gain estimate of each channel. This is described by:

\[ AGC^j = \alpha \cdot d^j + (1-\alpha) \cdot AGC^j \]

where

\[ d^j = \| \overrightarrow{R_0, R_1} \|, \quad j = 1, 2 \]

and \( 1/(1-\alpha) \) is the time constant of the IIR filter.

Next, receive combining is performed by summing the decision statistics across the two receive antenna elements in an equal gain combining (EGC) fashion:

\[
\begin{align*}
R_0 &= R_0^1 + R_0^2 \\
R_1 &= R_1^1 + R_1^2
\end{align*}
\]

The combined decision statistics are applied to a maximum likelihood (ML) decoder that determines the vector \( \hat{A}, \hat{B} \) that is closest (in terms of Euclidean distance) to the decision statistics vector \( \overrightarrow{R_0, R_1} \). This is described by:

Choose \( \hat{A}, \hat{B} = (A, B) \), such that \( \min \left\{ d^2 \left( \overrightarrow{R_0, R_1}, (A, B) \right) \right\} \)

Where \( d^2(x, y) \) is the Euclidean distance between signals \( x \) and \( y \).

Note that until ML decoding the symbol timing has not been achieved. An arbitrary output of the filter is assumed to be the right sample and decimation by three is followed to correspond to the sample of the next symbol for decoding. To derive symbol synchronization the output of ML decoder are inverse M-mapped and resolved into corresponding bits. These bits are stored in an array of length 31. Once the array is filled with bits a correlation is performed with known input.
PN sequence. If the correlation output is equal to 31 it signals the correct symbol timing. And the filter pointer is made as the reference. If the correlation is less than 31 the filter pointer is advanced to the next filter output sample and the process repeated until perfect correlation is achieved. Once synchronization is achieved the output of the ML decoder is passed to the channel estimation, bit error rate processing and RTDX.

The channel estimation process is a key to monitoring the MIMO channel. It is based on a decision directed mode once the error rate is below acceptable level (<1%). We re-generate an estimate of the transmitted symbols \( (\hat{s}_1, \hat{s}_2) \) by performing M mapping and differential re-encoding over the decoded bits. These feed-back estimates are used in the following set of linear equations to evaluate the MIMO channel estimates \( \hat{\alpha} = \begin{bmatrix} \hat{\alpha}_1^1 & \hat{\alpha}_1^2 \\ \hat{\alpha}_2^1 & \hat{\alpha}_2^2 \end{bmatrix} \) by:

\[
\hat{\alpha}_1^j = \frac{r_t^j \cdot (s_1)^* - r_{t+T}^j \cdot \hat{s}_2}{|s_1|^2 + |\hat{s}_2|^2}, \quad j = 1, 2
\]

\[
\hat{\alpha}_2^j = \frac{r_t^j \cdot (s_2)^* + r_{t+T}^j \cdot \hat{s}_1}{|s_1|^2 + |\hat{s}_2|^2}, \quad j = 1, 2
\]

(4.7)

Figure 4.10 shows the profiling results for the receiver implementation on the C6701 DSP. The plot shows the maximum number of cycles profiled for a function. Time sync function takes the most number of cycles only when it does the correlation with PN sequence which happens when 31 bits are decoded. That is once every 16 symbols (48 samples), whereas at all other times to process 3 input samples it takes 1326 clock cycles. The high number of computation in time sync function is due to 31 convolutions performed for correlation with a 31 length PN sequence which is implemented as an FIR filter. The total number of clock cycles required to do the receiver processing comes to about 62470 cycles which is equivalent to 468 µs. Note that this is the time required to process 6 received samples. Hence the time required to process one sample is 78 µs. To come up with this value the maximum number of cycles required for time sync was not used as it happens only once every 48 samples.
As seen from the plot, the match filtering function takes the next most of the clock cycles. The other computationally intensive operation is the Maximum Likelihood (ML detection), which requires 16 iterations in order to find the closest signal point in the differential STBC algorithm. The remaining STBC operations consume a small number of clock cycles, as the scheme relies on linear processing only.

To ensure that the receiver meets real time requirements without loosing samples, the TI code composer DSP/BIOS real time analysis (RTA) plug in was used. This analysis of the sampling/data for both transmitter and receiver is explained in the next section.
4.3.2 Communication between DSP receiver and Host PC

Communication between the host computer and the TI C67 EVM is performed through the EVM’s real-time data exchange (RTDX) capability. RTDX facilitates bi-directional real-time transfer of data between the host PC and the target TI C67 EVM through the JTAG interface such that the target application is not affected.

The application layer of the radio has three purposes: Display key parameters of physical layer (bit-error rate, constellation diagrams, diversity advantage curves, etc.), collect data for offline post-processing and modify a video sequence to demonstrate the effect of the proposed algorithms on video application. The process control software interfaces between the TI™ TMS320C67 EVM and the host PC and supports the MATLAB™ application. This software is composed of a single process containing two separate threads: main and data collection.

The only task of the main thread is to launch all other threads. The data collection thread interfaces with the TI™ TMS320C67 EVM, receiving data from the DSP and supporting a basic protocol to guarantee target/host synchronization.

The data collection thread interfaces directly to the TI™ TMS320C67 EVM through RTDX (real-time data exchange). RTDX™ facilitates bi-directional transfer of data between the host PC and the target TI™ TMS320C67 EVM through the JTAG interface in a way as not to interfere with the target application. The host application uses a Component Object Model (COM) client to interface with the RTDX™ Host Library through calls supplied by TI™.

Two RTDX™ channels were setup between the host and the TI™ TMS320C67 EVM; one channel was used to transmit from the TI™ TMS320C67 EVM to the host and the other channel controlled data flow in the reverse direction. A communications protocol over the RTDX™ link was implemented to guarantee that no buffer overflows occurred in the circular buffer used for RTDX™ communications between the TI™ TMS320C67 EVM and the host. The protocol follows the sequence seen in Figure 4.11.
Each data code in Figure 4.11 corresponds to the specific type of data to be transported in the next data set, such as the received signal constellation and the estimates of the channel coefficients. The acknowledgement from the host to the TI™ TMS320C67 EVM is received by the TI™ TMS320C67 EVM asynchronously since the host may require a lengthy amount of time to display the received information and process the reply.

The data collection thread passes the received data to the MATLAB™ environment running concurrently through the real-time data exchange protocol provided by MATLAB™. Once in the MATLAB™ environment, the data is processed and displayed by MATLAB™ on the host computer. A sample of telemetry data sent from the receiver processor is shown in Figure 4.12 and includes constellation diagrams at the matched filter output before and after decimation process (over sampling factor = 3), AGC curves for estimated received signal power in dBm, fading profiles of the MIMO channel, diversity gain curves, BER and more. This sample was collected from the target DSP by using synthetic data at the input to the DSP. It validates the real-time processing at the DSP and the communication protocol with the host PC via RTDX.
4.4 Making the Transceiver Real-time

To make a transceiver design function in real-time the important requirements are typically:

- The processing rate is as fast as the data acquisition rate
- The processing time has a low variance

To make sure that the processing takes less time than the data acquisition, the DSP/BIOS real time analysis (RTA) plug-in capability provided by the code composer was used.

The DSP code with different software interrupt functions and hardware interrupt functions were handled by the DSP/BIOS kernel which can be easily used for scheduling of interrupts and other functionalities. A brief explanation DSP/BIOS will be given in the next section. The RTA plug-in inserts some kernel software interrupts inside different code sections to collect real-time information to be passed to the host for analysis. This real time information includes the clock time stamp, posting of different software interrupts and end of software interrupts which can be selected from the RTA tool. The insertion of such code does not affect the real time performance.
as they have the least priority and are activated when the processor is free. When the load on the processor goes up the TRA code is preempted.

The transmitter real time execution graph is shown in Figure 4.13, where the update rate is set to 33.333 KHz.

The graph shows different software interrupt functions. Gen_stbc_swi is a software interrupt function for generating new samples. The kernel_swi is a software interrupt generated by DSP/BIOS utility for memory allocation and freeing operations in real time. Other threads include the functions called for RTA analysis. The right side of the execution graph shows the message log of the execution details. Each square on the execution graph corresponds to a message on the log. By double clicking a square on the execution graph the corresponding line of the log gets highlighted. This is a good way to check for completion of software interrupts in real time. The Time graph shows the number of timer interrupts generated which where set to 30 µs corresponding to the update rate. It can be seen that gen_stbc_swi which generates the D-STBC samples for transmission sometimes, does not finish processing in real time to transmit new samples. Therefore the red squares show up as errors when a process does not complete in real-time. Figures 4.14 and 4.15 show the execution graphs for update rates of 20 KHz and 10 KHz respectively.

Figure 4.13 Execution graph for transmitter code at 33.333 KHz
As can be seen from the execution graph for 20 KHz update rate the gen_stbc_sw is barely able to finish the execution in time. It is expected since from the clock cycles calculation it was found that to generate one sample takes about 75 µs. From Figure 4.16 it is clear that there is enough time for generation of new samples. The hardware interrupt always transmits new samples. Therefore we can say that below 10 KHz update rate the transmitter will successfully perform real time operation.

Looking at the receiver performance Figure 4.16 shows the execution graph at a sampling rate of 10 KHz.
Figure 4.16 Execution graph for receiver code at 10 KHz

It can be seen that the target CPU is heavily loaded and hence cannot supply the execution graph details in real time. The graph shows the RTA analysis after stopping the DSP for data which was buffered by the RTA application. The execution graph shows two software interrupt (SWI) processes receiveA_swi and receiveB_swi. Note that these two processes do receiver processing on buffers A and B which form one of the ping-pong buffers. For real time operation it is required that when one of the SWI is posted the other buffer should be empty for storing new samples. As is apparent from the graph receive B is in the middle of processing while receiveA_swi is posted. Next we consider decreasing the sampling rate to 5 KHz as shown in Figure 4.17.

Figure 4.17 Execution graph for receiver code at 5 KHz

In this case all each receive SWI is completed before switching to the other SWI. Note that other threads which run to pass the real time analysis data also get time to run on the DSP. This shows that with 5 KHz sampling rate the receiver can achieve real time operation. Hence the transmitter
update rate was set to 5 KHz and receiver sampling rate to 5 KHz. The over sampling factor is 3 so the actual bandwidth of the system is 1.6 KHz (5/3).

Figure 4.18 shows the execution graph for a sampling rate of 200 Hz.

\[\text{Figure 4.18 Execution graph for receiver code at 5 KHz}\]

The execution graph is regular and hence each receive process gets ample time to finish processing before the next buffer is ready.

4.5 Using DSP/BIOS for programming the DSP ‘C67

“DSP/BIOS is a scalable real-time kernel, designed for applications that require real-time scheduling and synchronization, host-to-target communication, or real-time instrumentation. DSP/BIOS provides preemptive multi-threading, hardware abstraction, real-time analysis, and configuration tools.” [Bio01]. Figure 4.19 shows how the DSP/BIOS module works with the host PC and the target DSP.

The host PC is used to write programs in C, C++ or assembly that uses the DSP/BIOS API. The Configuration Tool in code composer helps in defining objects to be used in your program. The program is then compiled, assembled and linked as shown in the figure. The DSP/BIOS Analysis Tools help test the program on the target device from Code Composer Studio while monitoring CPU load, timing, logs and thread execution. The threads include hardware interrupts, software interrupts, tasks, idle functions and periodic functions.
DSP/BIOS and its Analysis Tool for Code Composer Studio software are designed to minimize memory and CPU requirements on the target. All DSP/BIOS objects can be created in the Configuration Tool and bound into an executable program image. This reduces code size and optimizes internal data structures. There are some 150 APIs available which are modularized so that only those APIs that are used by the program need to be bound into the executable program. The DSP/BIOS takes about 150 words of program memory and about 575 words of data memory on the C67 DSP. The library is optimized to require the smallest possible number of instruction cycles, with a significant portion implemented in assembly language. The Communication between the target and the DSP/BIOS Analysis Tools is performed within the background idle loop. This ensures that the DSP/BIOS Analysis Tools do not interfere with the program’s tasks. If the target CPU is too busy to perform background tasks, the DSP/BIOS Analysis Tools stop receiving information from the target until the CPU is available. This was seen in the receiver execution graph earlier where the execution graph stopped updating due to high CPU load.
Figure 4.20 shows the amount of memory used on the SDRAM of the C6701 DSP for the transmitter. The figure was generated using the visual linker available on the code composer for version 2.0. This tool is not available on the code composer used on the receiver. Hence the results for the transmitter are presented here. The SDRAM memory ranges from address 80000000h to 80400000h which is equivalent to 4Mx32 bits of memory space.

In this figure the plane grey areas represent the program variables being stored; green areas represent the constants; the blue areas are the text of the code which forms the executable program and the yellow areas represent the system memory used for dynamic allocation. The dashed grey area represents free SDRAM memory. The total memory taken by DSP/BIOS programming in SDRAM memory size is equal to 1617Fh addresses which is 21.5 % of the total address space of SDRAM for C6711 DSK.

Figure 4.21 shows the zoom in of various blocks of memory in terms of text size which form the executables, memory used for storing constants and memory used for variables. In the case of receiver the total memory required is 5248 words in total.

DSP/BIOS API also standardizes DSP programming for a number of TI devices and provides easy-to-use powerful program development tools. These tools reduce the time required to create DSP programs. The Configuration Tool generates code required to declare objects used within the program. This allows DSP algorithm developers to provide code that can be more easily integrated with other program functions. The Chip Support Library (CSL) provides an easier method of device programming than traditional register programming. CSL APIs ensure portability between different DSP platforms with equivalent peripheral devices.
Figure 4.20 SDRAM usage by the DSP code
Figure 4.21 SDRAM usage by various individual sections of the DSP code
4.6 Space-time tradeoff

The concept of trading space against time occurs throughout the design and implementation of signal processing system. In software domain this means code size corresponding to memory space traded against execution speed. The languages used to develop and program the desired signal processing applications trade space for time. This also means a tradeoff between development time versus execution time. Spending time to optimize the code to ensure heavy pipelining can make a program run faster. The task of an algorithm language is to describe the algorithms with sufficient accuracy to allow debugging and manipulation by developers.

The DSP industry currently shows a trend towards architectures based on the Very Long Instruction Word (VLIW) like the C67 and Single Instruction Multiple Data like the ADI TigerSHARC paradigms. These new DSPs address the enormous computational requirements for next-generation communication devices such as wireless handsets for Wideband CDMA (W-CDMA) and provide special instructions for Viterbi decoding, adaptive filtering etc.

It has become increasingly difficult to take full advantage of the enormous computational power of modern DSPs in software. The main reasons for the "hardware/software performance gap" are the difficulty of exploiting parallelism in DSP architectures, deep pipelining without interlocks between hardware resources, and the fact that many DSP algorithms are data-transfer intensive. The solution provided to reduce this software/hardware gap is by DSP instruction set / algorithm co-optimization.

There is currently a hot debate on hand-designed vs. compiled DSP code: The traditional approach of hand-designed DSP assembly code is extremely difficult for VLIW/SIMD processors because signal-processing algorithms must be vectorized and hardware resources must be carefully scheduled by means of software pipelining, taking into account the latencies of all operations. For instance, a parallel multiply-accumulate operation is typically implemented by subsequent operand load, multiply, and add instructions, which have to be software-pipelined in order to obtain a throughput of one "parallel MAC operation" per cycle. The entire parallel MAC may take 8 or more cycles to complete. This way hand-designed DSP assembly code may offer significant performance advantages. On the negative side, it is hard to maintain and not portable.
The compiler-based approach, on the other hand, requires a very efficient C or C++ compiler. This approach obviously benefits from high level language (HLL) code simplicity but generic C code will not lead to equally efficient DSP code. Creating an efficient "DSP compiler" is difficult. First, many signal processing algorithms cannot easily be vectorized by a compiler, since compiler optimizations must generate equivalent and thus bit-accurate results—a compiler does not have a designer's choice of slightly modifying an algorithm to reduce computational complexity. Second, data-transfer intensive DSP algorithms must often be rearranged for more data reuse in order to eliminate the data-transfer bottleneck, but the corresponding compiler optimizations are difficult to implement. On the positive side, the compiler-based approach may be the only way to manage the complexity of next generation wireless devices and make DSP programming accessible to a wider range of programmers.

This is the approach followed by TI in developing a compiler for its VLIW architecture which gives various levels of optimization depending on the requirements of execution speed, pipelining and memory. Therefore a mixed approach, where most algorithms are written in HLL code and only few critical algorithms are coded in DSP assembler combines the advantages of the above two extremes. This approach was followed in the transceiver codes for the VT-STAR where the critical algorithms like filtering operations were hand coded in assembly and the rest in C. The refining of the current C code using intrinsic provided by the TI compiler should help further optimize the code for speed.

4.7 Summary

In this chapter we have discussed the implementation of D-STBC algorithm on a baseband processor. The hardware-software co-design methodology was explained. The real time performance issues of the transceiver were shown. Programming using DSP/BIOS real time kernel was adapted. Future of complex wireless designs will see greater use of real time operating systems (RTOS) software radio development. The space time tradeoff argument was put forward and the use of a combination of HLL and hand coded assembly was justified for development of VT-STAR. The next chapter reviews channel measurements described in literature and the following chapter describes the modification of VT-STAR to perform channel measurements and the results obtained from the measurement campaign.
Chapter 5

5 A Literature Survey of MIMO Channel Capacity

5.1 Introduction
Analysis of MIMO channel models for high speed wireless networks is gaining immense interest. Although a vast amount of measurements exist for the mobile channel, measurements and characterization of MIMO channels are very recent and quite limited. There is considerable interest to model the MIMO channel based on empirical data based channel coefficients arranged in a matrix. There is a need to validate the theoretical formulas derived for MIMO capacity from measurements performed under different environments. The aim of this chapter is to present a literature survey on the different measurement campaigns used to characterize MIMO channel capacity and discuss the results. First the channel capacity formula and its dependence on the channel matrix is explained. The different experimental campaigns reported in literature are reviewed for their experimental set up and results obtained.

5.2 Channel Capacity
If we assume $N_R$ receive and $N_T$ transmit antennas. The capacity in bits/sec/Hz of a MIMO channel under an average transmitter power constraint is given by Foschini in [Fos96] as shown in equation 5.1.

$$C = \log_2 \left[ \det \left( I_{N_R} + \frac{\rho}{N_T} HH^* \right) \right]$$

(5.1)

where $C$ is the capacity, $I_{NR}$ denotes the identity matrix of size $N_R$, and $\rho$ is the average signal-to-noise ratio (SNR) at each receiver branch. The elements of $H$ are complex Gaussian with zero mean and unit variance; i.e. $H_{n_T n_R} \sim CN(0, 1)$ for $n_T = 1, 2, ..., N_T$, $n_R = 1, 2, ..., N_R$. $H^*$ is the Hermitian of $H$. Since $H$ is random $C$ will be random as well.
The underlying assumption in the formula is that the transmitted signal vector is composed of \( N_T \) statistically independent spatially separated equal power components each with a Gaussian distribution. According to the formula, capacity increases linearly with the number of antenna elements. Also for large number of antenna elements the capacity scales linearly with SNR, rather than logarithmically. The parallelism of the channel assumed here is not realistic as these channels can be coupled subject to fading. Since capacity is a function of the channel matrix, it is treated as a random variable. For a piecewise constant fading model and coding over independent fading intervals the expectation of the channel capacities gives the Shannon capacity of the random MIMO channel.

To present results Complementary Cumulative Distribution Functions (CCDFs) are usually computed for this random variable, for various antenna configurations. Capacity is measured in terms of outage probability, which represents the percentage of channels in which the capacity is greater than a given threshold. Outage probability indicates the confidence level. For example, CCDF outage probability of 99% means that 99% of channel realizations allow capacity that is greater or equal a given threshold. Capacity results are presented as a function of the signal-to-noise ratio for a given outage probability.

In most of the measurement campaigns described later the goal is to find the channel matrix \( \mathbf{H} \) to apply the channel capacity formula to compute the capacity and generate CDF or CCDF plots. This channel matrix is also used to develop and validate statistical MIMO channel models. A description of most of the experiments carried out and available in literature is described in the next section. The purpose here is to show the general procedure for performing MIMO channel measurements and discuss their results, which is also helpful in validating the VT-STAR testbed as an indoor MIMO channel measurement set up.
5.3 Literature review

5.3.1 MIMO channel capacity of a measured indoor radio channel at 5.8 GHz
In [Str00] the authors have considered an indoor environment to examine possible increase in MIMO capacity. Their investigation in the 5.8 GHz band applies to the HIPERLAN/2 standard. The affect of intra element spacing is also studied.

Description of system:
Data was collected with synthetic array antenna using one receiver and one transmitter that are synchronized. The antennas used were of monopole type. The measurements were made by moving the transmitter to seven different locations about 300mm apart which is about 6 wavelengths apart. For each transmit location the receive antenna was moved on a track to a position about a quarter of a wavelength apart between each position. For each combination of transmit and receive configuration 20 samples were taken. To make the narrow band measurements out of the wideband channel, discreet Fourier transform (DFT) was performed to divide it into 10 channels of 20MHz bandwidth which apply to HiperLAN/2 scenario.

Measurement set up:
Measurements were carried out in an office space with cubicles. Carrier frequency was 5.8 GHz with a bandwidth of 200MHz. Measurements were performed by transmitting PN sequences and correlating with the same synchronous sequence at the receiver.

Results:
Narrowband capacity results were presented, where it was shown that as the number of transmit antennas are increased to 3, the capacity increases as the rank of the channel matrix $H$. Figure 5.1 shows the plot of capacity versus SNR for different number of transmit antenna elements based on measured channel capacity matrix. The next two plots in Figure 5.2 and 5.3 shows channel capacity cumulative distribution function (CDF) for a SNR at 20dB. It was shown that for 2 receive antenna element case the capacity is between 9-10 bps/Hz and as the number of receive antennas increases to more than 3 there is only a logarithmic increase in capacity which reaches to 20-21 bps/Hz for the case of 9 receive antennas. In the next plot the capacity CDF was plotted.
for different inter-antenna element spacing ranging from quarter of a wavelength to twice the wavelength. It was seen that as the spacing increases the capacity approaches that of IID case where the received signals undergo independent Rayleigh fading. In these experiments the measurements were made with single receive antenna placed at different positions (wavelengths apart) which were then combined to make up a channel matrix for different number of array elements. The effect of the radiation patterns of one element on other elements in the transmit and receive arrays was not taken into consideration.

Figure 5.1 MIMO capacity for different SNRs with different number of transmitter elements

[Str00]
Figure 5.2 CDF plots of MIMO Capacity for different number of receivers and 3 transmitters
5.3.2 Investigation of multiple-input multiple-output (MIMO) channels in indoor environments at 5.2 GHz

In [Kai01] the channel characteristics of Multiple Input Multiple Output (MIMO) indoor systems at 5.2 GHz are studied. Their investigation shows that the envelope of the channel for non-line-of-sight (NLOS) indoor situations are approximately Rayleigh distributed and consequently a statistical description of the first and second order moments of the narrowband MIMO channel is described.
**Description of system:**

The measurements were centered at 5.2 GHz. The measurements were carried out using a vector sounder with an 8-element omni directional uniform linear array (ULA) at the transmitter side and an 8-element ULA with 120° beam width at the receiver side. A periodic multi-frequency signal with 120 MHz bandwidth was sent out by the transmitter and captured by the receiver. The channel impulse response was then sampled and saved in the frequency domain. For each transmit element, one ‘vector snapshot’ (one measurement from each receive element) is taken by the receiver through switching control circuits. The sampling time for one MIMO snapshot (8 vector snapshots) is 102.4_s. One complete measurement included 199 blocks with 16 MIMO snapshots within each block. The time delay between two neighboring blocks was 26.624ms. This means the total time for one complete measurement is 5.3s. During the measurements, people were moving around both at the transmitter and receiver side. The sampling of the received signals is not simultaneous for all channels and relies on the assumption that the channel is static for 16 snapshots.

**Measurement set up:**

The test site is a Building of the University of Bristol. The general layout of the test site includes office rooms, computer labs, corridors and open spaces. The entire measurements include 15 transmitter locations and 3 receiver locations. This paper presents results for non line of sight (NLOS) cases. The transmitter was located in a computer lab and the receiver was located in a large modern office with cubicles. The distance between two neighboring antenna elements is 0.5? for both arrays. There is a feedback from the receiver to the transmitter by a cable in order to synchronize the transmitter and receiver.

**Results:**

From the fitting of one channel coefficient from the measured data it was shown that for NLOS indoor MIMO environment the channel coefficient is approximately complex Gaussian. It was also shown that the channel covariance matrix can be approximated by the Kronecker product of the covariance matrices at the transmitter and receiver side respectively. A narrowband model for the NLOS indoor MIMO channel based on this second order statistical structure was proposed.
which gave channel capacity CDFs of the Monte-Carlo simulations matching closely to measured results as shown in Figure 5.4.

![CDF plots for measured and simulation of MIMO statistical model](image)

**Figure 5.4** CDF plots for measured and simulation of MIMO statistical model [Kai01]

### 5.3.3 Experimental characterization of the MIMO wireless channel at 2.45 GHz

[Wal01] presents we report the development of an experimental platform designed to measure the transfer matrix for indoor and outdoor MIMO channels.

**Description of system:**

The experimental platform uses a custom MIMO communications system operating between 0.8 and 6 GHz. The transmitter uses a digital pattern generator (DPG) to create N unique binary codes. These codes are fed into the custom RF chassis where they are mixed with a local oscillator (LO) to produce N distinct co-channel binary phase shift keyed (BPSK) signals. The
resulting signals are amplified to 0.5 W and fed into one of the N transmit antennas. The receiver uses a custom RF chassis to amplify and downconvert the signals from each of the M antennas. The resulting M intermediate frequency (IF) signals are low-pass filtered, amplified, and sampled using a 16-channel 1.25 Msample/s A/D card for storage on the PC. Two different antenna arrays have been constructed for the experiments. The first design is a 4-element dual-polarization patch array with half-wavelength element spacing. The second consists of a square metal plate with 10 monopole antennas placed at quarter wavelength apart. The carrier frequency was 2.45 GHz with a BPSK code rate of 12.5 kb/s and a 1000 bit PN sequence was used.

**Measurement set up:**
In this measurement campaign the receiver was placed in a large student computer lab and data was collected at 12 locations spaced by about 2 m. The transmitter was placed in a smaller room adjacent to the computer lab. Both the 4-element patch array and a 10-element linear array of monopoles were used for data collection. The raw data collected using the measurement platform was processed to obtain estimates of the time-variant channel matrix. The technique consists of 3 basic steps: (1) code search, (2) carrier recovery, and (3) channel estimation. The code search determines the alignment of the modulating codes. As shown in Figure 5.5 the method correlates the signal from one of the M receive Antennas with a baseband representation of one of the transmit codes. An FFT of this result produces a peak at the IF when the known code and the code in the receive signal are aligned.

A rough estimate of the intermediate frequency is then obtained from the peak of the FFT taken during the code search process. Following estimation of the frequency, the phase is recovered using the procedure shown in Figure 5.6. In this method, a recovery window is shifted along the despread receive signal at one sample increments. At each position, the signal is correlated against a complex sinusoid at the estimated IF frequency. The estimated phase at the center of the window is the angle of the complex result of the correlation. This phase estimate is finally smoothed by an averaging window.
Channel estimates for each MIMO channel is found by correlating with the known binary code. This is then used to form the channel matrix.

**Results:**
The capacity was plotted as a function of time as shown in Figure 5.7. Snapshots of data were collected which is the reason for jumps in capacity plots. Also shown is a histogram of capacity across all probing times and locations. Received signal correlations for this test site compared with Jake’s model was also presented as shown in Figure 5.8 which agree with the Jake’s model.
Receive correlation was computed by using the correlation coefficient of signals on receive antennas separated by a given spacing, over all probe times, locations, and transmit antennas. Complementary CDF of Capacity was plotted for 2x2 case for various polarization and compared to IID case as shown in Figure 5.9. The results show that polarization diversity performs better than spatial diversity as there is less correlation between orthogonally polarized signals. It can be seen that the capacity ranges from 11 to 13 bps/Hz. Capacity CCDFs per number of antenna for different number of antenna element used were also plotted as shown in Figure 5.10 where the total array length was fixed to 2.25\(\lambda\). The plot shows that as the number of elements increases the capacity per antenna decreases which can be attributed to the increased correlation as the antenna spacing decreases with increasing elements.

**Figure 5.7** Channel capacity as a function of time and histogram of channel capacity for all times and locations [Wal01]
**Figure 5.8** Signal correlation and comparison to Jake’s model [Wal01]

**Figure 5.9** Channel capacity CCDFs for different polarization [Wal01]
5.3.4 MIMO Radio Channels for Indoor Picocell Scenarios

The paper [Ker00] describes the set-up for the measurement of MIMO radio channels for indoor Picocell scenarios.

**Description of system:**
A 4x4 MIMO system was built. The transmitter uses a 1-to-4 switch with a switch time of 50 µs between each element of the antenna array, implementing a pseudo parallel transmission. The receiver consisted of four parallel Rx channels. Channel sounding measurements were performed every 20 ms at a carrier frequency of 2.05 GHz and a chip rate of 4.096 Mcps. The complex narrowband information was extracted from the wideband channel data.

The MS uses two trolleys. One trolley carried all the electronic hardware of the transmitter. The other one, referred as the "satellite", was equipped with a linear slide used to move the antenna array at the MS as shown in Figure 5.11. The two trolleys were connected by 10 m coaxial and
signal cables. The purpose of using two trolleys was to avoid any interference from metallic surfaces. The satellite trolley was made of wood and the metallic part of the linear slide was shielded by microwave absorbers. The height of the antenna arrays at the MS and the BS were 1.69 m and 2.34 m respectively. The measurements were made free from people moving around to investigate time stationary picocell environments.

The MS was moved along the slide over a distance of 9? , where ? is the wavelength. The measurement procedure is described as follows and illustrated in Figure 5.12. For a stationary position of the satellite, the antenna array moves forward for 5 s from A to B while the received signals are being recorded. When the array reaches the end of the slide (B) it is moved backward while the slide is moved perpendicularly to the motion of the array over a distance of 0.4 ?. Starting from C, a new set of measurements is then collected (C to D). This provides two sets of measurements for each MS location. The acceleration and deceleration phases of the array moving along the slide were disregarded from the measurement analysis.

Figure 5.11 MS “Satellite” during measurement
Measurement set up:
The measurement campaigns were undertaken within several buildings. Three different environments were selected for their different characteristics. The first environment, referred to as Novi2, provides an example of a building with several small offices on the same floor. The second environment, denoted Nokia, illustrates a typical modern open office environment. The last environment, denoted Novi3, is a reception hall. It provides a large open indoor environment with two floors which could easily illustrate a conference hall or a shopping galleria scenario. For each environment several MS locations were selected to provide a set of measurements where Line-Of-Sight (LOS) and Non-Line-Of-Sight (NLOS) were present. Moreover, several BS locations were selected in addition to the MS locations in order to increase the statistical information of the environment.

Results:
one of the goals of the measurement campaign was to evaluate the spatial correlation between several elements of a same antenna array for picocell scenarios. Figure 5.13 represents the empirical cumulative distribution function of the spatial power correlation coefficient computed over all the MS and BS locations for each environment. This includes 21 different locations considered for Novi2, 12 for Novi3 and 15 for Nokia which are names of locations used. The cdf
Figure 5.13 Spatial power correlation coefficient [Ker00]
of the spatial correlation between the elements are grouped into three categories with the same spacing (0.4 ?, 0.8 ? and 1.2 ?). The curves have to be read such that for instance when looking at Figure 5.13 (a), at 50% of the measured location for the environment Novi2, the spatial power correlation at the MS for each element separated with 0.4 ? is less than 0.3. These plots suggest that the spatial correlation for different antenna element separation is in between .2 to .4 with 50% reliability threshold.

Eigenvalue decomposition method is used to identify the number of independent channels corresponding to the instantaneous correlation matrix \( \mathbf{R} \) defined as \( \mathbf{R} = \mathbf{HH}^H \) where \( \mathbf{H} \) is the narrowband complex channel matrix and \( \mathbf{./}^H \) represents Hermitian transposition.

Simulated data sets were generated according to a two phase procedure. In Phase 1 \( \mathbf{R}_{\text{MS}} \) and \( \mathbf{R}_{\text{BS}} \) are mapped to the identity matrix. The measured complex Doppler spectra (with phase and magnitude information) of the MN paths \( h_{mn} \) are fed into the model. This is a first validation of the model with respect to the implementation of the fading. In Phase 2 the true average spatial power correlation matrices \( \mathbf{R}_{\text{MS}} \) and \( \mathbf{R}_{\text{BS}} \) are applied to the model. MN i.i.d. variables with amplitude shaped by the average Doppler power spectrum and random phase uniformly distributed over \([0,2\pi]\) are generated by the model.

The cdf of the channel envelope \( h_{mn} \) and the eigenvalues \( ?_k \) (not the wavelength ? ) for a full run of the transmitter along the linear slide are displayed in Figure 5.14 for positions A and B respectively.

Measured and simulated results are both presented on the same graph. The eigenvalues are normalized to the mean gain value of a single transmit and single receive element \( h_{mn} \) of the channel matrix \( \mathbf{H} \). The fact that there are distinct eigenvalues in this 4x4 scenario demonstrated that the array elements at both the BS and MS were decorrelated and hence parallel subchannels were achieved within the investigated picocells with only 0.4 ? separation. Simulated and empirical cdf’s of the channel envelope fit well with the Rayleigh distribution reference line. This shows that for the two cases the channel is almost Rayleigh distributed. The simulated phase 1 fits perfectly well
with the measured cdf in both figures. From simulated phase 2, it can be seen that the simulated results are close to the measured ones but not perfectly.

![Figure 5.14](image)

**Figure 5.14** Empirical cdf of narrowband channel envelope and the eigenvalues for pos A and pos B (•: hmn, o: measured ?, continuous line: simulated phase 1, dashed line: simulated phase 2, thick dash-dotted line: Rayleigh distribution reference). [Ker00]

### 5.3.5 Multiple-input multiple-output (MIMO) outdoor radio channel measurements

In [Mar01] the authors present the results of the first field test to characterize the MIMO channel in a mobile environment. A 4x4 system was used with over a 30KHz bandwidth channel to show capacity improvements in suburban, highway and pedestrian environments.

**Description of system:**

The test system comprised of 4-branch base station receiver with roof top antennas and 4 coherent 1W 1900 MHz transmitters at the mobile with antennas mounted on a laptop computer. The rooftop antennas used were dual-polarized spatially separated antennas separated by 20 wavelengths. While for the mobile a dual-polarized array was considered with monopole elements which were placed half wavelength apart. The bandwidth of the system used was 30 KHz. Separate orthogonal bit and frame synchronous 8-symbol Walsh sequences were
transmitted from each transmitter antenna element. The symbol rate was 24.3 Ksymbols per second. Real-time baseband signal processing was performed using 4 TI TMS320C40 DSPs for timing recovery and symbol synchronization at the receiver.

**Measurement set up:**
Drive tests were conducted in a suburban environment in drive ways, parkways and parking lots for pedestrian environment. The vehicle speed in driveway was around 30mph and in parkway around 60mph and pedestrian tests were conducted by walking in different parking lots. At the receiver complex correlation of 16 channels corresponding to 4 transmit waveforms at each receive antenna was recorded at 3038 (24300/8) samples per second. The capacity and fading channel correlation of these measurements were calculated offline by analysis.

**Results:**
Normalized capacity with respect to a single channel was calculated by dividing the expression for capacity by the average capacity of a single channel. The average capacity of a single channel was calculated by averaging the capacity of the 16 measured channels. This averaging is valid as long as the channel powers are assumed to be approximately equal in each channel. The normalized capacity does not depend on the SNR. In their analysis however the SNR was fixed to 20 dB. It was also shown by simulation that for iid Rayleigh distributed fading channels that the instantaneous normalized capacity CDF variation is small compared to that averaged over many fades as shown in Figure 5.15.

The capacity and correlation values were computed by averaging over 1 second. Figure 5.16 shows the normalized capacity and correlation plots averaged over time for drive way and parkway respectively. They show a capacity of 4 times a single channel as predicted in the theoretical model. In Figure 5.17 the normalized capacity and correlation plots for outdoor to indoor measurements is shown. Here again the capacity is seen to be 4 times a single channel even when the correlation is as high as .5. This shows that the channel capacity does not vary for a mobile user to a pedestrian user. The reason sited is because the channel capacity is averaged over 4 received signals compared to a single received signal in a one antenna case. Also in [Ges00] the channel capacity is shown to depend on the rank of the channel matrix which may be
high in these scenarios. Finally the CDF plots for the measured capacity were shown as in Figure 5.17.

Figure 5.15 Capacity CDFs [Mar01]
Figure 5.16 Normalized capacity and correlation plot over time for driveway and parkway respectively [Mar01]

Figure 5.17 Normalized capacity and correlation for pedestrian plot and CDFs for all three cases [Mar01]
In [Sol01] measurements were also performed using multi-beam antennas. The equal power assumption on each of the 16 channels on an average no longer holds for this case and hence the average capacity was taken as $\frac{1}{4}$ times the capacity of the strongest beam. Therefore the estimated capacity has a significant variance which results in increased spreading of the normalized capacity distribution. This is seen in capacity results summarized by CDF plots in Figure 5.18. Figure 5.19 shows the various results of capacity and correlation for different types of polarized multi-beam antennas used at the receiver. It was seen that when the transmitter is in one beam the capacity reduced to 2 while it increased to 3 or 4 when the transmitter was in between beams. This shows that lower correlation of received signals affects the capacity of the system and a multi-beam scenario performs worse in terms of capacity. It was also shown that the type of antenna used at the laptop for polarization and diversity does not significantly affect capacity.

![Normalized capacity CDFs for different directional antenna configurations](image)

**Figure 5.18** Normalized capacity CDFs for different directional antenna configurations [Sol01]
Figure 5.19 Normalized Capacity and correlation for different directional antenna configurations
5.3.6 MIMO channel capacity for fixed wireless: Measurements and Models
In [Xu01] the authors have tried to verify the capacity for MIMO channels through measurements taken for fixed wireless channels.

Description of system:
The narrowband system comprised of a linear horizontal array with 5 antennas. Each antenna element is a panel antenna with 13 dB gain. The carrier frequency used is 2.44 GHz. The spacing between elements is .52 m. at the receiver both vertical and horizontal linear arrays with 4 elements each with 15 dB of gain.

Measurement set up:
The measurements were performed in 16 locations in the suburban environments. The transmitter is set up at antenna height of 35 m and the receiver at 10 and 5 m.

Results:
The CDF plots for both 10 m and 5 m heights and different number of receive antenna elements was obtained as shown in Figure 5.20. The measured capacity ranges from keyhole to Rayleigh iid case. A keyhole is described as a MIMO channel matrix with lowest rank. It was shown that the horizontally oriented arrays provide a higher median capacity than vertically oriented array for 10 m receiver height. This indicates high angular spread in the horizontal direction and a narrow angular spread in vertical direction and hence high correlation in vertical direction. It was also shown that at 5 m both cases had comparable capacities which indicate that at 10 m there was more chance of LOS to the transmitter. It was also noticed that at lower antenna heights the total received signal power reduces, but the received signal becomes less correlated. With normalized $H$ matrices and given SNR, the overall system capacity is higher at lower antenna height. The loss of capacity due to received power loss was observed to be larger than the increase of capacity due to scattering. Finally it was observed that the capacity does not grow linearly with increase in number of receive antennas. For a 4x5 system with horizontally oriented antennas the capacity was observed to be 60% of the capacity of Rayleigh iid case.
5.3.7 Measurement and Characterization of Broadband MIMO Fixed Wireless Channels at 2.5 GHz

In [Bau00] the authors have discussed the measurement results for a cellular broadband fixed wireless channel. These include results on the Ricean K-factor, cross polarization discrimination and doppler spectrum.

Description of system:
A coherent 2x2 MIMO channel measurement system was implemented spanning a bandwidth of 4 MHz. The operating center frequency was 2480 MHz. The system is based on swept frequency sounding in which a narrowband signal is swept in discrete steps across a 4 MHz frequency band. This is done synchronously with the transmitter with reference clock derived form rubidium clocks. Distinct transmitted signals are generated for all antennas using time and frequency multiplexing. The two independent 2x2 MIMO channel responses were recorded at the receiver independently. The recorded channel response data is streamed to a hard disc for

**Figure 5.20** Channel capacity for 4 and 7 receiver arrays at 10m and 5 m elevation [Xu01]
post processing off line. The receive antennas were dual-polarized with slanted polarizations +/-45° and a gain of 12 dB and an azimuthal beamwidth of 90° which was mounted on a retractable mast. At the transmitter a directive antenna with a beamwidth of 90° and a gain of 70 dB was used which is a standard configuration in mobile cellular systems. The antennas separation between transmitter elements was 1.8 m (15 wavelengths).

**Measurement set up:**
The measurements were carried out outdoor in a suburban environment with the transmitter antennas mounted on a van.

**Results:**
Often for a radio environment the time varying envelope of the composite path gain has a Ricean distribution. The ratio of the fixed and fluctuating power components is defined as the K-factor. The K factor varies with frequency and location. This was shown in the measurement results. It was also shown that with increase in distance between the transmitter and receiver the K-factor decreases also with reduction of height of the transmitter.

It was also shown that the cross polarization discrimination (XPD), which is the ratio of the power received by an antenna with equal polarization orientation as the transmit antenna to the power received by an antenna with cross polarization orientation to the transmit antenna, decreases with distance.

**5.4 Summary**
It can be seen that most of the measurement results were reported between 2000 and 2001 when the VT-STAR was built and the MIMO channel characterization was in the process. At the time it was important to perform measurements to see the MIMO capacity improvements achievable for different environments on actual measured data and validate theoretical results. Some of the salient features of the measurement campaigns reported were that almost all the measurements needed some kind of channel sounder and transmission of orthogonal signals from each antenna element at the transmitter which could be correlated at the receiver to derive the channel matrix.
The measurements were performed for narrowband channels. Measurement results have been shown for indoor, picocell and outdoor environments and for different polarizations. The VT-STAR measurement effort tries to characterize the channel matrix for indoor environment through the detection of orthogonal space-time coded symbols which are used to find the channel estimates. The next chapter describes the modified VT-STAR system for channel measurement and presents the results which validate many if the results presented in literature.
Chapter 6

6 MIMO Channel Measurements

6.1 Introduction
In the last chapter it was seen that higher capacity for MIMO channels suggested in theory needs to be validated for different wireless environments namely indoor, outdoor and frequency selective environments. The MIMO channel capacity formula depends on the rank of the channel matrix which in turn depends on the correlation properties of the received signal. This can only be evaluated by taking actual measurements in different environments. In this chapter, the use of VT-STAR testbed for MIMO channel measurements is explained. The measurements are described for indoor channel environment in the Industrial Scientific and Medical (ISM) band. The results from measurements are then discussed to show the increase in capacity in a wireless indoor scenario and compared with single input single output (SISO), single input multiple output (SIMO) and multiple input single output (MISO) cases.

6.2 VT-STAR in Snapshot Mode
In the snapshot mode, the receiver DSP is used as a data acquisition device. A flow diagram of the signal processing is depicted in Figure 6.1. The C67 collects raw received signal samples into buffers and dumps the buffers into the host PC using the real-time data exchange (RTDX) capability provided by the DSP EVM board. The stored data is retrieved by MATLAB and post-processed to characterize the channel.

6.2.1 Data Acquisition
In order to collect snapshots of data, the C67 uses its RTDX utility to perform transfer of data from the target (DSP) to the host (PC) without affecting other real-time operations on the DSP which is shown in Figure 6.2. The RTDX utility provides API commands to set up an RTDX channel between the DSP and the PC. Received signals sampled in real time are stored in a buffer in the DSP. When the buffer is full it is passed to the target RTDX library in the form of messages consisting of a group of words. The target library then sends one message at a time to
the host RTDX library using low priority message interrupt (MSGINT) to interrupt the DSP to start RTDX communication with the host. This transfer takes place over the JTAG interface on EVM board. The debugger controls the host RTDX library such that the received messages at the host are stored in a log file.

![Diagram of VT-STAR receiver in snapshot mode](image)

**Figure 6.1** VT-STAR receiver in snapshot mode

The functionality of the RTDX utility as a data acquisition utility relies on data not being lost or overwritten. This is done by making sure that the DSP load is less and making it free from processing during the transfer of data to the host.

The data acquisition buffer depth is set to collect snapshots of 1200 samples. Four words corresponding to one in-phase and quadrature sample from antenna 1 and 2 are stored in the buffer at each hardware interrupt from the ADC. After filling up this buffer, this data is transferred to the RTDX target library in the form of messages each consisting of ten, 32 bit words. Before initiating this RTDX transfer, the ADC interrupt is disabled hence making the DSP load lesser for the transfer to take place. A clock interrupt is generated every 1ms period, which sets up the RTDX channel transfer. This period is sufficient to ensure complete transfer of 10 data samples which is one message from the target to the host library using RTDX. This was made sure by performing many data transfers and checking the data collected at host by post-
processing in MATLAB. The ADC hardware interrupt is re-enabled after completion of data transfer of all the 1200 data samples in the buffer.

![Diagram of RTDX in snapshot mode](image)

**Figure 6.2** RTDX in snapshot mode

At the host, the received data is stored in a file of .rtd format. After passing the predetermined number of recorded samples the RTDX channel is disabled. The passing of data to host is monitored on the host debugger through the message log display using real time analysis (RTA) tools. The .rtd log file is played back by the code composer utility and a COM C++ application program running simultaneously on the host converts this file into a binary format. This binary file contains all sample values recorded from the ADC, and is used for post processing by the MATLAB™ software.

### 6.2.2 Post Processing

To do post processing and get meaningful results of channel capacity the channel fade coefficients need to be estimated. The VT-STAR transmitter transmits D-STBC symbols which are orthogonal in space. This fact is taken into consideration and for easy channel estimation it is
necessary to transmit a reference symbol which can be correlated at the receiver. To do this the transmitter always uses the same QPSK symbol as input to the D-STBC scheme and hence the transmitted symbols follow a particular pattern. This way the symbols at the receiver are correlated with the reference set generated by the transmitter to find the symbol timing to perform channel estimation.

The post processor operates on the raw samples by passing them through a matched filter, which again is the same used at the transmitter, removing residual frequency offsets between transmitter and receiver clocks and performing correlation processing to extract the channel fade coefficients. Once the channel matrix is obtained, it is embedded into the calculation of the channel capacity formula given in chapter 5 for different antenna configurations (i.e., single antenna system, transmit diversity, receive diversity and MIMO channel)

### 6.3 Description of system

The transmitter array described in the architecture for VT-STAR in chapter 3, radiates synchronized pulse shaped QPSK symbols, encoded by a full-rate space-time block code. The bit rate for the measurements reported herein is set to 6.7 Kbps. The orthogonality introduced by the space-time block code is exploited at the receiver to separate the simultaneous transmitted signals. The data collection scheme is based on the real-time data exchange (RTDX) capabilities of the TI C67 DSP. The scheme allows for alternate periods of data collection and RTDX-based data transfer from the target DSP to the host PC for storage and post-processing. This process is illustrated in Figure 6.3

![Figure 6.3 Data collection timing](image)

96
Sampling period = 100 µs

T1 corresponds to a measurement block of 300 samples x 100 µs = 30 msec.

T2 corresponds to RTDX data transfer time of

120 messages x 1ms (timer interrupt interval) = 120 msec.

Number of snapshots per location = 20

Total time period for measurement at one location = (120 + 30) ms x 20 = 3000 ms = 3 s

Number of ADC channels = 4

Total number of samples stored = 4x300 =1200

Size of each sample stored in memory = 4 bytes

Memory required to store data per location =1200 x 20 x 4 = 96000 Bytes.

The system is capable of making longer measurements by increasing the number of snapshots.

Typically in a static indoor environment the RMS delay spread is in the range of 25ns to 94 ns on an average [Rap96]. Also in a static indoor environment the channel undergoes flat fading. This measurement campaign focuses on static indoor environment with no movement between transmitter and receiver. Hence collection of 3s of channel estimates gives a good representation of the channel for a particular location. Taking measurements from multiple locations gives many realizations of the indoor wireless environment to calculate the capacity achievable with MIMO application.

The functionality of the complete system excluding the RF hardware is validated by connecting the baseband processing units on both sides of the link in a back-to-back manner and collecting data in this setting. The setup is shown in Figure 6.4. The principle behind this testing is to estimate and validate the channel gains.
Figure 6.4 Back-to-back testing for verification of channel estimation

Figure 6.5 presents the estimated squared channel gains for the back-to-back configuration. The path gains $h_{11}$ and $h_{22}$, which represent the uncoupled LOS single-input single-output channels are constant and centered at 0dB while the cross-channels $h_{12}$ and $h_{21}$ are 25dB down since they are not connected in the testing and are represented by noise. This confirms that our data collection mode is functioning correctly.

The mutual coupling between antennas can change the antenna pattern of each element, in an array, in free space. The change in antenna pattern tends to decrease the correlation between the received signals between two closely spaced antennas [Vau93]. The measured radiation pattern plot shown in Figure 6.6 corresponds to a dipole antenna element in a 2-element array with inter-element distance of 0.5 $\lambda$ (elements marked with X) [Die01]. It is assumed that the same general pattern would hold for a monopole on a ground plane as used in VT-STAR testbed. The radiation pattern for the other element will be a mirror image of the pattern shown here. In [Die01] it was reported that in practical systems each antenna has a different pattern due to pattern distortion caused by mutual coupling. Therefore relative weights of each of the multipath components received by each antenna is different even when they are spaced closely and when their phases are similar. This reduces the probability that received signals at both the antennas would be in fade simultaneously for closely spaced antennas. It was also shown that the square of the correlation of the complex antenna pattern is less than the omnidirectional assumption which
varies as the square of the Bessel function of the electrical antenna spacing. Hence the resulting pattern distortion as seen in a practical system is applicable to the VT-STAR setup and in turn would affect propagation characteristics and consequently diversity performance experiments of the multiple element antenna (MEA) system.

**Figure 6.5** MIMO channel estimations using VT-STAR in back-to-back testing mode

**Figure 6.6** Measured and modeled antenna pattern [Die01]
6.4 Measurement set up:

This thesis reports the measurement campaign carried out to characterize the MIMO channel performance in an indoor environment. The measurements were carried out in 3 locations; 478 MPRG DSP lab, 476 MPRG student cubicle area, and the Durham Hall 4th floor corridor. Figure 6.7 shows the lay out of the 4th floor of Durham hall and the sample locations of the transmitter (Tx) and receiver (Rx). The green dot suggests the location of the transmitter and the red location suggests the location of the receiver. For each campaign the transmitter or the receiver was moved to adjacent positions separated by a few feet and data was collected as explained in section 6.1 and 6.2. This was done to get a good spatial average of the MIMO indoor environment. In all the measurements taken the channel was quasi static as there where no objects or people moving between the transmitter or receiver. The next section discusses the results and observations of measurements performed in each campaign.

Figure 6.7 Floor plan of fourth floor Durham Hall
6.5 MIMO Channel Capacity Measurement Results

In the first measurement campaign measurement had a line of sight set up inside the MPRG DSP lab. This is shown by the green and red dot as seen in Figure 6.7. The transmitter and receiver antenna element axis were kept in line separated by 72 inches as shown in Figure 6.8.

![Figure 6.8 Transmitter and receiver positions](image)

The estimated channel envelope profiles as shown in Figure 6.9 reveals that the environment is stationary and that the order of the MIMO channel estimates follows the following pattern:

\[ |h_{22}| > |h_{21}| > |h_{12}| > |h_{11}|. \]

That is, the channel gains from transmit antenna 2 are stronger than the corresponding gains from transmit antenna 1. This is in agreement to what is expected due to the nature of pattern distortion for inline orientation as explained earlier. This validates the performance of the VT-STAR setup for over the air measurements.

For the second measurement campaign the transmitter was placed on one side of a dry-wood column and the receiver placed behind the column as shown in Figure 6.7. Figure 6.10 presents measured capacity in this NLOS environment with SNR of 20 dB for each one of the single-input single-output (SISO) links \((h_{11}, h_{12}, h_{21} \text{ and } h_{22})\), compared with the capacity achieved by employing MIMO configuration.
The second campaign was for a NLOS environment where the transmitter was kept behind a dry-wood column as shown in Figure 6.7. The third campaign was in the MPRG student computer lab where the area is divided into cubicles. The cubicles have a metal mesh inside which provides sufficient attenuation to signals at 2.05 GHz and hence can be considered NLOS environment. The fourth measurement campaign was carried out in the corridor of the 4th floor of Durham Hall. In this set up both LOS and NLOS environments where achieved for locations shown in Figure 6.7.
Next a comparison of the capacity of the MIMO channel with the capacity achieved by a single-input multiple-output (SIMO) channel with either optimal combining (OC) or diversity selection (DS) criterion, multiple-input single-output (MISO) channel employing transmit diversity only and single-input single-output (SISO) channel is shown in Figure 6.11. It illustrates the measured histograms for these cases. MIMO channel capacity outperforms receive (SIMO) or transmit diversity (MISO). Note that receive diversity outperforms transmit diversity due to the constraint of same total radiated power in both schemes. In the transmit diversity case, power is distributed equally across transmit antenna elements, resulting in lower effective SNR at the combiner output. Also optimal combining performs better than selection diversity in a SIMO case as should be the case.
In the second phase of this measurement campaign to get many realizations of the environment to plot the CCDF of capacity of SISO, SIMO, MISO and MIMO channels, measurements were collected by moving the receiver to different locations and taking 20 snapshots at each location. As shown in Figure 6.12 the transmitter was kept behind the dry wood column. The receiver was moved to different locations as marked by numbers in the figure. Also the orientation of the receiver antennas was changed for measurements from locations 16 through 20 though the have the same locations as 3, 4, 9, 10 and 15. The axis of the two element array coincides with base of the triangle representation for transmitter and receiver.

Figure 6.11 Capacity histogram comparisons for SISO, SIMO (optimal combining and selection diversity), MISO, and MIMO channels
Figure 6.12 Transmitter and receiver positions for the measurement campaign inside MPRG DSP Lab

Figure 6.13 shows the estimated channel envelope profiles recorded over 20 snapshots per location for 20 locations which gives a total of 400 snapshot average values for the channel coefficients.

The channel coefficients were used in computing the channel capacity for MIMO channels, as derived by Fochini and Gans [Fos96] in equation 5.1, to plot the complementary cumulative distribution function (CCDF) of the capacity for the DSP lab indoor scenario. The single input single output (SISO), single input multiple output SIMO, multiple input single output MISO and MIMO scenario CCDF plots derived from measurements in the MPRG DSP lab are compared in Figure 6.14. It can be seen that the MIMO channel always has a capacity greater than 8 bps/Hz compared to SISO, SIMO and MISO channels. This conforms with other measurement campaigns reported in literature for indoor environment. [Kai01], [Ker00], [Stri00].
Figure 6.13 Channel coefficients for MPRG DSP lab MIMO measurements
The third measurement campaign was carried out to measure the non line of sight (NLOS) MIMO capacity gains in the MPRG student cubicle area. The locations of the transmitter for different snapshots are shown by numbered triangular representation with red color in Figure 6.15. The receiver was placed between two cubicles as shown by the green triangle. Measurements were taken sequentially from location 1 through 11. The distances are marked in inches in the figure.

Figure 6.14 Indoor capacity CCDF plots NLOS indoor MPRG DSP lab scenario
Figure 6.15 MIMO channel measurement campaign: MPRG student cubicle area layout

Figure 6.16 shows the estimated channel envelope profiles recorded over 20 snapshots per location for 11 locations which gives a total of 220 realizations of the channel. The channel capacity CCDF comparison plots for the cubicle area are shown in Figure 6.17. It can be seen that the MIMO channel capacity is almost all the time greater than 8 bps/Hz and achieves a maximum capacity of 13 bps/Hz. Also SIMO performs better than MISO case as the power of the transmitted signal is divided equally among both antennas at the transmitter for the MISO case and hence the received signal has lower SNR compared to SIMO case.
Figure 6.16 MPRG cubicle area MIMO channel estimates

Figure 6.17 Capacity CCDF plots for channel measurements in MPRG labs cubicle area
The fourth measurement campaign was carried out in the corridor of the fourth floor of Durham Hall. The measurement set up is shown in Figure 6.18. As can be seen the measurements have both LOS and NLOS components. The walls are made of concrete stones and the transmitter was moved to different locations as marked in the figure.

Figure 6.18 MIMO channel measurement set up: Durham Hall 4th floor corridor

Figure 6.19 and 6.20 show the estimated channel coefficients for both LOS and NLOS cases respectively. The channel coefficients for LOS have a higher average value compared to NLOS as is expected due to dominant line of sight signal component.
Figure 6.19 Estimated channel coefficients for LOS measurements on 4th floor corridor of Durham Hall

Figure 6.20 Estimated channel coefficients for NLOS measurements on 4th floor corridor of Durham Hall
Figure 6.21 and 6.22 show the CCDF comparison plots for both LOS and NLOS cases respectively. On comparison it can be seen that LOS MIMO performs better than other schemes with a channel capacity greater than 7.5 bps/Hz. In the NLOS case the capacity is greater than 8.5 bps/Hz. This expected as NLOS would have less correlation and hence a resultant higher MIMO channel capacity. It is interesting to note that in the corridor LOS environment the signals are less correlated to provide MIMO channel capacity gains. This can be attributed to the strong diffuse components reflected from the walls.

![Capacity CCDFs for LOS measurements on Durham Hall 4th floor corridor](image_url)
6.6 Summary

Modification of VT-STAR testbed to take channel measurements was explained in this chapter. The validation of channel estimation method was shown for both back-to-back and over the air measurements. Channel measurement campaign set-up and the indoor environments where the measurements were taken were explained. The channel measurement results were displayed in terms of capacity CCDF plots and a comparison was made between SISO, SIMO, MISO and MIMO channels. As seen from the plots it can be concluded that MIMO channels present significant improvement in capacity compared to other diversity schemes in an indoor quasi static environment. This is even true in a LOS indoor environment as shown by measurement results.
Chapter 7

7 Conclusions

An overview of STBC schemes was presented in this thesis with an emphasis on D-STBC, followed by a general system overview of the VT-STAR. The system design issues involved in developing a DSP based prototype was presented. The transmitter and receiver sections of VT-STAR were examined in detail, outlining some of the challenges and design issues that needed to be resolved in the development of this prototype. The VT-STAR prototype was modified to make it capable of performing multiple tasks like real-time communications and measurement through the modification of software. Results from the operation of VT-STAR were presented, showing not only that VT-STAR is a functional test-bed, but also showing that there are clear improvements in a wireless link’s capacity and reliability through the use of MIMO technology. Finally, VT-STAR is designed to allow the expansion of its capabilities by modifying algorithms in DSP and will serve MPRG research for years to come.

7.1 Future Research Directions

The current test bed has been used to demonstrate channel capacity improvements in indoor quasi static flat fading environments. In all the measurements the channel was static with no movement of people or objects between the transmitter and receiver. The system can be modified to take longer duration measurements to characterize a dynamic environment with people moving in a hall. To analyze the performance in fast fading environment the dual monopole elements of the receiver can be mounted on a track run by a motor at a known speed and the measurements can be made by connecting long cables from the antennas to the current receiver. Other improvements include addition of multiple antenna elements and expansion of hardware to support various smart antenna and space time coding algorithms. The channel measurements from such a system can aid design of a hybrid system which can switch between beamforming and space-time coding depending on the state of the channel. Closed loop transmit diversity schemes can also be tested by developing a wire line feedback mechanism connecting from the receiver DSP to the transmitter DSP. Also effects of imperfect feedback and imperfect channel
estimates can be studied in such a system. The current VT-STAR system is limited in bandwidth as it uses one DSP to perform all the baseband processing. To analyze a wideband system for effects of frequency selective fading a faster DSP board is required.

As can be seen the VT-STAR test bed is flexible and provides a platform to develop algorithms and test them. It can also be used to take channel measurements for different environments which can enable simulation and analysis of BER performance of MIMO channels for different processing schemes.

Despite recent progress, MIMO research is largely immature and contains a number of unsolved problems in diverse areas as channel modeling, communication theory, signal processing and cellular applications. This thesis work has made an attempt to realize MIMO STBC scheme in real-time and characterize the MIMO indoor channel for actual capacity improvements. The following papers are the outcome of this effort.

- MIMO Channel Capacity Measurements Using the VT-STAR Architecture; R. Gozali, R. Mostafa, R.C. Palat, P.M. Robert, W.G. Newhall, B.D. Woerner and J.H. Reed submitted to VTC Fall 2002
- R. Mostafa, R. Gozali, M. Robert, R.C. Palat, B.D. Woerner and J.H. Reed; Virginia Tech Space-Time Advanced Radio: A DSP-Based Multiple Input Multiple Output System Prototype; submitted EURASIP journal on Applied signal Processing
Appendix

The actual pictures of the VT-STAR test bed.

VT-STAR transmitter DSP & RF front end

Transmitter baseband unit
Transmitter RF front end with 4 DACs

VT-STAR receiver
Receiver RF front end, 4 channel ADC and DSP inside PC chasis
8 BIBLIOGRAPHY


[Adc00] Designing With the THS1206 High-Speed Data Converter Application Report SLAA094 - April 2000


[Emi00] TI, TMS320C6000 EMIF to External Asynchronous SRAM Interface Application Report SPRA542A


[Ths01] TI, THS5661EVM for the THS5661A/51A/61A/71A 8-,10-,12-,and 14-Bit CommsDAC™ Digital-to-Analog Converters SLAU32B

[Tms00] TMS320C6701 Floating point digital signal processor SPRS067E May 2000

[Tms01] TI, TMS320C6711 TMS320C6711B TMS Floating point digital signal processor SPRS067E September 2001


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