ON THE CIRCUIT ORIENTED AVERAGE LARGE-SIGNAL MODELING OF SWITCHING POWER CONVERTERS AND ITS APPLICATIONS

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ABSTRACT

A systematic and versatile method to derive accurate and efficient Circuit Oriented Large Signal Average Models (COLSAMs) that approximate the slow dynamics manifold of the moving average values of the relevant state variables for Pulse-Width Modulated (PWM) dc to dc and three-phase to dc power converters is developed. These COLSAMs can cover continuous conduction mode (CCM) as well as discontinuous conduction mode (DCM) of operation and they are over one order of magnitude cheaper, computation wise, than the switching models. This method leads primarily to simple and effective input-output oriented models that represent transfer as well as loading characteristics of the converter. Since these models consist of time invariant continuous functions they can be linearized at an operating point in order to obtain small-signal transfer functions that approximate the dynamics of the original PWM system around an orbit.

The models are primarily intended for software circuit simulators (i.e. Spice derived types, Saber, Simulor, etc), to take advantage of intrinsic features such as transient response, linearization, transfer function, harmonic distortion calculations, without having to change simulation environment. Nevertheless, any mathematics simulator for ordinary differential equations can be used with the set of equations obtained through application of Kirchhoff’s laws to the COLSAMs. Furthermore, the COLSAMs provide physical insight to help with power stage and control design, and they allow easy interconnection among themselves, as well as with switching models, for complete analysis at different scales (time, signal level, complexity; interconnectivity).
A new average model for the Zero-Voltage Switched Full-Bridge (ZVS-FB) PWM Converter is developed with the above method and its high accuracy is verified with simulations from a switching behavioral model for several circuit component values for both CCM and DCM.

Intrinsic positive damping effects and special delay characteristics created by an energy holding element in a saturable reactor-based Zero-Voltage Zero-Current Switched Full-Bridge (ZVZCS-FB) PWM converter are explained for the first time by a new average model. Its large signal predictions match very well those from switch model simulations whereas its small-signal predictions are verified with experimental results from 3.5 kW prototype modules. The latter are used in a multi-module converter to supply the DC power bus in and aircraft. The design of control loops for the converter is based on the new model and its linearization.

The ZVZCS-FB PWM converter’s average model above is extended to deal with interconnection issues and constraints in a Quasi-Single Stage (QSS) Zero-Voltage Zero-Current Switched (ZVZCS) Three-Phase Buck Rectifier. The new model reveals strong nonlinear transfer characteristics for standard Space Vector Modulation (SVM), which lead to high input current distortion and output voltage ripple inadmissible in telecommunications applications. Physical insight provided by this average model led to the development of a combined modified SVM and feed-forward duty-cycle compensation scheme to reliably minimize the output voltage ripple. Experimental results from a 6 kW prototype validate large signal model for standard and modified SVM, with and without duty-cycle compensation scheme.
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To

Ligia,

Maria Fernanda

and

Miguel Eduardo
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1. **INTRODUCTION**

1.1. **Motivation and Goals**

Switching power converters have become ubiquitous in consumer products as well as in industrial, medical, and aerospace equipment due to their high efficiency, low volume and weight, fast dynamic response, and low cost. Even though extensive efforts and resources are continuously devoted to new component technologies and converter design, the development of versatile modeling techniques suitable for general switching power converters is still lagging.

This dissertation aims at reducing that gap by providing a systematic approach to the development of accurate and computationally efficient but still intuitively simple circuit oriented, average large-signal models for pulse-width modulated (PWM) full-bridge (FB) derived, dc to dc and three-phase to dc power converters. Since a large number of new converter topologies based on these structures have emerged lately, versatile and reliable models are needed to speed up exploitation of their full potential.

The objectives of the circuit oriented, continuous-time, large-signal average models developed here are, besides allowing very fast simulation times and reduced memory space with respect to discrete and switching models, to gain physical insight, to guarantee complete representation of large and small-signal behavior and to overcome limitations of existing average models by including discontinuous conduction mode (DCM) and continuous conduction mode (CCM) operation and storage element effects in the form of algebraic and/or dynamic constraints to handle large and asymmetric ripple components as well as feedback loops. This approach makes the new models very useful in large signal analysis and design of single-stage single and multi-module converters, as well as multistage converters, together with their respective input and output filters. In addition, the new models can be linearized at an operating point to derive a small-signal model that closely approximates the behavior around an orbit for the original system, and hence, provides a solid starting point for control design. As a result, thorough studies of
interaction effects and trade-offs amongst power stage(s) and filter(s) structures, current and voltage ripple, harmonic distortion, modulation scheme, control loop(s), stability, transient response, to name a few, can be conducted.

The systematic modeling procedure allows for easy adaptation of the models to perform analyses at different scales, such as time, signal level, complexity, interconnectivity. Model extension for hybrid simulation, i.e. mixing of average and switching models, can be easily carried out to accelerate analysis of specific subsystems in multi-stage and/or multi-module converters.

Even though the new circuit oriented average models can be used with any commercial mathematics software that allows simulation of ordinary differential equations, one of the major motivations for this work is to take advantage of common features in commercial circuit simulators, i.e. transient response, linearization, transfer function, harmonic distortion calculations; to help with power converters analysis and design issues without having to change simulation environment.

1.2. Literature Review

Most of the references mentioned in this work have excellent reference lists therein, which are also assumed referenced and that are omitted here for compactness.

Switching power converters can be mainly classified according to the type of input (ac or dc) and output (ac or dc) variables [E5, M7]. Further classifications with respect to parameters such as control variable, PWM, or frequency modulation, [E5, M7], waveform, i.e. piece wise linear or resonant [E5, M7], switching stresses, i.e. hard or soft [E5, J4, M7, H3, V6, V7], among others, are well known.

Most common PWM power converters have switch transitions determined by control and state variables through constraint equations [B6, B11, B12, C5, C7, C8, C20,
E1, E3, E5, F1, G1, H6, K7, L2, M7, O3, S4, T8, V3, X2], and in between those transitions the converters are very accurately described by linear autonomous ordinary differential equations. Sampled-data models [A1, B6, B12, F1, G1, G3, H4, L2, L13, L15, M5, P1, T7, V3, V4] are suitable to represent and to simulate these converters at switching instants, but they lack information between samples and are computationally expensive. However, the closed-loop operation can be accurately described and characterization (Poincare maps) of iterative maps for instability, bifurcation and chaotic behavior analysis can be easily obtained [A2, B2, C3, C17, D1, F4, H1, J1, L3, P4, S24, T3]. Large signal stability of PWM and quasi-resonant converters through nonlinear modeling and control has also been discussed in [C4, C17, E3, F2, G3, H6, L17, S18, S19]. From all of these large signal approaches, continuous-time small-signal models can be obtained through linearization around a periodic trajectory (orbit). When the starting model is discrete subsequent transformation of the results into continuous time is needed [F1, F3, L2, S17, T7, V3, W5].

Small-signal models have also been obtained from very dissimilar perspectives such as model fitting with neural networks of data from converter simulations [H5, L7], analytical approximations [E2, V11, W4], and perturbation of exponential transition matrices either on computer [M4, W5] or on state plane graphs [O4].

The well-known state-space averaging method [B11] can also be developed as the low-order approximation in several different methods by retaining only the first terms in:

(a) power series for the matrix exponentials in the sample-data modeling [V3],
(b) multi-frequency averaging [C1],
(c) the generalized method of averaging [K6, L4, L6, N3, S2, S13, V3, W3].

It provides information about the average of the state variables, but loses accuracy in the high frequency range, *i.e.* near a half of the switching frequency, and/or when the filter time constants are close to the switching period, as it usually happens in some of the sampled-data models above. Similar characteristics with slight result
improvements are exhibited by the current injection-absorption method [K5], by the averaged PWM-switch model [V8] and its several extensions for multi-switch PWM converters and resonant converters, and by several other circuit-oriented average models [A3, C5, C6, C7, C24, E4, J5, L9, L11, K4, M2, M6, N2, R1, O1, O2, R1, S4, S6, S7, S8, S20, T4, T8, V1, V8, V9, V10, W3, W7, X2, X4, Y2].

Validity of the method of averaging to simple PWM converter topologies was rigorously proved [B3, K6, L4, S2] and extended to provide frequency-dependent continuous-time average models for open and closed-loop operation [B5, L5, L6]. Unfortunately, application of this technique or the familiar state-plane portrait methods [G2, O3, S10], useful to analyze operation of low order resonant converters, to more complex soft-switched power converters becomes almost intractable. Analytic approximations and modifications to the method of averaging have also been proposed for PWM and some types of resonant converters [N3, S13, S14, S22, W3, X3].

Extended describing functions and multi-frequency methods [C1, C18, S3, Y1] overcome this tractability problem and had been proven useful in small-signal analysis of resonant and multi-resonant converters of any order, despite their lack of physical insight and the need for special software.

Some special simulator programs and/or algorithms have been developed to provide shorter simulation times [B6, B7, L8, M1, N1, P2, S5, T2, D2, B9, B10] at the expense of limited functionality and data preparation.

Following the attempt made in [R4], a corrected and general continuous-time, state-space, small-signal model of current programmed PWM converters was developed in [T5, T7] and verified with the so called exact small-signal models obtained by application of time varying transfer functions [T6, T9]. However none of these papers discusses relevance of time varying effects at frequencies near a half of the switching frequency which are detailed in [P3] and analyzed for three-phase PWM modulators in
The same happens in [K5, S16, S21, S24, T1, V8, V10] where attempts to fit and/or explain small-signal measurements in the high frequency range were made without dealing with the stochastic characteristics of those measurements. Furthermore, extensive similar work on small-signal modeling of the modulator and/or the whole converter for peak and average current control has been reported in [B8, C19, K1, K8, L10, P5, R5, S23, S24, T1, X1].

Geometrical linearization through graphical analysis of perturbed steady-state waveforms was used in [V5] to provide an approximate small-signal model of the widely used Zero-Voltage Switched, Full-Bridge (ZVS-FB) PWM converter [S1] based on the PWM switch model. An approximate large signal model whose usage is restricted to a narrow range in CCM and a small-signal model derivation along the lines of [S1] for the ZVS-FB converter was presented in [T4]. Similarly small-signal models for some ZVS and Zero-Voltage Zero-Current Switched Full-Bridge ZVZCS-FB converters are developed in [C15, X5].

Lately, with the progress in symbolic math packages, methods to obtain closed form expressions for large and small-signal models of PWM converters have been developed [B4, S12]. These methods separate fast and slow dynamic subsystems in the converter and describe their interaction through an algebraic equation. However, they do not allow for non-linear or energy holding components in the fast dynamic subsystem or high order systems for which closed form solutions cannot be computed. Therefore they cannot be applied to many new soft-switched topologies [B1, C9, C10, C11, C12, C16, J2, J3, J4, K2, K3, L1, L12, L14, M3, V6, V7, W1, W2, W6, X5].

From a different perspective, power transfer based models [S7, S8, E5] provide good low frequency description of input-output characteristics for certain PWM converters when loss-less switching devices are considered. When losses are included, the principle of energy conservation needs to be invoked [C24]. These approaches, when combined with other models such as current injection-absorption, state-space averaging,
PWM and resonant switch, are useful in model verification as well as in calculation of input and output impedances for subsystem interaction analysis [C13, G2, R3].

A few attempts to develop a SPICE oriented dual model to deal both with CCM & DCM were plagued with convergence problems [C7, G4, S21]. In [R5] the same authors of [C7] presented a revised version that solved those problems for the buck converter. A decade later the subject was retaken in [N4] where dual models for most of the simple PWM converters are presented.

As a matter of completeness the following special modeling approaches are also mentioned: geometric [S9], phasor transformation [R2], switching flow graph [S11], virtual winding for transformer magnetizing current [L16].

For the modeling presented here on the three-phase buck rectifier and a ZVZCS three-phase to dc converter the wonderful theses [H2, N2] and the references therein provide all the needed background.

1.3. Dissertation Outline and Major Results.

1. **Mathematical description of large signal average models for switching power converters.** The next chapter reviews analytical procedures for variations of the generalized method of averaging [K6, S13] proposed for switching power converters (SPCs). The theoretical foundation behind a method to synthesize averaged circuits models for SPCs [S4] is also presented. Scope and limitations of these methods are discussed. A new systematic procedure to derive circuit oriented average models, which describe input-output characteristics for PWM converters, and that overcomes several of those limitations is developed. This procedure combines the theoretical foundation of [S4] with variations of some ideas from in-place circuit averaging techniques in [V8, V9], extensions to constraints derivation to keep them valid during transient conditions [V3],
practices from analog and circuit simulation in order to model CCM-DCM bifurcation [R5] and heuristic guidelines for selecting averaged circuit structure and relevant states as well as for modeling energy storage components. Basic features of the new modeling procedure are introduced by applying it to a simple buck PWM converter. CCM and DCM operation is covered by the same average model.

2. **Modeling of the ZVS-FB PWM converter.** In Chapter 3 a new and very accurate average model for both DCM and CCM mode of operation is developed and its superiority compared to existing models is clearly seen for different parameter and load values. Small-signal models obtained through linearization of the new average model at different operating points show strong positive damping effects, *i.e.* intrinsic negative feedback, over the output filter. These results agree very well with those from experiments.

3. **Modeling of a saturable reactor-based ZVZCS-FB PWM converter.** Extension of the circuit averaging procedure to include new effects created by a saturable reactor and a so-called energy holding component, in power converter modeling literature, provided the only reported model for this ZVZCS converter. The model, detailed in Chapter 4, explains and recreates the interaction of power stage components, which leads to negative damping effects, *i.e.* intrinsic positive feedback, over the output filter. These effects were also reported for the first time with the model. Large signal simulation results from the average circuit model closely match those from a switching model for different parameter and load values. Small-signal models from linearization of the average circuit model, which correctly predicted the negative damping effects seen in transfer function measurements conducted on 3.5 kW prototypes, were a useful starting point for current-loop design in a multi-module prototype.

4. **Average modeling and modulation scheme development for a Quasi-Single Stage ZVZCS Three-Phase Buck Rectifier.** Chapter 5 illustrates versatility of
the modeling procedure when dealing with interconnection issues in this special multi-converter structure. It is formed by cascading a three-phase buck rectifier and the ZVZCS converter in the previous chapter. Physical insight provided by the average circuit model developed for this three-phase rectifier, which is also a new result, helped to discover the main causes of strong nonlinear relationships between commanded duty-cycles and effective duty cycles, *i.e.* voltage transfer ratio, near the boundaries of the sixty-degree electrical sectors in standard space vector modulation (SVM). These nonlinearities induced high distortion and ripple in ac input currents and dc output voltage, which rendered the system unsuitable for the intended telecommunications application. Physical insight from the model also helped to develop a new simple and effective modified SVM with feed-forward duty-cycle compensation scheme that reliably minimizes current distortion and voltage ripple while keeping the same single dimension control.
2. MATHEMATICAL DESCRIPTION OF SWITCHING POWER CONVERTERS AND THEIR LARGE AND SMALL-SIGNAL MODELING

This chapter starts with a review of state-space descriptions for PWM converters in continuous and discrete time forms followed by an outline of small-signal model derivation in both time forms. Afterwards variations of the method of generalized averaging are introduced. In addition the approaches to synthesize averaged circuit model for PWM converters are also discussed and a comparison analysis of these methods is presented. Then a new modeling procedure to obtain autonomous averaged circuits of PWM converters is outlined and illustrated through its application to the buck converter. The resulting averaged circuit covers a wide range of operation, i.e. DCM-CCM.

2.1 Characteristics and State-Space Description of PWM Converters

The PWM converters considered in this work consist of linear resistive and reactive elements, piece-wise linear switching elements with the externally controlled ones activated at a constant frequency, and input and output power terminals that can exhibit ac or dc variables as depicted in Fig. 2.1.

2.1.1. Continuous-time state-space equations

The conditions imposed upon the elements of the power stage allow the converters to be described, in between certain switching instants $t_{k,i}$, by linear time-invariant ordinary differential equations of the form [V4]

$$\frac{d}{dt} x(t) = A_{k,i} \cdot x(t) + B_{k,i} \cdot u(t) \quad t_{k,j-1} < t \leq t_{k,i},$$

where state vector $x(t)$ is $n \times 1$, state transition matrix $A_{k,i}$ is $n \times n$, input matrix $B_{k,i}$ is $n \times r$ and input vector $u(t)$ is $r \times 1$.

Switching instants $t_{k,i}$ are determined by combinations of control parameters and/or state variables from the power stage and control circuitry. Subscript $k$ corresponds to switching cycle, whose duration is assumed constant and designated by $T_s$, and subscript $i$ corresponds to a time interval within each cycle during which the system maintains the same switch configuration, Fig. 2.3. Entries for matrices $A_{k,i}$ and $B_{k,i}$ depend upon switch conditions (on or off), which determine circuit structure in between switching instants, and component values. The combinations that determine the switching instants in the $k$-th cycle can be described by the set on $m$ constraints

$$c(x(t_k), p(t_k), u(t_k)) = 0,$$

where $p(t_k)$ is a $q \times 1$ vector of independent controlling parameters.
Fig. 2.1. PWM converter structure.
2.1.2. Sample-data state-space equations

In general the change on the converter state-space vector $x(t)$ over one switching cycle, i.e. from $t_k$ to $t_{k+1}$, can be expressed by the $n$ sampled-data relations

$$x(t_{k+1}) = f(x(t_k), p(t_k), u(t_k)),$$  \hspace{1cm} (2.3)

upon integration of (2.1). $f(\cdot, \cdot, \cdot)$ represents a vector valued nonlinear function that in our case can be simplified to $[V3, V4]$

$$x(t_{k+1}) = F(p(t_k)) \cdot x(t_k) + H(p(t_k), u(t_k)),$$  \hspace{1cm} (2.4)

where $F(\cdot)$ and $H(\cdot)$ are $n \times n$ and $n \times 1$ matrices respectively that involve matrix exponentials of $A_{k,i}$ and are easily computable in terms of $A_{k,i}, B_{k,i}$ and $u(t)$.

When a dc-dc PWM converter is operating in steady state the state space vector returns at the end of the switching cycle to the same value it had at the beginning of it, i.e.

$$x(t_{k+1}) = x(t_k) = F(p(t_k)) \cdot x(t_k) + H(p(t_k), u(t_k)) = X$$  \hspace{1cm} (2.5)

is a constant as well as $p(t_k)=P$ and $u(t_k)=U$. As a result (2.2) and (2.5) become

$$c(X, P, U) = 0$$  \hspace{1cm} (2.6)

and

$$X = F(P) \cdot X + H(P, U).$$  \hspace{1cm} (2.7)

Small-signal dynamics of perturbations around an orbit can now be obtained by keeping up to linear terms of the Taylor series expansion of equations (2.6) and (2.7), i.e.

$$\Delta x(t_{k+1}) = F(P + \Delta p(t_k)) \cdot (X + \Delta x(t_k)) + H(P + \Delta p(t_k), U + \Delta u(t_k)) - X$$  \hspace{1cm} (2.8)

and

$$c(X + \Delta x(t_k), P + \Delta p(t_k), U + \Delta u(t_k)) = 0,$$  \hspace{1cm} (2.9)

where $\Delta x$ and $\Delta p$ represent those perturbations.

After carrying out some cancellations on the series expansions one obtains:
\[
\Delta x(t_{k+1}) = F(P) \cdot \Delta x(t_k) + \frac{\partial}{\partial p} F(P) \cdot \Delta p(t_k) \cdot X \\
+ \frac{\partial}{\partial p} H(P, U) \cdot \Delta p(t_k) + \frac{\partial}{\partial u} H(P, U) \cdot \Delta u(t_k) 
\] 
(2.10)

and

\[
\frac{\partial}{\partial x} c(X, P, U) \cdot \Delta x(t_k) + \frac{\partial}{\partial p} c(X, P, U) \cdot \Delta p(t_k) \\
+ \frac{\partial}{\partial u} c(X, P, U) \cdot \Delta u(t_k) = 0. 
\] 
(2.11)

which are basically a discrete small-signal model in implicit form and almost always needs to be solved numerically to compute the desired discrete transfer functions. Their continuous-time counterparts can then be computed numerically.

2.1.3 Sampled-data modeling of a simple PWM converter

Since this modeling process gets very involved for high-order systems, some simplifications based on practical converter characteristics are usually possible. To illustrate this process, the large-signal sampled-data model for the simple buck PWM converter, shown in Fig. 2.2, with the so-called peak current control and in CCM of operation is developed. In this system, in CCM operation, there are two state variables, inductor current and capacitor voltage, i.e.

\[
x(t) = \begin{bmatrix} i_L \\ v_C \end{bmatrix}^T, 
\] 
(2.12)

and the two switching configurations (circuit topologies), depicted in Fig. 2.3, i.e. interval subscript \( i \) in (2.1) takes the values 1 and 2. These switching configurations are determined by the conduction state of the switch, i.e. \( on \) or \( off \), and give origin to matrices \( A_{k,i} \) and \( B_{k,i} \),

\[
A_{k,1} = A_{k,2} = A = \begin{bmatrix} 0 & -1/L \\ 1/C & 1/R \cdot C \end{bmatrix}^T, 
\] 
(2.13)

\[
B_{k,1} = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}, 
\] 
(2.14)

and
\[
B_{k,z} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.
\] (2.15)

The remaining term in (2.1), input vector at time \( t_k \), is given by

\[ u(t_k) = v_i(t_k). \] (2.16)

Duration of the first interval in transient regime is determined from conditions represented in Fig. 2.4 where inductor current waveform, modulating ramp and current reference are shown. From Fig. 2.4 the switching constraint that determines \( d_k \) (the duty ratio for interval \( i=1 \)) is calculated as

\[ i^*(t_k) - m_r \cdot d_k \cdot T_s = i_L(t_k) + m_i \cdot d_k \cdot T_s, \] (2.17)

where \( i^*(t_k) \) represents inductor current reference (independent control parameter \( p(t_k) \) in (2.2)), \( i_L(t_k) \) is the inductor current values at time \( t_k \), \( m_r \) and \( m_i \) correspond to modulating ramp slope and approximated inductor current slope during interval 1 respectively when capacitor voltage is assumed constant over one switching cycle, i.e. \( T_s \).

The large signal sampled-data model for the buck converter, after assumption of constant control during each interval can be described as

\[ x(t_k + d_k \cdot T_s) = F_1(d_k) \cdot x(t_k) + H_1(d_k) \cdot u(t_k) \] (2.18)

and

\[ x(t_k + T_s) = F_2(d_k) \cdot x(t_k + d_k \cdot T_s) + H_2(d_k) \cdot u(t_k + d_k \cdot T_s), \] (2.19)

where

\[ F_1(d_k) = e^{A_1d_kT_s}, \quad H_1(d_k) = \int_0^{d_kT_s} e^{A_1\sigma} \cdot B_1 \cdot d\sigma \] (2.20)

and

\[ F_2(d_k) = e^{A_2(1-d_k)T_s}, \quad H_2(d_k) = \int_0^{(1-d_k)T_s} e^{A_2\sigma} \cdot B_2 \cdot d\sigma. \] (2.21)
Fig. 2.2 Simple buck PWM converter with current feedback.
Fig. 2.3. Buck converter circuit topologies

ON-state

Interval \( i=1 \)

\[ t_k < t < t_k + d_k T_S \]

OFF-state

Interval \( i=2 \)

\[ t_k + d_k T_S < t < t_{k+1} \]
Fig. 2.4 Relevant waveforms for duty-cycle calculation
Concatenation of (2.28) and (2.19) provides a cycle-to-cycle representation of the system that can describe the behavior either at the beginning of the cycles, (2.22), or at the switching instants, (2.23).

\[
x(t_{k+1}) = F_2(d_k) \cdot F_i(d_k) \cdot x(t_k) + (F_2(d_k) \cdot H_i(d_k) + H_2(d_k)) \cdot u(t_k).
\]  

(2.22)

\[
x(t_{k,i} + d_k \cdot T_s) = F_i(d_k) \cdot F_i(d_k) \cdot x(t_k + d_k \cdot T_s) + (F_2(d_k) \cdot H_i(d_k) + H_2(d_k)) \cdot u(t_k + d_k \cdot T_s).
\]  

(2.23)

When control signals vary slowly as compared to switching period, the matrix exponentials can be approximated by keeping up to the linear terms in their series expansion. That is,

\[
F_i = e^{A_i \sigma} \approx I + A_i \cdot \sigma,
\]  

(2.24)

and

\[
F_j F_i = e^{A_j \sigma} e^{A_i \lambda} \approx I + A_j \cdot \sigma + A_i \cdot \lambda,
\]  

(2.25)

which are the same approximations made in the continuous-time state-space averaged method.

After using these approximations in (2.22) the large-signal model becomes

\[
x(t_{k+1}) = \Phi(d_k) \cdot x(t_k) + \Psi(d_k) \cdot u(t_k)
\]  

(2.26)

where

\[
\Phi(d_k) = I + A_2 \cdot d_k \cdot T_s + A_2 \cdot (I - d_k \cdot T_s) = I + A \cdot T_s
\]  

(2.27)
and

$$\Psi(d_k) = (I + A \cdot T_S) \cdot B_i \cdot d_k \cdot T_S. \tag{2.28}$$

Linearization of (2.26), leads to an approximate discrete small-signal model of the following form

$$\Delta x(t_{k+1}) = \Phi(d_k) \cdot \Delta x(t_k) + (I + A \cdot T_S) \cdot B_i \cdot T_S \cdot u(t_k) \cdot \Delta d_k + \Psi(d_k) \cdot \Delta u(t_k). \tag{2.27}$$

Similarly linearization of (2.17) provides $\Delta d_k$ as

$$\Delta d_k = -\Delta i_L(t_k)/(m_i + m_r) \cdot T_s + \Delta i_p(t_k)/(m_i + m_r) \cdot T_s, \tag{2.28}$$

which when substituted in (2.27) gives after some manipulations the final form

$$\Delta x(t_{k+1}) = K \cdot \Delta x(t_k) + A \cdot \Delta i_p(t_k) + M \cdot \Delta v_{ios(t_k)}. \tag{2.29}$$

Equations 2.12 through 2.27 show that large and small-signal sampled-data model can be easily and systematically obtained for simple PWM converters in open and closed loop operation. Unfortunately modeling of interconnected converters from their independent models is not a straightforward procedure and most of the time requires a complete new derivation.

2.2. Generalized Method of Averaging for PWM Converters

The main objective for applying the generalized method of averaging, also known as KBM (Krilov, Bogoliubov, Mitropolski), to time varying systems, such as PWM converters, is to obtain an autonomous model that closely describes a moving average of the variables in the original system. In other words, we are trying to derive a simpler model that retains some of the main properties, a slow dynamics manifold, of the initial system.
In this chapter a general description of this method following the lines in [K5] and how to apply it to a simple PWM converter in CCM are presented. A simple way to estimate information about ripple of the variables is also discussed.

### 2.2.1. Procedures of the method

In order to apply the KBM method to a system it is necessary to cast it in the standard form

\[
\frac{d}{dt} x(t) = \varepsilon \cdot F(t, x), \quad x(t_0) = x_0, \tag{2.30}
\]

where \( \varepsilon \) is a small non-dimensional parameter and \( F \) is a vector valued function (see K5 and the references within for a rigorous justification of averaging for (2.30)). The integral

\[
G(\cdot) = \lim_{T \to \infty} \frac{1}{T} \int_0^T F(s, \cdot) ds, \tag{2.32}
\]

is defined as the time average of (2.30) and leads to the new time-invariant averaged model

\[
y(t) = \varepsilon \cdot G(y), \quad y(t_0) = y_0. \tag{2.33}
\]

When the system is periodic or quasi-periodic, as in PWM converters, the integral in (2.32) is finite and hence the limit exists.

The KBM method is based on the change of variables

\[
x(t) = y(t) + \varepsilon \cdot \psi_1(t, y) + \varepsilon^2 \cdot \psi_2(t, y) + \varepsilon^2 \cdot \psi_3(t, y) + \ldots, \tag{2.34}
\]

where \( \psi_i \) are functions of time with zero-average value, which transforms the original system, \( i.e \) (2.30), into the time invariant system
\[
\frac{d}{dt} y(t) = \varepsilon \cdot G_1(y) + \varepsilon^2 \cdot G_2(y) + \varepsilon^3 \cdot G_3(y) + \ldots \tag{2.35}
\]

In order to obtain a set of equations in the new variable \( y \), (2.30), (2.34) and (2.35) need be used. First, (2.34) gets differentiated with respect to time, then (2.30) is used to eliminate \( \dot{x} \), (2.35) to eliminate \( \dot{y} \), and (2.34) to eliminate \( x \). Then terms with the same power of \( \varepsilon \) are equated to get a system of equations that can be sequentially solved for \( \psi_i(t,y) \) and \( G_i(t,y) \).

### 2.2.2. Illustration of the generalized method of averaging for a simple PWM converter

This process is presented here for single switch PWM converters in CCM operation, i.e. two intervals per switching cycle. In the next section the same process will be specifically used with the open loop buck converter.

Equation 2.30 can be written as

\[
\frac{d}{dt} x(t) = \left[ A_2 + h(t,T_s) \cdot (A_i - A_2) \right] \cdot x(t) + \left[ B_2 + h(t,T_s) \cdot (B_1 - B_2) \right] \cdot u(t) \tag{2.36}
\]

where matrices \( A_i \) and \( B_i \) correspond to those defined in (2.1) for intervals 1 and 2 after dropping the index \( k \), and

\[
h(t,T_s) = H \left[ d(t) - \text{ramp}(t,T_s) \right]. \tag{2.37}
\]

where \( H(z) \) is the Heaviside or unit step function, \( d(t) \) is the duty-cycle control signal and the function \( \text{ramp}(t,T_s) \) corresponds to the PWM modulating signal. The latter is described by using the module operation

\[
\text{ramp}(t,T_s) = \frac{t \text{ mod}(T_s)}{T_s}. \tag{2.38}
\]

Calculation of the parameter \( \varepsilon \) is performed by selecting the largest absolute value of the entries in matrices \( A_i \) and \( B_i \), designated by \( \xi \) in (2.39), and multiplying it by \( T_s \), i.e.
\[ \varepsilon = \max_{i,j} \left\{ \left| a_{i,j} \right|, \left| b_{i,j} \right| \right\} \cdot T_s = \xi \cdot T_s. \quad (2.39) \]

If time is scaled as
\[ t = T_s \cdot \tau, \quad (2.40) \]
equations (2.36) and (2.37) can be expressed in terms of \( \varepsilon \) and \( \tau \) as

\[
\begin{align*}
\frac{d}{d\tau} x(\tau) &= \varepsilon \cdot \left\{ \frac{1}{\xi} \cdot A_2 + \frac{h(\tau,1)}{\xi} \cdot (A_1 - A_2) \right\} \cdot x(\tau) \\
&\quad + \left\{ \frac{1}{\xi} \cdot B_2 + \frac{h(\tau,1)}{\xi} \cdot (B_1 - B_2) \right\} \cdot u(\tau) \}
\end{align*}
\]

and

\[ h(\tau,1) = H \left[ d(\tau) - \text{ramp}(\tau,1) \right] \quad (2.42) \]

respectively. Thus application of the averaging operator (2.32) to the right hand side (RHS) of (2.41) produces

\[
G(y) = \left\{ \frac{1}{\xi} \cdot A_2 + \frac{d}{\xi} \cdot (A_1 - A_2) \right\} \cdot y \\
\quad + \frac{1}{\xi} \cdot \left\{ B_2 + \frac{d}{\xi} \cdot (B_1 - B_2) \right\} \cdot U, \quad (2.43)
\]

where \( d \) is the average duty-cycle. The average model, after returning to the original time scale, is given by

\[
\begin{align*}
\frac{d}{dt} y(t) &= \left[ A_2 + d \cdot (A_1 - A_1) \right] \cdot y(t) \\
&\quad + \left[ B_2 + d \cdot (B_1 - B_2) \right] \cdot U,
\end{align*}
\]

which is the same result obtained through state-space averaging. Estimates of variables ripple can now be computed by continuing with the KBM method. Manipulation of (2.34), (2.35) and (2.43) leads to
\[ \varepsilon \left[ \frac{1}{\xi} \cdot A_2 + \frac{h(\tau)}{\xi} \cdot (A_1 - A_2) \right] \cdot \left[ y + \varepsilon \cdot \psi_1 + \varepsilon^2 \cdot \psi_2 + \ldots \right] \\
+ \varepsilon \cdot \left[ \frac{1}{\xi} \cdot B_2 + \frac{h(\tau)}{\xi} \cdot (B_1 - B_2) \right] \\
= \left( \varepsilon \cdot G_1 + \varepsilon^2 \cdot G_2 + \varepsilon^3 \cdot G_3 + \ldots \right) \\
+ \varepsilon \cdot \left[ \frac{\partial \psi_1}{\partial \tau} + \frac{\partial \psi_2}{\partial \tau} \right] \cdot \left( \varepsilon \cdot G_1 + \varepsilon^2 \cdot G_2 + \ldots \right) \\
+ \varepsilon^2 \cdot \left[ \frac{\partial \psi_2}{\partial \tau} + \frac{\partial \psi_3}{\partial \tau} \right] \cdot \left( \varepsilon \cdot G_1 + \varepsilon^2 \cdot G_2 + \ldots \right) \ldots \tag{2.45} \]

from where equating terms with the same power of \( \varepsilon \) gives

\[ \varepsilon : \quad \left[ \frac{1}{\xi} \cdot A_2 + \frac{h(\tau)}{\xi} \cdot (A_1 - A_2) \right] \cdot y + \left[ \frac{1}{\xi} \cdot B_2 + \frac{h(\tau)}{\xi} \cdot (B_1 - B_2) \right] = G_1 + \frac{\partial \psi_1}{\partial \tau}, \tag{2.46} \]

\[ \varepsilon^2 : \quad \left[ \frac{1}{\xi} \cdot A_2 + \frac{h(\tau)}{\xi} \cdot (A_1 - A_2) \right] \cdot \psi_1 = G_2 + \frac{\partial \psi_1}{\partial \tau} \cdot G_1 + \frac{\partial \psi_2}{\partial \tau}, \tag{2.47} \]

\[ \varepsilon^2 : \quad \left[ \frac{1}{\xi} \cdot A_2 + \frac{h(\tau)}{\xi} \cdot (A_1 - A_2) \right] \cdot \psi_2 = G_3 + \frac{\partial \psi_1}{\partial \tau} \cdot G_2 + \frac{\partial \psi_2}{\partial \tau} \cdot G_1 + \frac{\partial \psi_3}{\partial \tau}. \tag{2.48} \]

Equation (2.46) is used to solve for \( G_1 \) by taking the average over one period with respect to \( \tau \) and the result is the same as the RHS of (2.44). Now \( G_1 \) is substituted in (2.46) and then the constant of integration is selected to make \( \psi_1 \) zero-average and of period \( T_s \). Similarly the other functions can be calculated to obtain a higher order approximation for variables ripple (see [K5] for modeling of the boost converter and its ripple estimation).
2.2.3. Generalized method of averaging for the open loop buck converter

The converter in Fig.2.3 is considered here but in open loop and its continuous-time state-space equations, i.e. (2.36), after substituting (2.13)-(2.15) reduces to

\[
\frac{d}{dt} x(t) = A_i \cdot x(t) + h(t, T_s) \cdot B_i \cdot v_{in}(t),
\]  
(2.49)

and

\[
h(t, T_s) = H \left[ d - \text{ramp}(t, T_s) \right].
\]  
(2.50)

The average equation is then given by

\[
\frac{d}{dt} y(t) = A_i \cdot y(t) + d \cdot B_i \cdot v_{in}(t)
\]  
(2.51)

and (2.45) reduces to

\[
\frac{1}{\xi} \cdot A_i \cdot y + \frac{h(\tau)}{\xi} \cdot B_i = G_i + \frac{\partial \psi_i}{\partial \tau},
\]  
(2.52)

from where after some manipulations \(\psi_i\) is obtained as

\[
\psi_i(\tau) = \frac{1}{\xi} \cdot B_i \left\{ [h(\tau) - d] \cdot \text{ramp}(t, 1) + [1 - h(\tau)] \cdot d + \frac{1}{2} \cdot (d^2 - d) \right\}
\]  
(2.47)

and the remaining \(G_i\) for \(i = 2, 3, \ldots\) are zero.
2.3. Averaging Method for Two-Time Scale PWM Converters

Most PWM converters can be classified as one or two-time scale systems. A method for the latter, developed very similarly by different authors [N2, S13, W3], is presented here. The former are already covered by the method in section 2.2.

2.3.1. State-space description for two-time scale PWM converters

The two-time scale characteristics of a PWM converter can be explicitly shown by representing the system in the form

\[
\frac{d}{dt} x(t) = \epsilon \cdot f(t, x, y), \quad x(t_0) = x_0, \quad (2.48)
\]

\[
\frac{d}{dt} y(t) = g(t, x, y), \quad y(t_0) = y_0, \quad (2.49)
\]

where \( \epsilon \) is again a small non-dimensional parameter, \( x \) and \( y \) are state vectors of dimension \( n \) and \( m \) respectively, and \( f \) and \( g \) are vector valued functions.

The average model for (2.48) is defined as

\[
\frac{d}{dt} X(t) = \epsilon \cdot f_0(X), \quad X(t_0) = x_0, \quad (2.50)
\]

with

\[
f_0(x) = \lim_{T_s \to \infty} \frac{1}{T_s} \int_t^{t+T_s} f(\tau, x, \varphi(\tau, x, t', y_0)) d\tau, \quad t \geq t_0, \quad (2.51)
\]

where \( \varphi(\tau, x, t', y_0) \) is the solution of (2.49) with initial value \( y(t') = y_0 \) and fixed \( x \).
When \( x \) is fixed switch patterns in PWM converters do not change, and hence, if \( \varphi(\tau, x, t', y_0) \) converges to a periodic function \( \psi(\tau, x) \) in a finite time (2.51) can be simplified to

\[
f_0(x) = \frac{1}{T_s} \int_0^{T_s} f(\tau, x, \psi(\tau, x)) \, d\tau,
\]

whose value is finite as described in section 2.2. Thus \( \psi(\tau, X) \) becomes the steady-state solution of \( y(t) \) for fixed \( X \).

For PWM converters (2.48) and (2.49) can be written as

\[
\frac{dx}{dt} = A_i^{sx} \cdot x + A_i^{sy} \cdot y + B_i^s \cdot u,
\]

\[
\frac{dy}{dt} = A_i^{fx} \cdot x + A_i^{fy} \cdot y + B_i^f \cdot u,
\]

where superscripts \( s \) and \( f \) stand for slow and fast in \( A_i \) and \( B_i \) matrices, which are constant during interval \( i \).

### 2.3.2. Practical procedure for the method

Starting with the PWM converter equations in the form of (2.53) and (2.54) the following steps summarize the averaging procedure.

1. Assume slow variables \( x \) as fixed in the equations for fast variables \( y \), (2.54):

\[
\frac{dy}{dt} = A_i^{fy} \cdot y + \left\{ A_i^{fx} \cdot X + B_i^f \cdot u \right\}.
\]
2. Compute steady-state solution \( y_{ss} \) of fast variables in (2.55);

3. Substitute \( y_{ss} \) into (2.53) to get

\[
\frac{dx}{dt} = A_i^{sx} \cdot x + A_i^{sy} \cdot y_{ss} + B_i^i \cdot u .
\] (2.57)

3. Compute the average of (2.57), over one switching period,

\[
f_0(x) = \frac{1}{T_s} \sum_{i=1}^{r} \int_{t_{k,i-1}}^{t_{k,i}} \left\{ A_i^{sx} \cdot x + A_i^{sy} \cdot y_{ss} + B_i^i \cdot u \right\} dt ,
\] (2.58)

to obtain the average model

\[
\frac{dX}{dt} = f_0(X) .
\] (2.59)

2.4. Synthesis Method for Averaged Circuit Models of PWM Converters

Development of autonomous averaged and small-signal circuit models according to [S4, V8] is presented in this section. Their intent is to reproduce state-space averaging results for single switch PWM converters. In [S4], an in-place circuit averaging is performed and analytical support is given whereas in [V8] an equivalent 3-terminal circuit is sought for the so-called PWM switch.

2.4.1. In-place averaging

When the moving average operation over one switching cycle given by
\[
\bar{y}(t) = \frac{1}{T_s} \int_{t-T_s}^{t} y(\sigma) \, d\sigma
\]  

(2.60)

is applied, in-place to each branch variable of PWM converters, in steady state operation, the transformed branch variables satisfy the same node and mesh constraints as the original variables. Therefore the synthesis of an averaged circuit model can be oriented towards a circuit layout topologically equivalent to the original simple PWM converter. Since a requirement for linear reactive elements not to be altered by the moving average operator is that the latter and differentiation with respect to time commute, \textit{i.e.}

\[
\frac{d}{dt} \left[ \frac{1}{T_s} \int_{t-T_s}^{t} y(\sigma) \, d\sigma \right] = \frac{1}{T_s} \left[ y(t) - y(t-T_s) \right]
\]

(2.61)

\[
= \frac{1}{T_s} \int_{t-T_s}^{t} \frac{d}{d\sigma} y(\sigma) \, d\sigma = \left[ \frac{d}{dt} y(t) \right]
\]

which implies continuous differentiability for the state variables, \textit{i.e.} their first time derivative to be continuous. Unfortunately this is not the case for the PWM converters treated here as stated by (2.1) and hence the moving average of the state variables do no satisfy the converter’s state equations in general.

Application of the one cycle moving average operator in (2.60) to the state-space representation of the PWM converter in (2.1), and reproduced here for clarity,

\[
\frac{d}{dt} x(t) = A_{k,j} \cdot x(t) + B_{k,j} \cdot u(t) \quad \quad \quad \quad \quad t_{k,j-1} < t \leq t_{k,j},
\]

(2.62)

leads to the form

\[
\frac{d}{dt} x(t) = \frac{1}{T_s} \int_{t-T_s}^{t} \left[ A_{k,j} \cdot x(s) + B_{k,j} \cdot u(s) \right] \left[ H(s-t_{k,j-1}) - H(s-t_{k,j}) \right] ds,
\]

(2.63)
which is valid for all \( k,i \) since \( H(\cdot) \), the Heaviside step function, in the last bracket selects the appropriate time intervals for matrices \( A_{k,i} \) and \( B_{k,i} \).

Direct computation of this moving average would require keeping track of intervals within each switching cycle, which is a terrible burden. Instead an approximated average per switching cycle described by

\[
\frac{d}{dt} X(t) = \frac{1}{T_s} \int_{t_k-T_s}^{t_k} \left[ A_{k,i} \cdot x(s) + B_{k,i} \cdot u(s) \right] \left[ H(s - t_{k,i-1}) - H(s - t_{k,i}) \right] ds
\]  

(2.64)

is used, where \( X \) is the new averaged state and \( t_k = t \). In other words the moving average interval of width \( T_s \) and the switching cycle are assumed to coincide.

[S4] provides a theorem regarding the synthesis of an averaged circuit for a PWM converter with a single controlled and linear time invariant components. The converter must fulfill the following conditions:

(a) be partitioned as shown in Fig. 2.5,

(b) have unique solutions for voltage and currents of its branches, e.g. no capacitor-voltage source loop, etc.,

(c) have a hybrid representation for the RESISTORS multiport in Fig. 2.5 with controlling port variables taken as currents for those ports connected to current source or inductive ports and as voltage for those ports connected to voltage source or capacitive ports, with a single current-controlled switch port and a single voltage controlled switch port.

Given all this it is possible to obtain an averaged circuit model by replacing the two-port switch network with a resistive two-port whose hybrid representation is

\[
H_s(d) = \frac{d}{1 - d} \cdot H_{22}
\]  

(2.65)

for \( d \neq 1 \), where \( H_{22} \) is the hybrid immittance seen by the switch two-port when all current source and inductive branches are replaced by open circuits and all voltage source and capacitor branches are replaced by short circuits.
Since application of this theorem is restricted to single switch converters, a procedure introduced in [V8] for the PWM-switch and then complemented in [L11, X4, Y2], which also leads, in a more direct way, to the synthesis of a valid circuit for the same hybrid representation is shown instead.

2.4.2. PWM-switch equivalent circuits

This method was proposed in [V8] for dc and small-signal model. It starts by noting that simple PWM converters include one active switch (externally controlled device) and one passive switch (diode). The combination of these two switches, shown in Fig. 2.6(a), is the so-called PWM switch. Because at most one switch is conducting at a time, some relationships for the instantaneous terminal variables of the PWM switch, depicted in Figs. 2.6(b) remain invariant in simple PWM converters, i.e.

\[
i_a(t) = \begin{cases} 
  i_c(t) & ; \quad 0 \leq t \leq d \cdot T_s \\
  0 & ; \quad d \cdot T_s \leq t \leq T_s
\end{cases}
\]

(2.66)

and

\[
v_{cp}(t) = \begin{cases} 
  v_{ap}(t) & ; \quad 0 \leq t \leq d \cdot T_s \\
  0 & ; \quad d \cdot T_s \leq t \leq T_s
\end{cases}
\]

(2.67)

where \(i\) and \(v\) represent instantaneous port variables, subscripts \(a, p, c\) stand for active, passive and common respectively, and \(dT_s\) represents the interval within the switching cycle when the active switch is on. From here an average model for the PWM switch, valid in steady-state operation, i.e. fixed duty-ratio, is developed by computing, from the waveforms in Fig. 2.6(b), average current and average voltage at its terminals. That is,

\[
I_a = d \cdot I_c
\]

(2.68)

and

\[
V_{cp} = d \cdot (V_{ap} - I_c \cdot r_{eq} \cdot (1 - d)),
\]

(2.69)

where \(I, V\) and \(d\) represent average quantities and \(r_{eq}\) is the equivalent resistor that causes the jump in \(v_{ap}\). That equivalent resistor is usually a combination of capacitor equivalent series resistor (esr) and/or load resistor. For instance in the boost and buck-boost converters \(r_c\) is the parallel combination of output filter capacitor’s esr and load resistor.
An equivalent circuits for the average model of the PWM switch, \textit{i.e.} (2.68) and (2.69), is shown in Fig. 2.7. [V8] uses an ideal transformer instead of the controlled sources. Note that the circuit representation for the PWM switch is not unique but must have the same terminal variables relations. The small-signal model of the PWM switch can be obtained by linearizing equations (2.68) and (2.69). The final result [V8] is

\begin{equation}
\Delta i_d = d \cdot \Delta i_c + I_c \cdot \Delta d, \tag{2.69}
\end{equation}

\begin{equation}
\Delta v_{ap} = \frac{\Delta v_{ap}}{d} + \Delta i_c \cdot r_{eq} \cdot (1 - d) - [V_{ap} + I_c \cdot (2 \cdot d - 1) \cdot r_{eq}] \cdot \frac{\Delta d}{d}. \tag{2.70}
\end{equation}

Computation of typical transfer functions such as control or input voltage to either state variables or output voltage can be carried out by placing the small-signal PWM model into the converter and then using node and mesh equations.

DCM of operation is covered in [V8] for the same type of analysis. Similar works in [X4, Y2] cover DCM and CCM operation respectively. Instead of transformer and equivalent resistor to replace the switch-diode pair the models exhibit a controlled current source and a controlled voltage source. The latter represents average switch current whereas the former represents average diode voltage. In [L11] a simplified version of [Y2], no capacitor \textit{esr} included, is used to model simple PWM converters with a current feedback loop.

2.5. Analysis of Strengths and Weaknesses of these Methods

Of all these methods for switching power converters generalized averaging (KBM) is the most systematic, can include any type of feedback loops but provides very little physical insight and becomes almost untraceable for high order systems. Even though state variables’ ripple can be approximated to an arbitrary degree it requires keeping track of phase relationships between PWM modulating signal perturbations in control and input signals. In other words time varying effects must be considered, which conflicts with the main purpose of averaging, \textit{i.e.} obtaining an autonomous representation.

Physical insight is incorporated into two-time scale averaging for switching power converters with the classification of fast/slow state variables based on waveforms analysis. Moreover the procedure for this method of averaging is systematic and can handle PWM as well as several resonant converter types. Unfortunately energy holding
Fig. 2.5. Partition of PWM converter structure.
Fig. 2.6. The PWM switch

(a) Structure and terminal variables
(b) Terminal waveforms
Fig. 2.7. PWM-switch equivalent average circuit.
elements, dealt with in more detail in *Chapter 4*, are not allowed within the fast state variables and steady-state conditions are used in some portions of the procedure. These steady-state conditions lead to unaccounted dynamic characteristics, *e.g.* input, control and ripple induced effects, which constrain model ranges, *e.g.* order, bandwidth.

PWM switch models and their extensions to some types of resonant converters give very good physical insight and allow for straightforward dc and ac calculations through circuit analysis tools. However, constraints imposed on the switch-diode pair configuration limit the set of converters that can be modeled.

In-place circuit averaging preserves converter structure and hence provides strong physical insight. In addition a systematic and rigorous procedure leads to analytical hybrid representation for the switch-diode pair. Regrettably, this procedure can become very involved for high order systems and deals with CCM and DCM separately as it is also the case for all previous methods. Even though PWM switch modeling and its extensions deal with multiple switches in a systematic way there is no provision for full-bridge based converters or energy storage elements.

### 2.6. A New Procedure for Averaged Circuit Models

Strong features from some of the methods discussed above are complemented with analog simulation and series expansion practices as well as heuristic guidelines to form a new modeling procedure. A simplified version of the so-called duo-mode average model [R5] that covers DCM and CCM for the buck converter with current feedback loop is developed to illustrate the new procedure and then simulation results from switching and average models are presented.

#### 2.6.1. Philosophy of the new average modeling procedure

Representation of port characteristics, *e.g.* impedances, average variables, as well as transfer characteristics, *e.g.* voltage conversion ratio, will be the major property sought for the average circuit model.

The starting point for the procedure is the set of open-loop typical waveforms in transient regime and of switching structures through which the converter passes, Fig. 2.8. Inclusion of transient regime conditions overcomes limitations induced by steady-state conditions used in PWM-switch modeling and in two-time scale averaging methods. Then classification of state variables into fast and slow types from the two-time scale method is used together with circuit topologies and typical waveforms to select, at input and output ports, filtering networks (slow state variable components) whose structures do not get altered by switch transitions, *i.e.* linear time invariant (LTI) networks, so that their contributions to open-loop input/output characteristics (impedances, dynamics) are preserved.
To keep consistency with this goal the equivalent driving and/or loading controlled sources for those LTI filtering networks must be identified and their moving average should be efficiently and accurately approximated (for this task one-cycle average has been heuristically selected). In other words we are trying to mimic the moving average properties stated in (2.61), from in-place averaging section, by applying the one-cycle average of those controlled sources to the LTI networks in the previous paragraph.

At this stage feedback loop effects, e.g. algebraic and dynamic constraints, can be incorporated for stability and transient analysis, and finally a simulator specific implementation should be developed.

In order to help with application of the procedure it gets described in a step-by-step fashion together with guidelines in the next section.

2.6.2. Steps of the new average modeling procedure and their guidelines

Step 1: Classify state variables according to slow/fast dynamics with respect to switching frequency and select meaningful slow states for average circuit model. These states should have neither zero steady-state average nor a zero value during a significant amount of time within the switching cycle and their moving average main frequency components should be much lower than the switching frequency, Fig. 2.9.

Step 2: Select linear time invariant (LTI) input and output parts, i.e. sub-networks made of sources and passive components whose structures do not get altered by switch and diode transitions, Fig. 2.10.

Step 3: Identify “dependent” variable(s) drawn from input network(s) and “independent” variable(s) delivered to output network(s), all from the Step 2, to be represented as controlled sources. These variables should not create discontinuities in state variables regardless of initial conditions, i.e. no current sources in series with inductors or voltage sources in parallel with capacitors, Fig. 2.11.

Step 4: Derive expression for one-cycle average of controlled sources in Step 4 from typical waveforms and circuit topologies. In most cases a few low order terms of power series approximation for waveform description will suffice, Fig. 2.12.

Step 5: Derive algebraic constraints in transient regime, e.g. variable-state dependent switching instants, DCM-CCM boundary conditions; as a function of input, control and fast dynamics variables. The latter should not be related to an energy holding component, described in detail in Chapter 4, since its state variable contributes with a dynamic constraint, i.e. an additional state, which usually requires a particular treatment. Here also low order terms in power series approximation of waveforms may suffice, Fig. 2.13.

Step 6: Incorporate feedback-loop induced algebraic constraints and additional estates (e.g. control and state dependent switching instants, compensator own states). By starting
with an open loop system and later including feedback loops effects it is very likely that only this step will need modifications when changing control strategies, Fig. 2.14.

**Step 7:** Use common and reliable analog simulation practices to implement the average model in circuit simulators and to blend models for different operating modes (e.g. closing a loop around an operational amplifier to find zeros or the inverse of a function, manipulating equations to avoid undefined operations such a division by zero, detecting inadmissible variable values such as bipolar output from a rectifier, on the fly state variables removal/addition etc.), Fig. 2.15.

### 2.6.3. Application of the new procedure to the buck converter

Figures 2.2, 2.3 and 2.4 show the buck converter with current feedback loop, its circuit topologies and its typical waveforms respectively in CCM. Fig. 2.16(a) exhibits an averaged circuit model for the same converter, which can be derived by applying the new procedure as detailed next.

Classification of state variables in **Step 1**, according to their dynamics speed, labels inductor current \(i_L\) and capacitor voltage \(v_C\), shown in Figs. 2.4 and 2.9, as slow type. In **Step 2** the voltage source gets easily identified as linear time invariant input structure whereas the second order filter becomes the output side counterpart, Fig. 2.10.

**Step 3** identifies switch current and diode voltage as “dependent” variable drawn from LTI input part and “independent” variable delivered to LTI output part in the previous step, Figs. 2.8 and 2.11.

In **Step 4** the one-cycle average both for switch current \(I_s\) and diode voltage \(v_D\), in Figs. 2.8 and 2.12 are calculated as

\[
I_s = d \cdot I_L \tag{2.71}
\]

and

\[
v_D = d \cdot v_i \tag{2.72}
\]

where \(d\), \(I_L\) and \(v_i\) are duty-ratio command, average filter inductor current and input voltage respectively.

From Fig. 2.8 peak and average inductor current, \(i_{pk}\) and \(I_L\) are related up to a first order approximation by

\[
i_{pk} = I_L + \frac{1}{2}\left[\Delta i_{up} \cdot d + \Delta i_{down} \cdot (1-d)\right], \tag{2.73}
\]
where

\[ \Delta i_{up} = m_1 \cdot d \cdot T_s = \frac{(v_i - v_C)}{L} \cdot d \cdot T_s, \quad (2.74) \]

and

\[ \Delta i_{down} = m_2 \cdot (1 - d) \cdot T_s = \frac{v_C}{L} \cdot (1 - d) \cdot T_s. \quad (2.75) \]

For later use \( d_2 \) is defined as

\[ d_2 = \frac{i_{pk}}{m_2 \cdot T_s}, \quad (2.76) \]

Algebraic constraint derived in \textit{Step 5} corresponds to CCM-DCM boundary condition, Fig. 2.1.3. Typical operating waveforms and circuit topologies for the buck converter in DCM operation are shown in Fig. 2.17. Development details for the average model in DCM shown in Fig. 2.18 will be presented after completing derivation in CCM.

\textit{Step 6} derives the algebraic constraint induced by current feedback loop incorporation, Fig. 2.14, which determines switching time in terms of current reference and state variables, \textit{i.e.}

\[ i^* - m \cdot d \cdot T_s = i_{pk}, \quad (2.76) \]

Circuit simulator oriented implementation of average model in \textit{Step 7}, includes feedback loop around an operational amplifier to find the root (zero) of a function, Fig. 2.15(a), as well as selection of a root within an admissible interval (duty-cycle between zero and one) and equation manipulation to avoid zero divisor condition, Fig. 2.15(b).

Before applying the new modeling procedure to DCM operation a few observations about the average circuit models for CCM in Fig. 2.16 are included. Even though \textit{Model I} is the only one derived so far, it can be transformed into the others through well-known controlled-source manipulation rules form circuit theory. As a result all three models exhibit the same input, output and transfer characteristics, and obviously any one can be transformed into the other two. Note that in Figs. 2.16(b) and (c) the controlled sources represent in place average voltage or current for the switch or the diode and are labeled as such.

The papers mentioned in the PWM switch model section replace switch and diode by average controlled sources and they arrive to average circuit models \textit{II} and \textit{III} in Fig. 2.16. From all of this it is clear that an input-output description of a switching power converter may have multiple average circuit representations and that sometimes several
or even all of them can be generated by a single procedure. However our goal is to have a modeling procedure that can handle as many types of PWM converters as possible, and some resonant converters as a byproduct, without trying to derive multiple average model structures for the same converter.

Figure 2.17 shows circuit topologies and typical waveforms for the buck converter in DCM operation. The corresponding average model, presented in Fig. 2.18, can be derived by following the new procedure.

Classification of variables according to their dynamics speed, Step 1, labels capacitor voltage as the only slow variable since filter inductor current stays at zero during a significant portion of the switching cycle. Therefore its one-cycle average solely depends on present switching cycle conditions, i.e. its own dynamic history does not directly matter.

In Step 2 only output capacitor is selected as the LTI part in that side whereas the voltage source gets selected for the input counterpart since the filter inductor is ruled out because of the diode, which by being connected in series with it during the second interval, prevents the current from becoming negative, i.e. makes the inductor look nonlinear.

From Step 3 switch current and filter inductor current get respectively identified as "dependent" variable drawn from the input LTI part and "independent" variable delivered to the LTI output part.

Calculation of one–cycle average for the variables in Step 3 is carried out in Step 4 with help from Fig. 2.17(b) where average switch current is clearly given by

$$\bar{i}_s = \frac{i_{pk}}{2} \cdot d,$$  \hspace{1cm} (2.77)

with

$$i_{pk} = m_1 \cdot d \cdot T_s = m_2 \cdot d_2 \cdot T_s,$$  \hspace{1cm} (2.78)

where $d_2$ remains consistent with its definition in 2.76. Similarly one-cycle average filter inductor current is expressed as

$$\bar{i}_L = \frac{i_{pk}}{2} (d + d_2),$$  \hspace{1cm} (2.79)

which can be combined with 2.74, 2.75 and 2.78 to obtain
\[
\overline{i}_L = \left(\frac{v_r - v_c}{2 \cdot L}\right) \cdot d^2 \cdot T_s \cdot \left(\frac{v_r}{v_c}\right).
\] (2.80)

The latter is consistent with the claim that one-cycle average filter inductor current is completely determined by present cycle conditions and hence classifies as a fast variable.

The CCM-DCM boundary condition, illustrated in Fig. 2.13, leads to the expression

\[
\overline{i}_L = \frac{i_{pk}}{2}
\] (2.81)

for which to check during the simulation when both average models, i.e. CCM and DCM version, get combined below by following the approach called duo-mode model presented in [R5] and shown in Fig. 2.19(a), which uses an ideal transformer representation, to cover CCM and DCM operation. Fig. 2.19(b) shows the controlled source equivalent version of the model. The transformer on the left with turns ratio \(1:d\) represents CCM operation whereas the other transformer, with turns ratio \((d + d_2):1\), makes adjustments for DCM operation. Notice that if the constraint

\[
d_2 \leq 1 - d
\] (2.82)

is enforced after calculating \(d_2\), according to (2.76), the turns ratio for the right transformer reduces to \(1:1\) during CCM, which makes it irrelevant as far as input-output transfer characteristics concerns and the correct model is seen. However during DCM operation \(d_2\) must be adjusted to enforce (2.80), i.e. average inductor current. The analog implementation diagram shown in Fig. 2.21 satisfies both CCM and DCM constraints.

Application of simple controlled-source manipulation practices from network theory transforms the average circuits in Fig. 2.19 into those in Fig. 2.20 while keeping the same input-output characteristics and all the relevant information available. The model in Fig. 2.20(b) can be covered by the new procedure if the circuit simulation oriented implementation in Step 7 is expanded to search for versatile analog circuit representations that can change the number of state variables (filter inductor current state removed during DCM) in real time during the simulation in a smooth and reliable fashion, i.e. no convergence prone or discontinuity inducing structures.

Current feedback loop incorporation in Step 6 deals with (2.76) again but \(i_{pk}\) is now given by (2.78) instead of (2.73). This illustrates another situation with which the versatile analog circuit representations in the previous paragraph must cope.

Regarding Step 7, Fig. 2.22 shows an analog circuit schematic to implement the calculation, in real time during the simulation, of \(d\) and \(d_2\) to allow for smooth transitions between CCM and DCM.
2.6.4. Model verification and comments

Verification of the average model was conducted through Saber simulations. Schematics and template listings for these simulations are included in Appendix A.

Figure 2.23 shows duty ratios, inductor current and output voltage waveforms from switch and average model. A zoom-in on these waveforms is shown in Fig. 2.24. It is apparent that average model waveforms very closely track those moving averages from the switch model for large transients, both in CCM and DCM operation even when the converter moves back and forth between those modes.

It is important to point out that there were no convergence problems for the average model and that waveform tracking was very good for simulation step size more than one order of magnitude larger than the step used with the switch model.

This close tracking indicates that the average model can be used to predict start-up transients and feedback loops effects and hence it can help in power stage and control design.

In these simulations good familiarity with the specific circuit simulator and reliable simulation practices is a must.
a) Switch structures (circuit topologies)

b) Operating waveforms

Fig. 2.8. Starting point for new average modeling procedure
Fig. 2.9. Step 1: Slow/fast variables separation
Fig. 2.10. Identification of Linear Time Invariant Input/Output parts.
Fig.2.11. Step 3: Identification of “dependent” variable drawn from input and “independent” variable delivered to output LTI parts.
Fig. 2.12. Step 4: Calculation of controlled source one-cycle average

- \( \overline{i_S} = d \overline{i_L} \)
- \( \overline{v_D} = d \overline{v_{in}} \)

**a)** Dependent and independent waveforms

**b)** One-cycle average

*Fig.2.12. Step 4: Calculation of controlled source one-cycle average*
$m_1 \; d_1 \; T_s = m_2 \; d_2 \; T_s = i_{pk}$

$$i_L = \frac{(d_1 + d_2)}{2} i_{pk} = \frac{i_{pk}}{2}$$

*a) Typical waveforms*  
*b) Algebraic constraint derivation*

**Fig.2.13. Step 5: Calculation of algebraic constraints**
\[ i^* - m_r d_1 T_S = i_{pk} \]

\[ \overline{i_L} + \frac{T_S}{2} \left[ m_1 d^2 + m_2 (1-d)^2 \right] = i_{pk} \]

a) Waveforms with feedback loop 

b) Loop-induced constraint derivation

Fig.2.14. Step 6: Incorporation of feedback loop
Fig. 2.15. Step 7: implementation of circuit simulator oriented average model

a) Root finder through loop around operational amplifier

b) Robust treatment of equation and root selection

Known input vector

\[ Z = \{i^*, i_L, V_{in}, V_o\} \]

Zero divisor potential problem

\[ d_2 = \frac{m_1 d_1}{m_2} \]

Root interval constraint through limiter

\[ d_1, m_2 - d_1, m_1 = 0 \]

\[ i^* (d_1 + d_2) - 2 i_L = 0 \]

\[ i^* - m_r d_1 T_s - i_{pk} = 0 \]

Zero divisor potential problem

\[ i_{pk} = \frac{2 i_L}{d_1 + d_2} \]
a) Averaged circuit model I

b) Averaged circuit model II

c) Averaged circuit model III

Fig. 2.16. Average circuit model for buck converter in CCM operation
Fig. 2.17. Buck converter in DCM operation
Fig. 2.18. Average circuit model for buck converter in DCM.
Fig. 2.19. Average circuit models for buck converter in CCM and DCM operation

a) Transformer based average circuit model

b) Controlled-source based average circuit model

Fig. 2.19. Average circuit models for buck converter in CCM and DCM operation
Fig. 2.20. Input/output structure average circuit models for buck converter in CCM and DCM operation

a) Transformer based average circuit model

b) Controlled-source based average circuit model

Fig.2.20. Input/output structure average circuit models for buck converter in CCM and DCM operation
Fig. 2.21. Analog computation of \( d_2 \).
Fig. 2.22. Analog computation of $d$ and $d_2$ with feedback loop.
Fig. 2.23. Simulation results from average (red-dashed) and switch (green-solid) mode. Top: duty ratios, middle: inductor current, bottom: output voltage.
Fig. 2.24. Simulation results from average (red-dashed) and switch (green-solid) mode. Top: duty ratios, middle: inductor current, bottom: output voltage.
3. MODELING OF THE ZVS-FB-PWM DC-DC CONVERTER

The new procedure for the derivation of autonomous average circuit models given in the previous chapter is complemented here and then applied to the ZVS-FB-PWM converter to get a new model. Previous averaged models were based on steady-state operation and neglected variables’ ripple effects. As a result their range of validity, i.e. frequency, large signal excursions, was limited and could not make a smooth transition between CCM and DCM operation. Comparison of simulation results between new and previous model shows that most of those limitations have been overcome. Furthermore a small-signal model is derived through linearization of the new average model and within the circuit simulator; whereas previous small signal models were obtained through graphical approximations of perturbations evolution.

3.1 ZVS-FB-PWM Converter Operation

The ZVS-FB PWM dc-dc converter and its typical switch structures (circuit topologies) in CCM operation are shown in Fig. 3.1(a) and (b) whereas its typical waveforms are depicted in Fig. 3.2. It operates with zero-voltage switching in both legs and it is widely used in high power applications. Its complete analysis and design considerations as well as its small signal models can be found in [S1] whereas some large and small-signal models are provided in [T4, V5].

3.1.1. CCM operation

Figure 3.1(b) and 3.2 describe CCM operation of the converter through equivalent circuit structures for each major switch configuration interval, i.e. Charging, Transfer and Circulating, whose characteristics are summarized below [S1, V5], and waveforms for bridge voltage, \( V_{ab} \), blocking capacitor voltage, \( V_{ab} \), primary current, \( I_p \), bus current, \( I_{bus} \), filter inductor current, \( I_f \), rectifier’s output voltage, \( V_s \), and output voltage, \( V_0 \). Blocking capacitor voltage is assumed negligible with respect to both input and reflected output voltage as Fig. 3.2 suggests.

Charging Stage. Starts at \( t_0 \) when input voltage \( V_{in} \) is applied between nodes a and b, and ends at \( t_1 \) when primary current equals reflected filter inductor current. On the primary side, after neglecting transformer’s magnetizing current and second and higher order terms in Taylor’s series expansion, input voltage determines the rate of change of current in the leakage inductor \( L_{Lk} \), i.e. \( ml \) in Fig. 3.2 and given by

\[
ml = \frac{V_{in}}{L_{Lk}},
\]  

(3.1)
while rectifier diodes short circuit transformer’s secondary winding and hence the output voltage $V_0$, whose changes over a switching cycle are assumed negligible, determines the rate of change of current in the filter inductor $L_f$, i.e. $m4$ in Fig. 3.2 and given by

$$m4 = \frac{V_0}{L_f}.$$  (3.2)

According to (3.1) the change in primary current during this stage is approximately given by

$$I_1^p - I_0^p = \left( \frac{V_n}{L_{ik}} \right) (t_i - t_0) = (mI) \cdot (D_{ch} \cdot T_s),$$  (3.3)

from where duty ratio for this stage, $D_{ch}$, is given by

$$\frac{I_1^p - I_0^p}{mI \cdot T_s} = D_{ch}.$$  (3.4)

Similarly from (3.2) the change in the filter inductor current during this stage is approximately given by

$$I_1^f - I_0^f = \left( \frac{V_0}{L_f} \right) (t_i - t_0) = (m4) \cdot (D_{ch} \cdot T_s).$$  (3.7)

Current changes in (3.3) and (3.7) are related by the transformer’s turns ratio $N$, i.e.

$$I_1^f - I_0^f = N \cdot (I_1^p - I_0^p).$$  (3.5)

**Transfer Stage.** Starts at $t_1$ after primary current equals reflected filter inductor current with transformer in normal operation and hence instantaneous primary current and filter inductor current are related by the transformer’s turns ratio and ends at $t_2$ when $V_{ab}$ becomes zero. Reflection of input voltage and transformer’s leakage inductance to the secondary side gives, for this stage, the equivalent circuit shown in Fig. 3.1. From here the rate of change of primary current, $m2$ in Fig. 3.2, is given by

$$\frac{V_n - N \cdot V_0}{L_{ik} + N^2 \cdot L_f} = m2,$$  (3.6)

and from Fig. 3.2 the duty ratio for this stage is

$$D_{on} = \frac{D_{on} - \frac{I_1^p - I_0^p}{mI \cdot T_s}}{mI \cdot T_s}.$$  (3.7)
Fig. 3.1. ZVS-FB PWM converter

a) Circuit schematic

b) Switch structures in CCM

**Fig. 3.1. ZVS-FB PWM converter**
Fig. 3.2. Typical ZVS-FB PWM converter waveforms in CCM.
Change in filter inductor current is given by

\[ I_f^2 - I_f^1 = \left( \frac{V_{in}/N - V_o}{L_{lk}/N^2 + L_f} \right) \cdot (t_2 - t_1) = (N \cdot m2) \cdot \left( D_{on} \cdot T_s \right), \quad (3.8) \]

where \( m2 \) is defined by the first bracket and \( D_{on} = \frac{t_2 - t_1}{T_s} \).

Circulating stage starts when bridge voltage \( V_{ab} \) becomes zero, primary current and filter inductor current are related by the transformer’s turns ration, and the change in inductor current for this interval is expressed as

\[ I_f^3 - I_f^2 = \left( \frac{V_o}{L_{lk}/N^2 + L_f} \right) \cdot (t_3 - t_2) = \left( N \cdot m3 \right) \cdot \left[ (I - D_{on}) \cdot T_s \right], \quad (3.9) \]

where \( m3 \) is defined by the first bracket, and the commanded duty-ratio, \( D_{on} \), is given by

\[ D_{on} = D_{ch} + D_{on}. \quad (3.10) \]

Equations (3.1) through (3.6) together with Fig. 3.3 can now be used to calculate the one-cycle average of filter inductor current \( I_f \), i.e.

\[ I_f = \left( \frac{I_0^f + I_1^f}{2} \right) \cdot (D_{on} - D_{on}) + \left( \frac{I_1^f + I_2^f}{2} \right) \cdot D_{on} + \left( \frac{I_2^f + I_3^f}{2} \right) \cdot (I - D_{on}). \quad (3.11) \]

The set (3.1) through (3.11) represents the algebraic constraint set needed to develop the average circuit model.

**3.1.2. DCM operation**

Typical waveforms for DCM operation are shown in Fig. 3.4. Clearly there is no charging stage and hence commanded duty cycle determines duration of transfer stage.

Peak filter inductor current is given by

\[ I_f^{pk} = \left( \frac{V_{in}/N - V_o}{L_{lk}/N^2 + L_f} \right) \cdot (t_1 - t_0) = (N \cdot m2) \cdot \left( D_{on} \cdot T_s \right) \quad (3.12) \]

and by

\[ I_f^{pk} = \left( \frac{V_o}{L_{lk}/N^2 + L_f} \right) \cdot (t_2 - t_1) = (N \cdot m3) \cdot \left( D2 \cdot T_s \right). \quad (3.13) \]
One-cycle average inductor current is calculated from (3.8) and (3.9) as

\[ \bar{I}_f = I_{pk} \cdot \left( \frac{D_{on} + D2}{2} \right), \quad (3.14) \]

which gives the same DCM-CCM boundary condition as in the buck converter, i.e.

\[ \bar{I}_f = \frac{I_{pk}}{2}. \quad (3.15) \]

Equating (3.12) and (3.13) gives

\[ D2 = \frac{D_{on} \cdot m^2}{m^3} \quad (3.16) \]

and its substitution together with (3.12) into (3.14) gives the algebraic constraint on one-cycle average inductor current, i.e.

\[ \bar{I}_f = \frac{m^2 \cdot (D_{on})^2 \cdot T_s}{2} \left( 1 + \frac{m^2}{m^3} \right). \quad (3.17) \]

The same as in the buck converter, this constraint indicates that one-cycle average filter inductor current is not an independent state.

3.2. New Average Circuit Model for the ZVS-FB Converter

Systematic application of the new procedure leads to the input-output structure average model of the ZVS-FB PWM dc-dc converter shown in Fig. 3.4(a) as detailed next.

3.2.1. Step 1: Fast/slow classification of state variables

From Figs. 3.1 and 3.2, filter inductor current and output capacitor voltage qualify as slow variables in CCM to be used as states in the average circuit model. However in DCM only the output capacitor remains as a slow state. Filter inductor current stays at zero during a significant amount of time within a switching cycle, which leads to having its one-cycle average fully determined by present switching cycle condition and hence being converted to a fast variable.

Primary current is not considered a relevant average state variable, even though it corresponds to leakage inductor state variable, because its moving average is zero in steady state operation and exhibits large components at one half the switching frequency and higher harmonics during transient regime. In other words no new information would
be provided in steady state and time varying effects would have to be included in the model.

3.2.2. Step 2: LTI input/output parts

Output filter and input voltage source get selected as LTI networks according to circuit topologies in Fig. 3.1(b).

3.2.3. Step 3: “Independent” variable drawn from LTI input network and “dependent” variable delivered to LTI output network

Average bus current is the “dependent variable” drawn from input voltage source whereas secondary rectifier’s output voltage is the “independent variable” applied to the output filter during CCM operation. On the other hand one cycle average inductor current becomes the sought independent variable fed to the output section during DCM operation the same as in the buck converter.

3.2.4. Step 4: Calculation of one-cycle average for the variables in the previous step

CCM. According to Figs. 3.1(b), 3.2 and 3.4(c) rectifier voltage is equal to zero during charging stage; it becomes a function of input source voltage and output capacitor voltage, during transfer stage after neglecting blocking capacitor voltage, i.e.

\[
V_s = \frac{V_{\text{in}}}{N} \cdot L_f + \frac{V_0}{N^2} \cdot \frac{L_{\text{th}}}{N^2}, \quad t_1 \leq t \leq t_2,
\]  

(3.18)

and only a function of capacitor voltage during circulating stage given by

\[
V_s = \frac{V_0}{N^2} \cdot \frac{L_{\text{th}}}{N^2 + L_f}, \quad t_2 \leq t \leq t_1.
\]  

(3.19)

From (3.18), (319) and Fig. 3.2 the one-cycle average rectifier voltage given to controlled source \( V_2 \) can be expressed as

\[
V_2 = \bar{V}_s = \frac{V_{\text{in}}}{N} \cdot L_f + \frac{V_0}{N^2} \cdot \frac{L_{\text{th}}}{N^2} \cdot D_{\text{on}} + \frac{V_0}{N^2} \cdot \frac{L_{\text{th}}}{N^2 + L_f} \cdot (1 - D_{\text{on}}).
\]  

(3.20)
Fig. 3.3. Typical ZVS-FB PWM converter waveforms in DCM.
The average circuit model shown in Fig. 3.4(b) includes transformer’s leakage inductance reflected to the secondary side to highlight its dynamic effects, which are implicitly included in (3.20). The model becomes equivalent to that in Fig. 3.4(a) if $V_{eq}$ is computed to make $V_2$ appear in between the two inductors, that is, to have the same average voltage delivered to the output filter. Therefore $V_{eq}$ is given by

$$V_{eq} = \frac{V_{in}}{N} \cdot D_{trf} + \frac{V_0 \cdot L_{lk}}{N^2 \cdot L_f} \cdot (I - D_{ch}). \quad (3.21)$$

Fig. 3.4 indicates that controlled current source $I_1$ corresponds to one cycle average bus current. From Figs. 3.1(b) and 3.2, $I_1$ can be computed as

$$I_1 = \bar{I}_{bus} = \frac{(-I_{o}^p + I_p)}{2} \cdot D_{ch} + \frac{(I_{i}^p + I_p)}{2} \cdot D_{trf}. \quad (3.22)$$

Calculation of $D_{trf}$ is again carried out on line in the simulator by closing the loop around operational amplifiers to find the root located between 0 and $D_{on}$. Equations (3.1) through (3.22) can be combined to find the expression with $D_{trf}$ as the only unknown or they can be arranged to solve for as many of the unknown quantities as desired.

**DCM.** One-cycle average filter inductor current is now given by (3.14) and the average circuit model is shown in Fig. 3.5(a). Since this situation its very similar to that found in the buck converter model the value $\bar{I}_f$ may be enforced by adjusting, in the average circuit model shown in Fig. 3.4, controlled source $V_2$, which in turn depends on $D_2$. Therefore filter inductor current can be treated the same as in the buck converter model, *i.e.* a loop around an operation amplifier that enforces algebraic constraint (3.14).

Bus current, according to (3.12) and Figs. 3.2 and 3.4 is given by

$$I_1 = \frac{I_{f}^{pk} \cdot D_{on}}{2} = \frac{m2 \cdot (D_{on})^2 \cdot T_s}{2}. \quad (3.23)$$

### 3.2.5. Step 5: Calculation of algebraic constraints

These constraints are already described in (3.1) through (3.23) both for CCM and DCM operation.

### 3.2.6. Step 7: Implementation of circuit oriented simulation

Fig. 3.6 shows the same technique used in Chapter 2 to compute, in real time during the simulation, $D_{trf}$ and $D_2$ both in CCM and DCM for the average model.
3.3. Previous Average Models for the ZVS-FB Converter

Models presented in [T4, V5] used the PWM switching model in [V8]. However [T4, V5] neglects some effects of transformer’s leakage inductance upon rectifier’s output voltage and upon filter inductor current slopes. As a result this average model neither makes a smooth transition between CCM and DCM nor gives an accurate small-signal model through linearization.

[V5] does not provide a large signal average model but only a DC (steady-state) model and a small-signal model is developed by adding some controlled sources to the small-signal model, derived through the PWM switching model in [V8], for the Buck converter. It also neglects some effects of transformer’s leakage inductance upon rectifier’s output voltage and upon filter inductor current slopes.

None of these models follows the correct introduction order for perturbation and steady-state constraints pointed out in [V3] and hence validity-range of derived small-signal models gets compromised.

3.4. Simulation Results

New and previous [T4] average models of the ZVS-FB PWM dc-dc converter get compared to its switching model through transient simulations. These simulations are carried out for several sets of parameter values similar to those used in [V5], which are listed in Table 1. Commanded duty-ratio $D_{on}$ for all simulation is shown on top graph of Fig. 3.23. Appendix B contains templates for the Saber simulator.

State variables from the new average model very closely follow moving average of their respective counterparts in the switching model for all parameter sets, Figs. 3.7 through 3.20, whereas state variables from previous model can only exhibit good tracking under special conditions, Figs. 3.14, 3.17 and 3.19, and can present faster or slower dynamics than that of the switching model depending of operating conditions, Figs. 3.9, 3.11, 3.14 and 3.190. Furthermore the new average model maintains excellent tracking during transient regimes that go back and forth between CCM and DCM as Figs. 3.8, 3.9, 3.10, 3.13, 3.16, 3.17 and 3.18 show.

3.4.1. Transient simulations for parameter set 1

Simulations results for this set are shown in Fig. 3.8 through 3.10. Even though the ratio of filter inductance to transformer’s leakage inductance is 60 and hence effects of the latter upon average behavior might be assumed negligible, as the previous model [T4] does, Figs. 3.8 through 3.10 indicate that those effects are still relevant. The new model maintains excellent state variables tracking for back and forth transitions between CCM and DCM operating modes whereas the previous model [T4] lacks it due to the loose approximation to model leakage inductor influence as Fig. 3.7, 3.9 and 3.10 clearly show. The large in-rush current shown in Figs. 3.7 and 3.8, not allowed in practice by the
start-up sequence, was used here to solely illustrate average circuit model tracking properties. Commanded duty-ratio $D_{on}$ for all simulation is shown on top graph of Fig. 3.19. Figs. 3.7 and 3.8 show responses to zero initial conditions for all models.

Table 1 Parameter value sets for transient response of ZVS-FB converter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Set 1</th>
<th>Set 2</th>
<th>Set 3</th>
<th>Set 4</th>
<th>Set 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turns Ratio</td>
<td>5</td>
<td>1</td>
<td>1</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>Leakage Induc. $\mu H$</td>
<td>5</td>
<td>30</td>
<td>5</td>
<td>5</td>
<td>30</td>
</tr>
<tr>
<td>Filter Induc. $\mu H$</td>
<td>12</td>
<td>30</td>
<td>12</td>
<td>12</td>
<td>100</td>
</tr>
<tr>
<td>Filter Cap. $\mu F$</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>200</td>
<td>100</td>
</tr>
<tr>
<td>Load Resist. $\Omega$</td>
<td>20</td>
<td>75</td>
<td>5</td>
<td>10</td>
<td>75</td>
</tr>
<tr>
<td>$L_f/(L_{lk}/N^2)$</td>
<td>60</td>
<td>1</td>
<td>2.4</td>
<td>60</td>
<td>3.33</td>
</tr>
<tr>
<td>$V_{in} \ [V]$</td>
<td>600</td>
<td>600</td>
<td>600</td>
<td>600</td>
<td>600</td>
</tr>
</tbody>
</table>

3.4.2. Transient simulations for parameter set 2

Simulation results for this set are shown in Fig. 3.11 through 3.13. The ratio of filter inductance to transformer’s leakage inductance is 1 and hence effects of the latter upon average behavior are very strong, contrary to what the previous model assumes. Fig. 3.12 clearly shows three different slopes on inductor current waveforms, as considered by the new model derivation above, and very close tracking characteristics of the new model for transitions between CCM and DCM operating modes. In contrast to this the previous model completely lacks tracking. Furthermore the previous model exhibits slower dynamics than the correct one for certain operating conditions during the transient and faster dynamics than the correct one for other operating conditions. As a result the previous model cannot be used either for transient or stability analysis.
3.4.3. Transient simulations for parameter set 3

Figures 3.14 through 3.16 show simulation results for this special set of parameter values. The latter were selected so that the steady state part of the simulation from the previous average model matched very well results from the other two models but the fast transients show not so good an agreement. Since results from previous average model for set 2 showed faster and slower than correct dynamics it seemed possible to get a correct response for certain range of parameter values and operating conditions. Obviously this example warns about apparent good results when the ratio filter inductance to reflected leakage inductance is relatively low. The same excellent tracking is observed for the new model.

3.4.4. Transient simulations for parameter set 4

Figures 3.20 and 3.21 show simulation results for another special set of parameter values. The latter were selected very similar to set 1, i.e. large ratio of filter inductance to reflected leakage inductance, but to provide smooth transition between CCM and DCM for the previous average model and to coincide with the other two models. These results highlight the region of validity for the previous model. Once again the new model shows excellent tracking.

Table 2. Parameter value set I for small-signal model and transient response of Buck, ZVS-FB and ZVZCS-FB converters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Buck</th>
<th>ZVS</th>
<th>ZVZCS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turns Ratio</td>
<td>NA</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Leakage Induct. $[\mu H]$</td>
<td>NA</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Blocking Cap. $[\mu F]$</td>
<td>NA</td>
<td>20</td>
<td>1</td>
</tr>
<tr>
<td>Filter Induc. $[\mu H]$</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Filter Cap. $[\mu F]$</td>
<td>200</td>
<td>200</td>
<td>20</td>
</tr>
<tr>
<td>Load Resist. $\Omega$</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
</tr>
<tr>
<td>Saturable Reactor $[\mu V \text{–} \text{sec}]$</td>
<td>NA</td>
<td>NA</td>
<td>60</td>
</tr>
<tr>
<td>Vin $[V]$</td>
<td>55</td>
<td>330</td>
<td>330</td>
</tr>
</tbody>
</table>
Table 3. Parameter value set II for small-signal model and transient response of Buck, ZVS-FB and ZVZCS-FB converters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Buck</th>
<th>ZVS</th>
<th>ZVZCS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turns Ratio</td>
<td>NA</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Leakage Induct. $\mu H$</td>
<td>NA</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Blocking Cap. $\mu F$</td>
<td>NA</td>
<td>20</td>
<td>1</td>
</tr>
<tr>
<td>Filter Induc. $\mu H$</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Filter Cap. $\mu F$</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Load Resist. $\Omega$</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
</tr>
<tr>
<td>Saturable Reactor $\mu V - sec$</td>
<td>NA</td>
<td>NA</td>
<td>60</td>
</tr>
<tr>
<td>Vin $V$</td>
<td>330</td>
<td>330</td>
<td>330</td>
</tr>
</tbody>
</table>

3.4.5. Transient simulations for parameter set 5

Figures 3.22 and 3.23 show simulation results for another special set of parameter values. Now the latter were selected very similar to set 2, i.e. low ratio of filter inductance to leakage inductance. However the results look quite different from those for set 2 since good tracking is seem from the previous average model. Here the new average model also exhibited excellent tracking.

3.4.6 Transient and small-signal simulation results.

Results from transient and linearization, within the same circuit simulator, for the average model with two different resistive load values are shown in Figs. 3.21 through 3.24 for Buck, ZVS and ZVZCS converters. The latter, thoroughly analyzed in chapter 4, is included here to highlight the contrast between the two soft-switched converters with respect to the damping added to the output filter. The transfer functions shown in Figs. 3.22 and 3.24, are $D_{on}$ to filter inductor current and $D_{on}$ to capacitor voltage. In the buck
converter these transfer functions have the same shape, i.e. pole frequency and damping, as those from output low pass filter except for a different gain factor. Both ZVS-FB and ZVZCS-FB converters alter output filter damping coefficient and pole frequency. These changes depend on parameters values and/or operating conditions for both ZVS-FB and ZVZCS-FB converters. With parameter value Set I in Table 2 both soft-switched converters change the damping factor by a fairly large amount albeit in opposite directions. For the other parameter value set the ZVZCS-FB converter exerts a very small reduction in damping whereas the ZVS-FB converter introduces a large increment.
Fig. 3.4. ZVS converter equivalent average models and waveforms in CCM.

- **a) Input-output structure model**

- **b) Mixed input-output-internal structure model**

- **c) Waveforms for controlled-source average calculation**

\[ I_1 = \bar{I}_{bus}(t) \quad \text{and} \quad V_2 = \bar{V}_s(t) \]
a) Input-output structure model

\[ I_1 = \overline{I_{bus}} \]

\[ I_2 = \overline{I_f} \]

b) Waveforms for controlled-source average calculation

c) Waveforms for controlled-source average calculation

Fig. 3.5. ZVS converter equivalent average model and waveforms in DCM.
Fig. 3.6. Analog schematic for computation of $D_{\text{trf}}$ and $D_2$.
Fig. 3.7. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 1 with zero initial state for all models.
Fig. 3.8. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 1 with zero initial state for all models.
Fig. 3.9. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 1 with zero initial state for all models.
Fig. 3.10. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 1 with zero initial state for all models.
Fig. 3.11. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 2 with zero initial state for all models.
Fig. 3.12. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 2 with zero initial state for all models.
Fig. 3.13. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 2 with zero initial state for all models.
Fig. 3.14. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 3 with zero initial state for all models.
Fig. 3.15. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 3 with zero initial state for all models.
Fig. 3.16. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 3 with zero initial state for all models.
Fig. 3. 17. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 4 with zero initial state for all models.
Fig. 3.18. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 4 with zero initial state for all models.
Fig. 3.19. Duty ratios (top), filter inductor current (middle) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 5 with zero initial state for all models.
Fig. 3.20. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), new average (pink) and previous average (black) models for parameter set 5 with zero initial state for all models.
Fig. 3.21. Capacitor voltage (top) and filter inductor current (bottom) transient response from new average models for Buck (red), ZVS-FB (blue) and ZVZCS-FB (black) converters with parameter set I.
Fig. 3.22. Capacitor voltage (top) and filter inductor current (bottom) transfer functions from new average models for Buck (red), ZVS-FB (blue) and ZVZCS-FB (black) converters with parameter set I.
Fig. 3.23. Capacitor voltage (top) and filter inductor current (bottom) transient response from new average models for Buck (red), ZVS-FB (blue) and ZVZCS-FB (black) converters with parameter set II.
Fig. 3.24. Capacitor voltage (top) and filter inductor current (bottom) transfer functions from new average models for Buck (red), ZVS-FB (blue) and ZVZCS-FB (black) converters with parameter set II.
4. MODELING OF THE SATURABLE INDUCTOR BASED ZVZCS-FB-PWM DC-DC CONVERTER

The new procedure for the derivation of autonomous average circuit models given in Chapter 2 is again complemented here and then applied to the ZVZCS-FB-PWM converter to get its circuit average model, which is a new result.

Comparison of simulation results between average and switching model shows that most of the average dynamics is preserved. Furthermore a small-signal model is derived through linearization of the new average model within the circuit simulator and compared to those for buck and ZVS models.

4.1 ZVZCS-FB-PWM Converter Operation

The ZVZCS-FB topology introduced in [C11], Fig. 4.1(a), and whose switch structures and typical waveforms for CCM operation are shown in Fig. 4.1(b) and 4.2, respectively, operates with zero-voltage switching in the leading leg and zero-current switching in the lagging leg for very wide load and line ranges. Although initially intended to have its lagging leg built with IGBTs, the latter’s switching speed limitations prevent their application at very high frequencies, where MOSFETs become the only choice. However, by having conduction losses in the primary side strongly reduced through almost complete elimination of freewheeling stage in that side, the ZVZCS topology can still provide high efficiency for wide line range even with MOSFETs.

Appendix C provides detailed design procedure for the converter as well as its waveforms and their exact describing equations for CCM operation. In this chapter only brief descriptions of waveforms relevant to the development of the averaged circuit model and their simplified expressions are presented.

4.1.1. CCM operation

Fig. 4.1(b) shows major topological stages for CCM operation of the ZVZCS converter, i.e. Blocking, Charging, Transfer, Resetting and Off, whose characteristics are summarized below [C11]. Fig. 4.2 shows typical waveforms for bridge voltage, $V_{ab}$, primary current, $I_p$, bus current, $I_{bus}$, blocking capacitor voltage, $V_{cb}$, filter inductor current, $I_f$, rectifier’s output voltage, $V_s$ and output voltage, $V_0$.

Assume the switching cycle starts with the blocking stage at $t_o$, when bridge voltage $V_{ab}$ becomes positive and saturable reactor blocks any primary current, and ends at $t_f$ when the reactor gets saturated. The sum of input voltage and blocking capacitor voltage determines the rate of change of flux in the saturable reactor. The change of flux during this stage amounts to
\[
\Delta \phi_{blk} = (t_f - t_i) \left( \frac{V_{in} + V_{cpk}}{N_{sr}} \right) = (D_{blk} \cdot T_s) \left( \frac{V_{in} + V_{cpk}}{N_{sr}} \right),
\]

where \( D_{blk}, N_{sr} \) and \( V_{cpk} \) are blocking stage duty-ratio, saturable reactor number of turns and peak blocking capacitor voltage, respectively. On the secondary side output voltage determines rate of change in filter inductor current, \( m4 \) in Fig. 4.2, as

\[
m4 = \frac{V_0}{L_f}.
\]

During charging stage, \((t_1,t_2)\), the same rate of change applies to filter inductor current whereas the change in primary current, after neglecting transformer’s magnetizing current and second order terms in Taylor’s series expansion, is approximately given by

\[
I_p^f = \left( \frac{V_{in} + V_{cpk}}{L_{lk}} \right) (t_2 - t_1) = (m1) \cdot (D_{ch} \cdot T_s),
\]

where slope \( m1 \), shown in Fig. 4.3, is defined by the first bracket, \( D_{ch} \) corresponds to charging stage duty ratio and the remaining quantities are defined in Fig. 4.2.

At time instant \( t_2 \) primary current and filter inductor current are related by transformer’s turns ratio, i.e.

\[
I_p^f = I_s^f \cdot N,
\]

and they remain so through transfer stage, which ends at \( t_3 \) with commanded duty-cycle \( D_{on} \).

\[
D_{on} \cdot T_s = (t_3 - t_0) = (D_{blk} + D_{ch} + D_{onf}) \cdot T_s.
\]

Reflection of input voltage and transformer leakage inductance to the secondary side leads to the equivalent circuit for this stage, Fig. 4.1(b). Change in the filter inductor current, after neglecting blocking capacitor effects, is approximately given by

\[
I_s^f - I_p^f = \left( \frac{V_{in}/N - V_o}{L_{lk}/N^2 + L_f} \right) \cdot (t_3 - t_2) = (N \cdot m2) \cdot (D_{onf} \cdot T_s),
\]

where slope \( N \cdot m2 \) is defined by the first bracket and the other terms by Fig. 4.2. Blocking capacitor voltage, \( V_{cb} \), is neglected here to simplify the derivation and because its contribution is very small as later simulation results confirm.
Figure 4.2. ZVZCS-FB PWM primary and filter inductor current waveforms in CCM.
Resetting stage starts at \( t_3 \) when bridge voltage \( V_{ab} \) becomes zero and it ends when primary current does the same at \( t_4 \). Duration of this stage is given by

\[
t_4 - t_3 = D_{res} \cdot T_s = \frac{1}{\sqrt{L_{th} \cdot C_{blk}}} \cdot \arcsin \left( \frac{I^p_3 \cdot \sqrt{L_{th}}}{V_{cpk} \cdot C_{blk}} \right).
\] (4.6)

Off stage begins at \( t_4 \) when saturable reactor blocks any primary current by taking \( V_{cpk} \) as its flux rate of change and it ends at \((t_0 + T_s)\) with half of primary switching cycle when \( V_{ab} \) becomes negative as shown in Fig. 4.2. During this stage the change in flux across the saturable reactor is given by

\[
\Delta \phi_{off} = \frac{V_{cpk} \cdot (I - D_{on} - D_{res}) \cdot T_s}{N_{sr}},
\] (4.7)

which together with saturable reactor volt-second blocking capability determines blocking stage duration, i.e.

\[
\Delta \phi_{blk} = 2 \cdot \phi_{sat} - \Delta \phi_{off},
\] (4.8)

where \( \Delta \phi_{blk} \) is given by (4.1) and \( 2 \cdot \phi_{sat} \) is the volt-second blocking capability of the saturable reactor.

Expressions for peak blocking capacitor voltage, \( V_{cpk} \), filter inductor current average and ripple values, \( I_L \equiv I_f \) and \( \Delta I_f \) are calculated next to complete the set of equations. An approximation to \( V_{cpk} \) value is obtained by looking at converter’s steady-state operation and by taking into consideration the relevance of each stage’s duration upon change in the capacitor voltage. These voltage changes during transfer and resetting stages are respectively approximated by

\[
\Delta V_{c-ref} = \frac{I_L \cdot D_{ref} \cdot T_s}{N \cdot C_h}
\] (4.9)

and

\[
\Delta V_{c-res} = \frac{(I^f_3) \cdot D_{res} \cdot T_s}{2 \cdot N \cdot C_h}
\] (4.10)

From Figs. 4.2 and 4.5, after neglecting voltage change during charging stage, \( V_{cpk} \) is given by
Figure 4.3. ZVZCS-FB PWM primary and filter inductor current waveforms in DCM.
\[ V_{\text{epk}} = \frac{\Delta V_{\text{c-trf}} + \Delta V_{\text{c-res}}}{2}. \] \hspace{1cm} (4.11)

On the other hand \( \Delta I_f \) is calculated as
\[ \Delta I_f = D_{\text{trf}} \cdot (I_f' - I_f^\alpha) + (1 - D_{\text{trf}}) \cdot (I_f' - I_f^\beta), \] \hspace{1cm} (4.12)

where
\[ I_f' - I_f^\alpha = \left( \frac{V_o}{L_f} \right) \cdot (1 - D_{\text{trf}}) \cdot T_s = m4 \cdot (1 - D_{\text{trf}}) \cdot T_s. \] \hspace{1cm} (4.13)

**4.1.2. DCM operation**

Typical waveforms for DCM operation are shown in Fig. 4.3. Clearly there is no charging stage and hence commanded duty cycle equals the sum of blocking and transfer stages, i.e.
\[ D_{\text{on}} = D_{\text{blk}} + D_{\text{trf}}. \] \hspace{1cm} (4.14)

Peak filter inductor current is given by
\[ I_f^{pk} = \left( \frac{V_o}{L_{\text{tk}} / N^2 + L_f} \right) \cdot (t_2 - t_1) = (N \cdot m2) \cdot (D_{\text{trf}} \cdot T_s). \] \hspace{1cm} (4.15)

and by
\[ I_f^{pk} = \left( \frac{V_o}{L_{\text{tk}} / N^2 + L_f} \right) \cdot (t_3 - t_2) = (m4) \cdot (D2 \cdot T_s). \] \hspace{1cm} (4.16)

One cycle average inductor current is calculated from (4.15) and (4.16) as
\[ I_L = \overline{I_f} = \frac{I_f^{pk} \cdot (D_{\text{trf}} + D2)}{2}, \] \hspace{1cm} (4.17)

which gives the same DCM-CCM boundary condition as in the buck converter, i.e.
\[ \overline{I_f} = \frac{I_f^{pk}}{2}. \] \hspace{1cm} (4.18)
Equating (4.15) and (4.16) gives

\[ D2 = \frac{D_{\text{trf}} \cdot N \cdot m2}{m4} \]  \hspace{1cm} (4.19)

and its substitution into (4.17) gives the algebraic constraint on one-cycle average inductor current, i.e.

\[ \bar{I}_f = \frac{N \cdot m2 \cdot (D_{\text{trf}})^2 \cdot T_s}{2} \left( 1 + \frac{N \cdot m2}{m4} \right) . \]  \hspace{1cm} (4.20)

As in the Buck converter, this constraint indicates that one-cycle average filter inductor current is not an independent average state.

Equation (4.1) still applies during blocking stage and (4.7) now represents the change in flux across the saturable reactor during the sum of intervals for off and idling stages. On the other hand expressions for capacitor voltage, i.e. (4.9), (4.10) become

\[ \Delta V_{c-\text{trf}} = \frac{I_{pk} \cdot D_{\text{trf}} \cdot T_s}{2 \cdot N \cdot C_h} , \]  \hspace{1cm} (4.21)

and

\[ \Delta V_{c-\text{res}} = \frac{I_{pk} \cdot D_{\text{res}} \cdot T_s}{2 \cdot N \cdot C_{ch}} , \]  \hspace{1cm} (4.22)

whereas (4.11) remains the same.

### 4.2. New Average Circuit Model for the ZVZCS-FB Converter

Systematic application of the new procedure leads to the input-output structure average model of the ZVZCS-FB PWM dc-dc converter shown in Fig. 4.4(a) as detailed next.

#### 4.2.1. Step 1: Fast/slow classification of state variables

Figure 4.2 indicates that filter inductor current and output capacitor voltage qualify as slow variables in CCM to be used as states in the average circuit model. However in DCM only the output capacitor remains as a slow state. Similarly to the situation in Chapter 3 filter inductor current stays at zero during a significant amount of time within a switching cycle, which leads to having its one-cycle average fully determined by present switching cycle condition and hence being converted to a fast variable.
**Fig. 4.4. ZVZCS converter equivalent average models and waveforms in CCM.**

- **a) Input–output structure**
- **b) Mixed input-output-internal structure**
- **c) Typical waveforms**

- $I_1 = \overline{I_{bus}}(t)$
- $V_2 = \overline{V_s}(t)$
Again primary current is discarded as a relevant average state variable, even though it corresponds to leakage inductor state variable, because its moving average is zero in steady state operation and exhibits large components at one half the switching frequency and higher harmonics during transient regime. In other words no new information would be provided in steady state and time varying effects would have to be included in the model.

Blocking capacitor voltage gets classified as a fast variable and its waveform in Fig. 4.2 indicates that it is an energy holding element. Its treatment is presented later in this chapter.

4.2.2. Step 2: LTI input/output parts

Output filter and input voltage source get selected as LTI networks according to circuit topologies in Fig. 4.1(b).

4.2.3. Step 3: \textit{“Independent”} variable drawn from LTI input network and \textit{“Dependent”} variable delivered to LTI output network

From Fig. 4.1(b) it looks apparent that average bus current is the \textit{“Dependent variable”} drawn from input voltage source whereas secondary rectifier’s output voltage is the \textit{“Independent variable”} applied to the output filter during CCM operation. On the other hand from Fig. 4.3 it is clear that one cycle-average inductor current becomes the sought \textit{Independent variable} fed to the output section during DCM operation the same as in the ZVS-FB converter.

4.2.4. Step 4: Calculation of one-cycle average for the variables in the previous step

\textbf{CCM}. According to Figs. 4.1(b), 4.2 and 4.4(c) rectifier’s voltage is a function of input, blocking capacitor and output voltages during transfer stage, \textit{i.e.}

\begin{equation}
V_s = \frac{V_{in} + V_{cb} \cdot L_f + V_0 \cdot \frac{L_{ik}}{N^2}}{\frac{L_{ik}}{N^2} + L_f}, \quad (4.23)
\end{equation}

whereas the rest of the switching cycle it becomes zero. From (4.23) and Fig. 4.2 the one cycle average rectifier voltage can be expressed as

\begin{equation}
\bar{V}_s = \frac{\left( V_{in} + V_{cb} \right) \cdot L_f + V_0 \cdot \frac{L_{ik}}{N^2} \cdot D_{bf}}{\frac{L_{ik}}{N^2} + L_f}, \quad (4.24)
\end{equation}
Figure 4.5. Calculation of average blocking capacitor voltage.

\[ m_{cb} \approx \frac{I_L}{N \cdot C_b} \]

\[ V_{cb} = \frac{A_1 - A_2}{D_{trf} \cdot T_s} \]
where $\overline{V_{cb}}$ is the average of blocking capacitor voltage during transfer stage. According to Fig. 4.5 $\overline{V_{cb}}$ is directly proportional to the difference between areas $A2$ and $A1$, i.e.

$$\overline{V_{cb}} = \frac{A2 - A1}{D_{nf} \cdot T_s} = \frac{(A2 + A3) - (A1 + A3)}{D_{nf} \cdot T_s}$$  \hspace{1cm} (4.25.a)$$

$$\overline{V_{cb}} = \frac{(V_{cpk} \cdot D_{nf} \cdot T_s) - \left( \frac{I_L \cdot D_{nf} \cdot T}{2} \right)}{D_{nf} \cdot T_s} = \overline{V_{cpk}} - \frac{I_L \cdot D_{nf} \cdot T_s}{2 \cdot N \cdot C_b}$$  \hspace{1cm} (4.25.b)$$

where the slope of blocking capacitor voltage during transfer stage is approximated by

$$m_{cb} \approx \frac{I_L}{N \cdot C_b}.$$  \hspace{1cm} (4.26)$$

The average circuit model shown in Fig. 4.4(b) includes transformer’s leakage inductance reflected to the secondary side to highlight its dynamic effects, implicitly included in (4.25). As in the ZVS-FB converter case $V_{eq}$ can be computed to make $V_2$ appear in between the two inductors, that is, to have the same average voltage delivered to output filter. Therefore $V_{eq}$ is given by

$$V_{eq} = \frac{V_{in} + \overline{V_{cb}}}{N} \cdot D_{nf} = \frac{V_o \cdot L_{th}}{N^2 \cdot L_f} \cdot (I - D_{nf}).$$  \hspace{1cm} (4.27)$$

Fig. 4.5 indicates that controlled current source $II$ corresponds to one cycle average bus current. From Figs. 4.2, and 4.4(c) $II$ can be computed as

$$II = \overline{I_{bus}} = \frac{I_p^2}{2} \cdot D_{ch} + \frac{(I_p^2 + I_p^3)}{2} \cdot D_{nf}.$$  \hspace{1cm} (4.28)$$

**DCM.** One-cycle average filter inductor current is now given by (4.17). Since this situation is the same as that found both in the buck and ZVS-FB converter models the value $\overline{T_f}$ must be enforced by adjusting, in the average circuit model, controlled source $V_2$, which in turn depends on $D2$. Therefore filter inductor current can be treated the same as in the previous two converter models, i.e. a loop around an operation amplifier that enforces algebraic constraint (4.17).

Calculation of $D_{nf}$ is again carried out on line in the simulator by closing the loop around operational amplifiers to find the root located between 0 and $D_{on}$. Equations (4.1)
through (4.29) can be combined to find an expression with $D_{ref}$ as the only unknown or they can be arranged to solve for as many of unknown quantities as desired.

Bus current, according to (4.15) and Fig. 4.3 is given by

$$I_l = \frac{I_{pk} \cdot D_{ref}}{2 \cdot N} = \frac{m \cdot (D_{ref})^2 \cdot T_s}{2}. \tag{4.29}$$

4.2.5. **Step 5: Calculation of algebraic constraints**

These constraints are already described in (4.1) through (4.22) both for CCM and DCM operation.

4.2.6. **Step 7: Implementation of circuit oriented simulation**

Fig. 4.6 shows the same technique used in the previous two chapters to compute, in real time during the simulation, $D_{ref}$ and $D2$ both in CCM and DCM for the average model.

4.2.7. **Identification and modeling of energy holding elements in fast dynamic subsystems**

An energy holding element is a reactive component that does not appear as a relevant state in the average model and its state variable (voltage for capacitors, current for inductors):

a) gets classified as fast type.

b) has zero moving average in steady state operation and exhibits large components at one half the switching frequency and higher harmonics during transient regime.

c) exhibits relatively large peak-to-peak excursions.

d) exhibits nonzero and relatively large constant value during a significant time interval within a switching cycle.

e) exerts a significant influence upon switching instants and/or “Dependent/Independent” controlled sources’ one-cycle average value.

Since this state variable is the integral of a piece-wise continuous function it is continuous and from (a) and (b) its temporary nonzero constant value depends on the history of that integrand, in general a function of some state variables. Because of (d) this “nonzero constant value” is a critical parameter in the converter constraint equations and its dynamics must be appropriately modeled. Sample data models can very easily and accurately describe these effects whereas high order average continuous models need be used for the same accuracy.
Figure 4.6. Analog computation of $D_{trf}$ and $D_2$. 

$D_{On} - D_{Blk} - D_{Ch} - D_{Trf} = 0$ 

$D_2 \cdot m_2 \cdot T_s - i_{Lpk} = 0$ 

$Z = \begin{bmatrix} D_{On} \\ I_f \\ V_{in} \\ V_C \end{bmatrix}$
Figure 4.7. Analog implementation of dynamic relationship between filter inductor current and blocking-capacitor peak voltage.
Here a heuristic approach is followed to obtain a simple and effective representation of this energy holding element effects. Circuit simulations verify usefulness of this representation.

In our ZVZCS-FB converter blocking capacitor reaches $V_{cpk}$ at the end of resetting stage and holds it constant until the end of blocking stage. Duration of the latter is inversely related to $V_{cpk}$ and hence to the long history of $I_L$ whereas that of charging stage is directly related to $I_L$ in the present switching cycle. As a consequence, an intricate relation among circuit parameters determines whether positive or negative damping is added to the output filter as summarized next and explained in more detail in Appendix C for steady-state operation.

The change in damping is directly related to the loss of duty-cycle,

$$D_{on} - D_{nf} = D_{blk} + D_{ch}, \quad (4.30)$$

and hence inversely related to the change in transfer stage duty ratio. Since duration of the charging stage, i.e. $D_{ch}$, is proportional to $I_L$ the change in duration of blocking stage with respect to $I_L$ has to overcome that in $D_{ch}$ for damping of the output filter to get reduced (intrinsic positive feedback). A low $C_{blk}$ value in the ZVZCS converter, as compared to that in the ZVS converter, leads to a large change in $V_{cpk}$ with $I_L$. This in turn makes the product $V_{cpk} \cdot D_{off} \cdot T_s$ bigger, which produces a reduction in blocking stage duration, since saturable-reactor volt-second blocking capability is constant. The size of that reduction will strongly depend on blocking capacitor value and saturable reactor volt-second blocking capability. Furthermore, it is possible to have an increase in duty-cycle loss for some component values, especially when they resemble those used in the ZVS converter.

Moreover, the amount of damping added to the output filter in the average model is strongly dependent on the type of relationship representation, i.e. algebraic or dynamic, between $V_{cpk}$ and $I_L$ as transient simulation results in Figs. 4.8 through 4.10 show. These results, for parameter value Set I in Table 4, correspond to a switching model, a simplified average model and the proposed average model. The simplified average model uses a standard algebraic equation whereas the proposed average model approximates the relationship between $V_{cpk}$ and $I_L$ as dynamic through a single time constant equal to a switching semi-cycle, $T_s$, as shown in Fig. 4.7, i.e. $I_L$ is modified by a first order low pass filter, whose output is labeled $I_{L,slow}$ in Fig. 4.7, before been used in the computation of $V_{cpk}$ according to (4.9) through (4.11).

Clearly the simulation results in Fig. 4.8 through 4.10 indicate that the proposed average model closely tracks moving average of switching model state variables whereas the simplified model presents poor tracking due to its faster dynamics, i.e. equivalent pole frequency and damping factor higher than actual ones. Only usefulness of the average model with the dynamic constraint will be thoroughly verified through transient simulations for different parameter set values.
Figure 4.8. Filter inductor current (top) and capacitor voltage (bottom) from switching (green), first average (blue) and second average (pink) models for parameter set 1 with zero initial state for all models.
Figure 4.9. Zoom in of filter inductor current and capacitor voltage from switching (green), first average (blue) and second average (pink) models for parameter set 1 with zero initial state for all models.
Figure 4.10. Zoom in of filter inductor current and capacitor voltage from switching (green), first average (blue) and second average (pink) models for parameter set 1 with zero initial state for all models.
4.3. Simulation Results

State variables from the average model with the dynamic constraint very closely follow moving average of their respective counterparts in the switching model for different parameter value sets (Table 4) as Figs. 4.10 through 4.25 show.

\[ \text{Table 4. Parameter set values for transient simulations.} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Set 1</th>
<th>Set 2</th>
<th>Set 3</th>
<th>Set 4</th>
<th>Set 5</th>
<th>Set 6</th>
</tr>
</thead>
<tbody>
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<td>4</td>
<td>4</td>
<td>4</td>
<td>6</td>
<td>4</td>
</tr>
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<td>1 uH</td>
<td>2uH</td>
<td>2uH</td>
<td>2uH</td>
<td>1uH</td>
<td>1uH</td>
</tr>
<tr>
<td>Blocking Capacitor</td>
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<td>0.5uF</td>
<td>0.5uF</td>
<td>0.5uF</td>
<td>1uF</td>
<td>2uF</td>
</tr>
<tr>
<td>Filter Inductance</td>
<td>2uH</td>
<td>8uH</td>
<td>8uH</td>
<td>3uH</td>
<td>2uH</td>
<td>2uH</td>
</tr>
<tr>
<td>Filter Capacitor</td>
<td>200uF</td>
<td>50uF</td>
<td>50uF</td>
<td>33uF</td>
<td>200uF</td>
<td>50uF</td>
</tr>
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<td>Load Resistance</td>
<td>1.1 Ω</td>
<td>1.1 Ω</td>
<td>3 Ω</td>
<td>1.8 Ω</td>
<td>0.3 Ω</td>
<td>1.1 Ω</td>
</tr>
<tr>
<td>Saturable Reactor</td>
<td>60 μV-s</td>
<td>60 μV-s</td>
<td>60 μV-s</td>
<td>60 μV-s</td>
<td>60 μV-s</td>
<td>60 μV-s</td>
</tr>
</tbody>
</table>

4.3.1. Transient simulations for parameter set 1

Simulations results for set 1 are shown in Figs. 4.11 through 4.14. This set of parameters was calculated in a specific application design [20]. The load here was selected to obtain a very lightly damped response with large oscillation amplitude while still maintaining CCM operation since these conditions fully test the CCM model. State variables of the proposed average model almost perfectly match the dynamics, i.e. pole frequency and damping factor, of switching-model state-variable moving average for a time interval over twenty times larger than the oscillation period, which is around 150 μs. The oscillation amplitude of the average filter inductor current over the same interval changes from 15A to 0.2mA, i.e. attenuation of 97dB. It is important to point out that simulation time for the average model is still less than one tenth of that required by the switching model for this type of agreement. The difference in pole oscillation frequency between average model and switching model is around 1% according to the phase difference seen at the end of the simulation interval in Fig. 4.14, i.e. phase shift less than one quarter of a cycle after 20 cycles.
Figure 4.11. Whole transient and zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 1 with zero initial state for both models.
Figure 4.12. Zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 1 with zero initial state for both models.
Figure 4.13. Zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 1 with zero initial state for both models.
Figure 4.14. Zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 1 with zero initial state for both models.
Moving average of filter inductor current was not calculated because of the excellent agreement in output voltage. In other words, the only way for the capacitor voltage in the average model to almost perfectly follow the moving average of the capacitor voltage in the switching model is by receiving the same average filter inductor current since the resistive loads are equal.

4.3.2. Transient simulations for parameter set 2

Simulations results for set 2 are shown in Figs. 4.15 and 4.16. All the parameter values are different from those in set 1 but the load, which remained at 1.1 ohms. Moreover these parameters were selected to produce a less lightly damped response than the previous one with the same pole frequency. Consequently deep CCM operation is seen. Again state variables of the proposed average model very closely match the dynamics, i.e. pole frequency and damping factor, and steady state of switching-model state-variable moving average over the transient interval and the subsequent time respectively. Simulation time for the average model is again less than one tenth of that required by the switching model for this type of agreement. Difference in output-voltage steady-state values between models is less than 1%.

4.3.3. Transient simulations for parameter set 3

Simulations results for set 3 are shown in Figs. 4.17 through 4.19. All the parameter values are the same as those in set 2 but the load, which changed to 3 ohms. Naturally a more lightly damped response than the previous one is obtained but deep CCM operation is still seen. Once again state variables of the proposed average model very closely match the dynamics, i.e. pole frequency and damping factor, and steady state of switching-model state-variable moving average for a time interval over twenty times larger than the oscillation period, which is around 150 $\mu$s. It is important to point out that simulation time for the average model is still less than one tenth of that required by the switching model for this type of agreement. The difference in pole oscillation frequency between average model and switching model is around 1% according to the phase difference seen at the end of the simulation interval in Fig. 4.19, i.e. phase shift less than one quarter of a cycle after 20 cycles.

4.3.4. Transient simulations for parameter set 4

Simulations results for set 4 are shown in Figs. 4.20 and 4.21. Output filter component values and load resistor value are reduced with respect to those in set 3 so that the response is almost critically damped. Similarly to the previous cases average dynamics is very closely matched and simulation time for the average model is still less than one tenth of that required by the switching model for this type of agreement. Output voltage steady state error is again less than 1%.
Figure 4.15. Whole transient filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 2 with zero initial state for both models.
Figure 4.16. Zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 2 with zero initial state for both models.
Figure 4.17. Whole transient of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 3 with zero initial state for both models.
Figure 4.18. Zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 3 with zero initial state for both models.
Figure 4.19. Zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 3 with zero initial state for both models.
Figure 4.20. Whole transient and zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 4 with zero initial state for both models.
Figure 4.21. Zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 4 with zero initial state for both models.
4.3.5. Transient simulations for parameter set 5

Simulations results for set 5 are shown in Figs. 4.22 and 4.23. All the parameter values are the same as in set 1 except for load resistor which gets reduced to 0.3 ohms. The same as for set 1 average dynamics is almost perfectly matched and simulation time for the average model is still less than one tenth of that required by the switching model for this type of agreement.

4.3.6. Transient simulations for parameter set 6

Simulations results for set 5 are shown in Figs. 4.24 and 4.25. Except for leakage and filter inductance values all the parameter values are changed. The same as for set 6 average dynamics is almost perfectly matched and simulation time for the average model is still less than one tenth of that required by the switching model for this type of agreement.

4.4. Dynamics Comparison among Buck, ZVS-FB and ZVZCS-FB Converters

4.4.1. Transient response and small-signal transfer function from new average model and its linearization

Results from linearization and their respective transient simulations, already presented in Chapter 3, are reproduced here in Figs. 4.26 through 4.29 for further analysis.

As already pointed out in Chapter 3 transfer functions in Figs. 4.27 and 4.29 show that the amount of damping added to output filter and of reduction in its pole frequency depends on parameters values and/or operating conditions for both ZVS-FB and ZVZCS-FB converters. With parameter value Set I both soft-switched converters change the damping factor by a fairly large amount albeit in opposite directions. For the other parameter value set the ZVZCS-FB converter exerts a very small reduction in damping whereas the ZVS-FB converter introduces a large increment.

Transient responses in Fig. 4.26 for parameter Set I show that voltage conversion ratio, i.e. output voltage, is larger in the ZVS-FB converter whereas Fig. 4.28 shows the opposite for parameter Set II.

From these observations it looks likely for the ZVZCS-FB converter to add either positive or negative damping to the output filter depending on parameter values and operating conditions as Appendix C explains in more detail.
4.4.2. Small-signal experimental results

Figure 4.30 shows experimental voltage to output transfer function for Buck and ZVZCS-FB converters for parameter value Set I. Peaking for ZVZCS-FB converter is higher than that for the Buck converter as predicted by the small-signal average model. Differences between experimental and simulation results are mostly due to idealization of components, \textit{i.e.} neglect of parasitics, hysteresis and tolerances.
Figure 4.22. Whole transient and zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 5 with zero initial state for both models.
Figure 4.23. Zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 5 with zero initial state for both models.
Figure 4.24. Whole transient and zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 6 with zero initial state for both models.
Figure 4.25. Zoom in of filter inductor current and capacitor voltage from switching (green) and second average (pink) models for parameter set 6 with zero initial state for both models.
Figure 4.26. Capacitor voltage (top) and filter inductor current (bottom) transient response from new average models for Buck (red), ZVS-FB (blue) and ZVZCS-FB (black) converters with parameter set I.
Figure 4.27. Control to capacitor voltage (top) and control to filter inductor current (bottom) transfer functions from new average models for Buck (red), ZVS-FB (blue) and ZVZCS-FB (black) converters with parameter set I.
Figure 4.28. Capacitor voltage (top) and filter inductor current (bottom) transient response from new average models for Buck (red), ZVS-FB (blue) and ZVZCS-FB (black) converters with parameter set II.
Figure 4.29. Control to capacitor voltage (top) and control to filter inductor current (bottom) transfer functions from new average models for Buck (red), ZVS-FB (blue) and ZVZCS-FB (black) converters with parameter set II.
Figure 4.30. Experimental control to capacitor voltage (top) transfer for Buck and ZVZCS-FB converters with parameter set II.
5. MODELING AND MODULATION FOR QSS-ZVZCS THREE-PHASE BUCK RECTIFIER

The new procedure and the average model for the ZVZCS-FB-PWM dc-dc converter from the previous chapter are extended here to develop a counterpart for the Quasi-Single-Stage (QSS) ZVZCS three-phase buck rectifier shown in Fig. 5.1(a). Average steady-state operation occurs over one line voltage cycle, e.g. 60Hz, and hence average along the switching frequency orbit to obtain autonomous average model, as in previous chapters, no longer applies. Nevertheless, the average model still can represent most of the rectifier’s dynamics and can be used for stability analysis.

Assuming that closed-loop bandwidth dynamics is much faster than line frequency allows us to consider the QSS-ZVZCS rectifier as operating in a quasi-steady-state tracking condition. This new average model revealed strong nonlinear relations between applied and effective duty-cycles of standard space vector modulation (SVM). Those nonlinearities are the source of increased input current distortion and output voltage ripple. If these were left to be solely counteracted by the feedback loop, the latter would have to exhibit very large bandwidth, which is already constrained by the switching frequency.

Based on insight provided by the development of the average model, a new modulation scheme together with feed-forward duty-cycle compensation is proposed to effectively minimize output voltage ripple with slight ac current distortion, while allowing use of the same single-loop control strategy. Experimental results verify average model predictions as well as modulation and duty-cycle compensation scheme efficacy.

5.1 Three-Phase Buck Rectifier

Operation of the three-phase PWM buck rectifier, Fig. 5.2(a) is reviewed first to help description of its synchronization with the ZVZCS-FB converter.

According to the nature of the input and output variables (currents and voltages) and the direction of energy flow, three phase converters can be classified as current source or voltage source rectifiers or inverters. The input variables of the buck rectifier are the three phase input voltages and the dc current source. The output variables are the dc link voltage and the three-phase AC input currents. Hence the buck rectifier can be also viewed as a Voltage Source Rectifier. The process of synthesizing the low frequency output variables of the converters could be described as follows [H3, N3]:

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Fig. 5.1. QSS-ZVZCS three-phase rectifier

Buck Rectifier
(SVM)

ZVZCS-FB Converter
(Phase Shifted Modulation)

Fig. 5.1. QSS-ZVZCS three-phase rectifier
a) Simplified three-phase buck rectifier structure

b) Input phase voltage determines $60^0$ electric sectors and the corresponding switch that is always-on throughout the sector

Fig. 5.2. Three-phase buck rectifier and electric sectors.
For a set of input voltages,
\[ v_a = V_m \cos(\omega t + \varphi), \]
\[ v_b = V_m \cos(\omega t - 2\pi/3 + \varphi), \]
\[ v_c = V_m \cos(\omega t - 4\pi/3 + \varphi), \]
\[ (5.1) \]
output current,
\[ i_o = I, \]
\[ (5.2) \]
desired set of input currents,
\[ i_a = I_m \cos(\omega t + \theta), \]
\[ i_b = I_m \cos(\omega t - 2\pi/3 + \theta), \]
\[ i_c = I_m \cos(\omega t - 4\pi/3 + \theta), \]
\[ (5.3) \]
and desired dc link voltage,
\[ V_{out} = V_{pm}, \]
\[ (5.4) \]
determine the control law requirements for the switches of the front-end rectifier.

The six-step modulation of the three-phase PWM buck rectifier is described in the following with reference to Fig. 5.3. Due to voltage sources on the AC side and current sources on the DC side of the rectifier, the converter switches can assume only six allowable combinations that yield non-zero phase currents and three combinations that yield zero phase currents. In space vector representation, the input phase currents are therefore synthesized from 7 discrete current vectors \( I_0 \) to \( I_6 \), also called current switching state vectors (SSVs). The set of SSVs that yield non-zero phase currents form the VSR hexagon as shown in Figure 5.3(a). The parenthesized symbols in the VSR Hexagon represent the switches that are conducting during the synthesis of the respective current vector. The triangular area between two adjacent space vectors is called a sector and it is analog to the sectors in Fig. 5.2 (b). The space vector of the desired phase currents \( i_{\text{ref}} \), called the reference vector, can be synthesized as a time weighted average of the two adjacent non-zero SSVs and an appropriate zero SSV over a switching cycle \( T_s \). Since the operation of the converter within the sectors has circular symmetry, the duty cycles of the three SSVs belonging to a sector that are used for the synthesis of the reference vector over a switching cycle are given by:
\[ d_1 = m \cdot \sin(60^\circ - \theta), \]
\[ d_2 = m \cdot \sin \theta, \]
\[ d_0 = 1 - d_1 - d_2 \]
\[ (5.5) \]
Fig. 5.3. Three-phase buck rectifier with standard SVM

a) SVM hexagon and vector synthesis

b) Normalized duty-cycle variation within electric sector 1

a) Circuit topologies for electric sector 1

**Fig. 5.3. Three-phase buck rectifier with standard SVM**
Fig. 5.4. Three-phase buck rectifier ideal SVM operation

- **Phase Currents**
  - **d1**
  - **d2**

- **Rail Voltage**
  - **V_{bpn}
  - **V_{abc}

- **Ideal phase currents (Amp) and output voltage ripple (Volt)**

- **Normalized duty cycles**

- **Pulsed waveforms**
where \( d_1, d_2 \) and \( \theta_i \) are shown in Figure 5.3(a) and (b) and \( 0 < m < 1 \) is the modulation index. In this standard SVM operation, the same SSV is applied first throughout the sixty-degree sector as indicated in Figs. 5.3(b) and (c). The major advantage of this modulation scheme is smooth moving average of the phase currents and output voltage.

With these duty cycles and fixed \( m \) and the current source value \( I \), the local averages of the phase currents are sinusoidal (5.3), and the average voltage \( V_{pn} \) is dc as desired, Fig. 5.4(a),

\[
V_{pn} = \frac{3}{2} m V_m. \tag{5.6}
\]

The sectors of the VSR hexagon shown in Figure 5.3(a) correspond directly to the \( 60^0 \)-sector within the period of the desired phase currents. The angle \( \theta_i \) in (5.5) and Fig. 5.3(a) and (b) is the angle within the sector, and the duty cycles \( d_1 \) and \( d_2 \) can then be expressed as:

\[
d_1 = m \frac{|i_1|}{I}, \tag{5.7}
\]

\[
d_2 = m \frac{|i_2|}{I},
\]

where \( i_1 \) and \( i_2 \) are the two phase currents that have the same sign within the current \( 60^0 \) segment. It should be noted that SSV duty cycles given by (5.7) are not the duty cycles of the individual switches but of the switching combinations that realize the same. Also the term normalized duty-cycles used in Figs. 5.3, 5.4 and 5.6 denotes duty-cycles with \( m = 1 \).

5.1.1. Three-phase buck rectifier average model

The average circuit model for the three-phase buck rectifier shown in Fig. 5.5 [H3, N3] can also be easily obtained with the procedure given above by starting with the circuit topologies and pulsed waveforms shown in Figs. 5.3 and 5.4. The current source \( I \) is assumed constant during a switching cycle, \( i.e. \) no ripple, and the sector duty-cycles are given by (5.5). The quantities \( d_a, d_b \) and \( d_c \) represent ac phase-current duty-cycles, \( d_a = d_{ap} - d_{an}, \ d_b = d_{bp} - d_{bn}, \ d_c = d_{cp} - d_{cn} \), whereas \( d_{ab}, d_{bc} \) and \( d_{ca} \) correspond to line-voltage duty-cycles, \( d_{ab} = d_{ap} - d_{bp}, \ d_{bc} = d_{bp} - d_{cp}, \ d_{ca} = d_{cp} - d_{ap} \). The former are the individual contributions of \( I \) to \( i_a, i_b \) and \( i_c \) and the latter are the individual contributions of instantaneous \( V_{ab}, V_{bc} \) and \( V_{ca} \) to the rail voltage. Normalized values for phase current and line voltage duty-cycles are represented by the solid traces in Fig. 5.13(a) and (b) respectively for a whole line cycle with SVM operation. Since there is no neutral connection, the sum of the three-phase currents is zero at any time and hence the sum of their duty-cycles must equal zero.
Fig. 5.5. Three-phase buck rectifier average model structure
Fig. 5.6. Three-phase buck rectifier SVM with and without swapping

a) Normalized duty-cycle variation and SSV sequence within electric sector 1 for standard SVM

b) Normalized duty-cycle variation and SSV sequence within electric sector 1 for SVM with swapping
5.1.2. Three-phase buck rectifier with single-loop control

According to (5.5) and (5.7) the modulation index can be varied to control phase currents and rail voltage. When only the modulation index is changed to regulate the output voltage, the control becomes single-loop type, which is the one used in our application. The other parameter that can be changed in the sector duty-cycles, for our control scheme, while still producing sinusoidal phase currents, is the phase shift, \( i.e. \) instead of \( 60^\circ \) and \( 0^\circ \) in (5.5) a feedback dependent angle may be added to the argument in the sine function. This allows control of input displacement factor and turns the control into a two-loop type.

5.1.3. Modified SVM (swapping)

A modified SVM operation, named duty-cycle swapping from here on, and shown in Fig. 5.6, swaps the order of application of the duty-cycles in the middle of the \( 60^\circ \) electric sector so that the larger duty-cycle always appears first in a switching period. Effects of this modulation scheme on the phase currents and output voltage are discussed later in the chapter.

5.2. QSS-ZVZCS Three-Phase Buck Rectifier Operation

5.2.1. Three-phase buck rectifier and ZVZCS-FB converter synchronization

When the three-phase buck rectifier and the ZVZCS-FB converter get directly connected (no energy storage components in between them) to form the QSS rectifier shown in Fig. 5.1, the switching transitions must be carefully synchronized to obtain proper operation of the whole system.

According to Fig. 5.3(c), when non-zero SSVs are selected, the current source \( I \) is connected between two phase-voltages. The ZVZCS-FB converter simulates this current source by connecting reflected filter inductor current, \( I_{Lf} \), to the rails \( p \) and \( n \) when diagonally opposed full-bridge switches get activated, Fig. 5.7(a). For the zero SSVs interval either top or bottom switches in the full-bridge are activated, Fig. 5.7(b). This disconnects the current source from the ac voltages and takes full advantage of ZVZCS-FB converter characteristics [W2], \( e.g. \) reduced conduction losses since fewer switches are connected in series, zero-current switching for some devices in the front-end buck. Furthermore, to produce balanced driving of the transformer duty cycles of switch combinations in the front-end buck rectifier are kept the same for positive and negative primary-side semi-cycles, as shown in Fig. 5.8.

5.2.2. QSS-ZVZCS three-phase buck rectifier operation with standard SVM

Figure 5.8 shows QSS-ZVZCS three-phase rectifier’s typical waveforms when the ZVZCS-FB converter section operates in CCM. These waveforms correspond to Sector 1
Fig. 5.7. Synchronization between three-phase buck rectifier and ZVZCS-FB converter

a) Non-zero phase current vectors

a) Zero phase current vectors
of input phase voltages in Fig. 5.2(b). In this chapter, only a brief description of CCM waveforms relevant to the development of the averaged circuit model and its simplified expressions for use in the duty-cycle compensation scheme are derived.

From Figs. 5.7 and 5.8 it is apparent that only 6 of the 10 switches are active during a 60° sector. The 4 switches of the ZVZCS full-bridge are activated during every sector and their sequence remains unchanged throughout the entire operating duration of the converter. The switching sequence of the devices in the front-end buck rectifier is decided by the respective SSVs that have to be made active to synthesize the reference current vector.

5.2.3. Topological stages and analytical description

Figure 5.8 describes the CCM operation of the converter through equivalent circuit structure for each switch configuration interval as well as waveforms for bus and bridge voltage, \(V_{pm}\) and \(V_{ab}\), primary current, \(I_p\), bus current, \(I_{bus}\), blocking capacitor voltage, \(v_{cb}\), filter inductor current, \(I_f\) and, output and secondary rectifier’s voltage, \(V_0\) and \(V_s\).

Assume the switching cycle starts with the blocking stage at \(t_0\) (beginning of \(d_1\)) when bridge voltage \(V_{xy}\) becomes positive and the saturable reactor blocks any primary current, and ends at \(t_1\) when the reactor gets saturated. The sum of input line voltage \(V_{ab}\) (for Sector 1 in Fig. 5.2) and blocking capacitor voltage determines the rate of change of the flux in the saturable reactor. The change of flux is

\[
\Delta \phi_{blk} = (t_1 - t_0) \cdot \left( \frac{V_{line1} + V_{cpk}}{N_{sr}} \right) = (D_{blk} \cdot T_s) \cdot \left( \frac{V_{line2} + V_{cpk}}{N_{sr}} \right), \tag{5.8}
\]

where \(D_{blk}, N_{sr}\) and \(V_{cpk}\) are the blocking stage duty-ratio, saturable reactor number of turns and peak blocking capacitor voltage. On the secondary side, the rectifier output voltage determines the rate of change in the filter inductor current.

During charging stage, \((t_1, t_2)\), the same rate of change applies to filter inductor current, whereas the change in primary current, after neglecting transformer’s magnetizing current,

\[
I^p_2 = \left( \frac{V_{line1} + V_{cpk}}{L_{lk}} \right) (t_2 - t_1) = (mI) \cdot (D_{ch} \cdot T_s), \tag{5.9}
\]

where slope \(mI\), shown in Fig. 5.8(a), is defined by the first bracket, \(D_{ch}\) corresponds to the charging stage duty ratio and the remaining quantities are defined in Fig. 5.8(a).
a) Typical waveforms in CCM Case 1

b) Switch structures in CCM Case 1

Fig. 5.8. QSS-ZVZCS rectifier typical waveforms and switch structures
At time instant $t_2$, primary current and filter inductor current are related by transformer’s turns ratio, i.e.

$$I^f_2 = I^p_2 \cdot N,$$  \hspace{1cm} (5.10)

and they remain so through transfer stage 1. The latter ends at $t_3$ with first commanded duty-cycle $d_1$, when the buck rectifier selects line voltage $V_{ac}$, for sector 1 in Fig. 5.2(b) i.e.

$$d_1 \cdot T_x = (t_3 - t_0) = (D_{blk} + D_{ch} + D_{uf1}) \cdot T_x.$$  \hspace{1cm} (5.11)

Reflection of input line voltage and transformer leakage inductance to the secondary side leads to the equivalent circuits shown in Fig. 5.1(b) for this transfer stage. Change in the filter inductor current, after neglecting blocking capacitor effects, is approximately given by

$$I^f_3 - I^f_2 = \left( \frac{V_{line1}}{N} - V_0 \right) \cdot \left( t_3 - t_2 \right) = (N \cdot m2) \cdot \left( D_{uf1} \cdot T_x^f \right),$$  \hspace{1cm} (5.12)

where slope $N \cdot m2$ is defined by the first bracket and the other terms by Fig. 5.8.

Duration of transfer stage 2 is directly second commanded duty-cycle $d_2$ and the change in the filter inductor current is given by

$$I^f_4 - I^f_3 = \left( \frac{V_{line2}}{N} - V_0 \right) \cdot \left( t_4 - t_3 \right) = (N \cdot m3) \cdot \left( d_2 \cdot T_x^f \right),$$  \hspace{1cm} (5.13)

where slope $N \cdot m3$ is defined by the first bracket and the other terms by Fig. 5.8(a).

Resetting stage starts at $t_4$, when bridge voltage $V_{xy}$ becomes zero and it ends when primary current does the same at $t_5$. Duration of this stage is given by

$$t_5 - t_4 = D_{res} \cdot T_x = \frac{1}{\sqrt{L_{lk} \cdot C_{blk}}} \cdot \arcsin \left( \frac{I^p_4}{V_{cpk}} \cdot \sqrt{\frac{L_{lk}}{C_{blk}}} \right).$$  \hspace{1cm} (5.14)

Off stage begins at $t_5$ when saturable reactor blocks any primary current by taking $V_{cpk}$ as its flux rate of change and it ends at $(t_0 + T_x)$ the with primary switching semicycle when $V_{xy}$ becomes negative as shown in Fig. 5.8(a).
Fig. 5.9. QSS-ZVZCS PWM rectifier average model structure
During this stage the change in flux across the saturable reactor is given by

\[ \Delta \phi_{\text{eff}} = \frac{V_{c_{pk}} \cdot (I - d_i - d_2 - D_{res}) \cdot T_s}{N_{sr}}, \]  \hspace{1cm} (5.15) \]

which together with saturable reactor volt-second blocking capability determines blocking stage duration, i.e.

\[ \Delta \phi_{\text{blk}} = 2 \cdot \phi_{\text{sat}} - \Delta \phi_{\text{eff}}, \] \hspace{1cm} (5.16) \]

where \( \Delta \phi_{\text{blk}} \) is given by (5.8).

Expressions for peak blocking capacitor voltage, \( V_{c_{pk}} \), and average filter inductor current \( I_L \), are calculated next to complete the set of equations and the same approximation to calculate \( V_{c_{pk}} \) value followed in Chapter 4 is used here. That is, looking at converter’s steady-state operation and taking into consideration relevance of stage’s duration upon change in capacitor voltage. These voltage changes during transfer and resetting stages are respectively given by

\[ \Delta V_{c_{-\text{trf}}} = \frac{I_L \cdot (D_{ trif1} + d_2) \cdot T_s}{N \cdot C_{blk}} \] \hspace{1cm} (5.17) \]

and

\[ \Delta V_{c_{-\text{res}}} = \frac{(I^f_4)^2 \cdot L_{ik}}{N \cdot I_L \cdot (D_{ trif1} + d_2) \cdot T_s}, \] \hspace{1cm} (5.18) \]

From Fig. 5.8, after neglecting the voltage change during charging stage, \( V_{c_{pk}} \) is given by

\[ V_{c_{pk}} = \frac{\Delta V_{c_{-\text{trf}}} + \Delta V_{c_{-\text{res}}}}{2}. \] \hspace{1cm} (5.19) \]

On the other hand, \( I_L \) is calculated as

\[ I_L = \frac{1}{2} \left[ D_{ trif1} \cdot (I^f_5 + I^f_2) + d_2 \cdot (I^f_4 + I^f_3) + (I - D_{ trif1} - d_2) \cdot (I^f_5 + I^f_4) \right], \] \hspace{1cm} (5.20) \]

where

\[ (I^f_5 - I^f_4) = \left\{ \frac{V_0}{L_f} \cdot (I - D_{ trif1} - d_2) \right\} \cdot T_s = m4 \cdot (I - D_{ trif1} - d_2) \cdot T_s, \] \hspace{1cm} (5.21) \]

with slope \( m4 \) defined by the term in the first bracket and Fig. 5.8(a).
Fig. 5.10. Calculation of average blocking capacitor voltage.

\[
\bar{V}_{cb} = \frac{A_1 - A_2}{(D_{trf1} + D_2) T_S}
\]
5.3. New Average Circuit Model for the QSS-ZVZCS Rectifier

An input-output structure for the average model of the QSS-ZVZCS rectifier is shown in Fig. 5.9. This structure has been obtained by following the new procedure as in Chapter 4 and in Section 5.1.1 together with the assumption of quasi-steady state operation. The starting point is the circuit topologies and pulsed waveforms shown in Fig. 5.8. A detailed derivation is presented below.

5.3.1. Step 1: Fast/slow classification of state variables

Figures 5.8 indicates that filter inductor current and output capacitor voltage should be considered slow variables in CCM and used as states in the average circuit model, similarly to Chapter 4.

Once again, the primary current is discarded as a relevant average state variable because its moving average is zero in steady state operation and exhibits large components at one half the switching frequency and higher harmonics during transient regime.

The blocking capacitor voltage waveform in Fig. 5.8 indicates that it must be classified as a fast variable that belongs to an energy holding element. Its treatment here is the same as is the previous chapter, i.e. its effect on peak blocking capacitor voltage is modified by a time constant.

5.3.2. Step 2: LTI input/output parts

Output filter and three-phase input phase voltage sources get selected as LTI networks according to circuit topologies in Fig. 5.8(b).

5.3.3. Step 3: “Independent” variable drawn from LTI input network and “Dependent” variable delivered to LTI output network

From Figs. 5.1 and 5.8 it looks apparent that average phase currents are the “dependent variables” drawn from the three-phase voltage sources, whereas secondary rectifier’s output voltage is the “independent variable” applied to the output filter during CCM operation.

5.3.4. Step 4: Calculation of one-cycle average for the variables in the previous step

For the average model in Fig. 5.9 the quantities $\hat{d}_a$, $\hat{d}_b$ and $\hat{d}_c$ represent ac phase-current duty-cycles or equivalent primary duty-cycles as defined in Fig. 5.12, whereas $\tilde{d}_{ab}$, $\tilde{d}_{bc}$ and $\tilde{d}_{ca}$ correspond to line-voltage duty-cycles or equivalent secondary duty-cycles as defined in Fig. 5.12. The former are the individual contributions of reflected filter inductor current to $i_a$, $i_b$ and $i_c$ and the latter are the individual contributions of reflected instantaneous $V_{ab}$, $V_{bc}$ and $V_{ca}$ to the secondary rectifier voltage.
Fig. 5.11. QSS-ZVZCS rectifier desired and experimental waveforms with typical SVM operation

a) Waveforms for ideal buck and experimental ZVZCS rectifiers

b) Applied and effective duty-cycles for ZVZCS rectifier
a) Case 1

b) Case 2

b) Case 3

Fig. 5.12. QSS-ZVZCS rectifier equivalent primary and secondary duty-cycles cases with typical SVM operation
Normalized values for phase current and line voltage duty-cycles are represented by the dashed traces in Fig. 5.13(a) and (b) respectively for a whole line cycle with SVM operation.

Figure 5.12 shows three different cases for equivalent primary and secondary duty-cycles cases based upon duty-cycle loss. In Case 1, Fig. 5.12(a), the loss of duty-cycle occurs only in the first duty-cycle both in primary and secondary side, e.g. when the first commanded duty-cycle has a large value, i.e. at the beginning of the sixty-degree electrical sector. In Case 2, the loss of duty cycle occurs in both first and second duty-cycles, Fig. 5.12(b), e.g. near the end of the electrical sector. Moreover, the first secondary duty-cycle becomes zero and stays the same for Case 3 when first primary duty-cycle also becomes zero as shown in Figs. 5.12(c) and 5.13.

One-cycle average calculation of the controlled sources is derived next for Case 1 in Fig. 5.12. Modified equations for the other cases are given in Appendix D.

According to Fig. 5.8, the secondary rectifier voltage is a function of blocking capacitor voltage $V_{cb}$, output and line voltages during transfer stages 1 and 2, i.e.

$$V_{s1} = \frac{V_{line1} + V_{cb}}{N} \cdot L_f + \frac{V_0 \cdot L_{lk}}{N^2} \cdot \frac{L_{lk}}{N^2} + L_f$$

and

$$V_{s2} = \frac{V_{line2} + V_{cb}}{N} \cdot L_f + \frac{V_0 \cdot L_{lk}}{N^2} \cdot \frac{L_{lk}}{N^2}$$

where $V_{line1}$ and $V_{line2}$ are the line voltages applied during duty-cycles $d_1$ and $d_2$ respectively to the full-bridge by the front-end buck rectifier. Secondary rectifier voltage is zero during the rest of the switching semi-cycle. From (5.22), (5.23) and Fig. 5.8 the one-cycle average rectifier voltage can be expressed as

$$\bar{V}_s = \frac{(V_{line1} \cdot D_{ref1} + V_{line2} \cdot D_2) \cdot L_f + \left( V_0 \cdot \frac{L_{lk}}{N^2} + V_{cb} \cdot \frac{L_f}{N} \right) \cdot (D_{ref1} + D_2)}{N \cdot \frac{L_{lk}}{N^2} + L_f}$$

(5.24)
where $V_{cb}$ is the average of blocking capacitor voltage during transfer stages. $V_{cb}$ is, according to Fig. 5.10, directly proportional to the difference between areas $A2$ and $A1$, i.e.

$$
V_{cb} = V_{cpk} - \frac{I_L \cdot (D_{trf1} + D_2) \cdot T_s}{2 \cdot N \cdot C_{blk}}.
$$

(5.25)

Figures 5.4, 5.8, 5.11 and 5.12 indicate that each controlled current source corresponds to one-cycle average phase current and that average first and second phase currents $I_{phase1}$ and $I_{phase2}$ can be computed as

$$
I_{phase1} = \frac{I_p}{2} \cdot D_{ch} + \frac{(I_{3p} + I_{4p})}{2} \cdot D_{trf1}
$$

and

$$
I_{phase2} = \frac{(I_{3p} + I_{4p})}{2} \cdot d_2.
$$

(5.26)

(5.27)

In the simulations, the calculation of $D_{trf1}$ is again carried out on-line in the simulator by closing the loop around operational amplifiers to find the root located between 0 and $d_1$. Equations (5.1) through (5.27) can be combined to find an expression with $D_{trf1}$ as the only unknown or they can be arranged to solve for as many of unknown quantities as desired.

5.3.5. **Step 5: Calculation of algebraic constraints**

These constraints have been already described in Section 5.2.2 by (5.1) through (5.14) for Case 1 in Fig. 5.12. Modified equations for the other cases are given in Appendix D.

5.3.6. **Step 7: Implementation of circuit oriented simulation**

The same analog techniques used in the previous three chapters can applied here to compute $D_{trf1}$ in real time during the simulation. The small differences arise in the number of equations and boundary conditions for the different cases in Fig. 5.12.

5.3.7. **Modeling of energy holding elements in fast dynamic subsystems**

The same heuristic approach followed in Chapter 4 for the dynamic relation between average filter inductor current and peak blocking capacitor voltage is used here for large signal transient simulations. However, the analysis is instead oriented towards identification of ac input current distortion and output voltage ripple origins, as well as their correction.
Fig. 5.13. Three-phase buck rectifier (solid) and QSS-ZVZCS rectifier simulated effective (dashed) primary and secondary duty-cycles for whole line cycle with SVM

a) Primary

b) Secondary
Effective duty cycle 1

Effective duty cycle 2

\[ d_{1\text{-desired}} \]

\[ d_{2\text{-desired}} \]

\[ d_{1\text{-eff}} \]

\[ d_{1\text{-compens}} \]

\[ d_2 \]

\[ d_1 \]

\[ \theta_i \]

\[ \text{Comp} \]

\[ v_C \]

a) Simulation: 60 degree sector

b) Experimental: 1 line cycle

Fig. 5.14. Normalized QSS-ZVZCS rectifier simulated and experimental duty-cycles, compensation with SVM and phase voltage
5.4. Distortion Analysis

Ideally, the duty-cycles applied to two switches of the front-end buck rectifier, $d_1$ and $d_2$, are sinusoidal as shown in Figs. 5.3 and 5.4 whereas the switch corresponding to the largest absolute phase voltage stays on for a $60^\circ$ electric sector (Figs. 5.1, 5.3, 5.7 and 5.8). When pulsed phase currents and rail voltage are as in Fig. 5.4(c) their ideal moving average values look like those in Fig. 5.4(b). Unfortunately, QSS-ZVZCS rectifier typical pulsed waveforms, Fig. 5.8, for the same sinusoidal duty-cycles exhibit strong differences from those in Fig. 5.4(c), which leads to the highly distorted filtered experimental phase currents and large output voltage ripple in Fig. 5.11(a) and 5.15(a). These differences, detailed in Fig. 5.11(b), are mainly caused by the loss of duty-cycle that affects effective primary and secondary duty-cycles $d_{1-pri}$ and $d_{1-sec}$ in Fig. 5.12. As explained in Section 5.2.4 they are the equivalent contribution of filter inductor current and input line voltages to input phase current and secondary rectifier voltage respectively. As the value for duty-cycle $d_1$ approaches zero at the end of the $60^\circ$ sector, QSS-ZVZCS rectifier pulsed waveforms suffer further changes as depicted in Fig. 5.12 and labeled Cases 2 and 3. In the average circuit model shown in Fig. 5.9 $d_{1-pri}$ and $d_{1-sec}$ are replaced by equivalent phase current duty-cycles (with caret) and equivalent secondary rectifier duty-cycles (with tilde).

These nonlinear relations between commanded and effective primary and secondary duty-cycles are illustrated in Fig. 5.13 for a full line cycle. Clearly the largest perturbations in effective duty-cycles occur in the vicinity of the electric sector border.

5.5. Hardware implementation

Figure 5.16 shows control block diagram for the prototype whereas Fig. 5.17 presents power stage circuit diagram. Details for the former with standard SVM are presented next.

The operation of the switches of the converter has to be synchronized with the three phase input AC voltages. The present $60^\circ$ sector in the input line cycle is determined according to the polarity of the input phase and line voltages. This sector information is coded into a six bit control word ($S_{i0}$-$S_{i5}$), where the lower three bits ($S_{i0}$-$S_{i2}$) represent the polarities of the line voltages $V_{ab}$ through $V_{ca}$, and the upper three bits ($S_{i3}$-$S_{i5}$) represent the polarities of the phase voltages $V_a$ through $V_c$. The SSVs to be applied to synthesize the reference current vector are determined from the control word. The modulation index $m$, is supplied to the digital control algorithm from the error amplifier network that implements the output voltage and inductor current loops. The sinusoidal functions required for the determination of the duty cycles in Fig. 5.4 can be obtained either from the input phase voltages by reading them through A/D converters or from pre-stored look-up tables with the table read-out synchronized with the input phase voltages. The latter approach is followed here in that the duty cycles are synchronously derived from the look up tables to reduce number of A/D conversions. The synchronization process is explained in detail in a later section. The duty cycles along
with the control word is then sent to the decoder logic, which distributes the switching pulses to the respective switches with the appropriate duty cycles.

5.5.1. Implementation of digital controller

The block diagram of the controller hardware shown in Figure 4.16 indicates that the digital controller is built around the ADSP-2101, a 16-bit fixed point digital signal processor from Analog Devices Inc. The control board houses an 8-channel 8-bit A/D converter, a 4-channel 8-bit D/A converter, an address decoder and an EPLD (Electrically programmable Logic Device) from Altera Inc. The EPLD consists of the decoder logic that derives the switching waveforms based on the sector information in the control word. The controller uses two A/D converter channels to sample the voltage at phase $a$ and a square wave at 6 times the line frequency containing the zero cross information of all the three phase voltages. This square wave is used to synchronize the six-step modulation with the input phase voltages. The synchronization process is presented in a later section. A third A/D converter channel is used to sample the modulation index $m$ from the output voltage and inductor current feedback loops. 2 PWM signals $A$ and $B$, as determined from the duty cycles read from the look-up tables, a synchronization signal $S_1$ and the control word are required for the generation of the switching waveforms for the devices. These are supplied to the decoder logic built into the EPLD to determine the appropriate switches to be turned on or off with their respective duty cycles. The signals from the decoder are then fed to a digital interface board that incorporates the required turn-on and turn-off delays for the individual switches before they are sent to the gate drive circuits.

5.5.2. Implementation of decoder logic

The decoder logic that generates the switching signals for all the switches of the converter is implemented using an Electrically Programmable Logic Device (EPLD) from Altera Inc. The decoder consists of an array of double buffered counters that are used to generate the main PWM signals $A$ and $B$. It also consists of a sampling clock generated by dividing the system clock. The sampling clock is also used to generate the interrupt to the DSP to enable sampling the analog inputs at regular intervals. In addition, the decoder contains the combinatorial logic blocks implemented to determine the switching instants of the switches of the ZVZCS bridge and of the front-end buck rectifier from the control word generated from the signs of the input phase and line voltages. The turn-on and turn-off delays for the switches are not implemented inside the EPLD. A dedicated digital interface board is used to implement these delays. The EPLD used is the Altera EPM-5192, which has 192 macrocells. The architecture of the decoder logic is optimized such that the EPLD can be operated at a maximum system clock frequency of 21.73MHz. This frequency limits the switching frequency of the converter depending on the bit resolution used in the counters for producing the PWM signals. With a counter frequency of 20MHz and a bit resolution of 8 bits the switching frequency $f_s$ can be derived to be equal to 78kHz. This is the switching frequency at which the converter is operated.
Fig. 5.15. QSS-ZVZCS rectifier open-loop experimental phase voltage and currents and output voltage ripple with SVM, before and after compensation for 360V peak line voltage, 48V output voltage and 40A load current.
Fig. 5.16. Control block diagram.
5.6. Software Implementation

The controller software implemented in the ADSP-2101 from Analog Devices generates the sinusoidal duty cycle functions that are synchronized with the input phase voltages. The six-bit control word that identifies the current 60° sector that the converter is operating in, is determined by the software program. The controller software reads in the modulation index \( m \), from the external feedback controller and multiplies it with the sinusoidal duty cycles that are read from pre-stored look up tables. Duty cycle compensation in order to compensate for the loss of duty cycle due to the ZVZCS operation is also implemented in the program. General purpose functions such as soft-start operation and watch-dog timer are incorporated. The details of the controller software are presented in the following sections.

5.6.1. Synchronization with input voltages

The synchronization of the operation of the converter with the input phase voltages is essential in the determination of the six-bit control word that contains the present 60° sector information. Knowledge of the current 60° sector is critical in determining the switches that are to be modulated to synthesize the reference vector. In addition, the duty cycles that are to be read out of the look-up tables need to be synchronized with the three phase voltages since they repeat every 60°. The 60° sector information is derived from the input phase voltages as follows:

A phase locked loop is used to derive a square wave, whose frequency is six times the line frequency and is synchronized with the zero-cross of each of the input phase voltages, and to feed it to the digital controller through one of the channels of the A/D converter. The synchronization algorithm has to obtain a measure of the average duration of \( 1/6^{th} \) of the line frequency cycle. In other words, if the look-up table consists of \( N \) entries, the algorithm must read the values from the table at appropriate intervals such that the pointer to the table is at its last value or its immediate neighborhood by the end of the current 60° sector. The algorithm must hence measure the time interval between two successive zero-crossing instants of the synchronizing signal. The time interval thus measured will then be used in the subsequent 60° sector to determine the spacing between the successive values read out from the table. The synchronization algorithm implemented in software requires the zero crossing information of one of the phase voltages and the signal and the square wave at six times the line frequency to determine the duty cycles and the six-bit control word.

5.7. Compensation Scheme for Standard SVM

A natural procedure to reduce phase current distortion and output voltage ripple would be to compensate for the duty-cycle loss by pre-distorting \( d_i \). For this task a simplified set of equations was developed (see [C22, C23] and Appendix D) and solved for \( d_i \), i.e. compensated duty-cycle expressed in terms of desired duty-cycle \( d_{pri} \) among others. The final result is

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Fig. 5.17. QSS-ZVZCS rectifier power stage for 208-380V line voltage, 48V output voltage, 6 kW output power and 40 kHz switching frequency
Fig. 5.18. QSS-ZVZCS rectifier closed-loop experimental phase voltage and currents and output voltage ripple with SVM, before and after compensation for 360V peak line voltage, 48V output voltage and 40A load current.
Simulation results in Fig. 5.14(a) indicate that once the duty-cycle compensation is incorporated second duty-cycle loss for \( d_2 \) does not occur, i.e. \textit{Cases 2 and 3} in Fig. 5.12 disappear. Since \((5.28)\) is a very involved relation that requires extra variable sensing and big computational cost for direct implementation a power series approximation with coefficient look-up tables is used instead. As a first cut compensation approach, the dependence on the line voltage is only taken into account and compensated for.

The loss of duty-cycle is mainly inversely proportional to the input line voltage that corresponds to the first commanded duty-cycle. Moreover, this voltage is a cosine signal from 0 to 60°. The inverse relationship between the duty-cycle loss and the line voltage results in the duty-cycle compensation to be an appropriately scaled secant function from 0 to 60°. Since the loss of duty cycle is dependent on the filter inductor current in addition to the input voltage, a power series of the angle into the sector is implemented in the software.

Figure 5.14(b) shows experimental waveforms for new duty-cycles, phase voltage and compensation function. The latter exhibits a discontinuity at the sixty-degree sector border, which invariably creates problems over wide operating ranges. Power-series coefficients for the compensation can be tuned to reduce the effects of that discontinuity in a narrow operating range without incurring excessive computational and storage costs. Fig. 5.15(b) shows open-loop experimental phase currents and output voltage ripple waveforms for the QSS-ZVZCS rectifier with SVM and duty-cycle compensation. The latter strongly reduces phase current distortion but only causes moderate improvements in output voltage ripple. The major difficulties for arriving at an optimal experimental compensation that minimizes output voltage ripple (the most critical parameter in this application) are large changes in both first applied line voltage (from its peak to half of it) and first desired duty-cycle (normalized values from \( \sqrt{3}/2 \) to zero), and the effect of the latter: the already mentioned above large discontinuity in the compensation itself.

Closed-loop experimental phase current and output voltage ripple waveforms without and with duty-cycle compensation are shown in Fig. 5.17(a) and 5.17(b) respectively. Fig. 5.16(a) clearly indicates that loop bandwidth of the single input control strategy, which already includes optimized current and voltage loop compensators, cannot remove much of the current distortion and voltage ripple created by duty-cycle loss, i.e. difference between applied and effective duty-cycles. On the other hand 5.17(b)
Fig. 5.19. QSS-ZVZCS rectifier simulated and experimental duty-cycles and compensation with modified (duty-cycle order swapping) SVM
Fig. 5.20. QSS-ZVZCS rectifier phase currents and secondary rectifier voltage at swapping border (phase voltage crossing) with modified SVM
indicates that duty-cycle compensation together with the selected control can remove a lot of current distortion and voltage ripple. Unfortunately this output voltage ripple is not acceptable for high performance applications such those in telecommunications.

5.8. Compensation Scheme for Modified SVM

Since the main causes of output voltage ripple are:

i) Discontinuity in the compensation function at sixty-degree sector crossing due to change in first applied duty-cycle.

ii) Simultaneous requirement of near zero effective values and relatively large applied compensated values for first duty-cycle at the end of the sixty-degree sector.

A simple way to avoid the latter problem is to swap the order of commanded duty-cycles somewhere inside the sixty-degree sector. Note that selecting the duty-cycle order-swapping instant when both phase voltages cross each other can solve the first problem. Selection of that swapping instant causes the same required duty-cycle compensation value, which mainly depends on first input line voltage during a short interval of time, to be used in the switching cycles right before and after the duty-cycle swapping. As a result the compensation function becomes continuous. All of this can be seen in Fig. 5.19(a) where simulated duty-cycles are shown and in Fig. 5.19(b) where experimental compensation functions with and without swapping are displayed.

Effects of this new scheme are analyzed with the help of Fig. 5.20, which shows simplified pulsed phase-current and secondary rectifier voltage waveforms before and after the swapping border. Even though the two desired duty-cycles could be different from each other when their corresponding phase voltages cross the loss of duty-cycle seen before and after the swapping border remains constant. Since both applied line voltages have the same value an unperturbed moving average of secondary rectifier voltage, represented by the sum of the areas of the two trapezoids, is produced across the swapping boundary despite the difference in individual phase contribution.

However the two corresponding phase currents will exhibit a strong perturbation in their moving average if no duty-cycle compensation is introduced together with swapping in duty-cycle order as Fig. 5.20 shows. Therein duty-cycle loss occurs in phase-current $b$ before the swapping and it ceases after the swapping whereas phase-current $c$ experiences the opposite change. In addition, phase-current pulse positions are altered across the swapping border. This combined effect is illustrated by open-loop experimental waveforms in Fig. 5.21(a).
Fig. 5.21. QSS-ZVZCS rectifier open-loop experimental output voltage ripple, phase current and voltage with modified SVM, before and after compensation for 360V line voltage, 48V output voltage and 40A load current.
Fig. 5.22. QSS-ZVZCS rectifier closed-loop experimental output voltage ripple, phase current and voltage with modified SVM after compensation for 360V line voltage, 48V output voltage and 40A load current.
The latter also shows that large output voltage ripple appears when the swapping takes place at very dissimilar phase voltage values. It should be noticed that even with an excellent compensation function value moving averages of corresponding phase currents experience a slight perturbation across the swap border due to alteration in current pulse position as can be observed in the open-loop experimental waveforms shown in Fig. 5.21(b).

Closed-loop experimental phase current and output voltage ripple are shown in Fig. 5.22. The big reduction in output voltage ripple is clear and better than that in Fig. 5.18(b) for standard SVM with compensation. However the trade-off in phase current distortion is noticeable when looking at Figs. 5.22 and 5.18(b).

5.9. Compatibility of Modified SVM and Compensation Scheme with Single Input Control Strategy

The control block diagram of Fig. 5.16 indicates PLL synchronization and analog circuitry implementation of output voltage and filter inductor current regulators together with single input control to minimize number of sampled state variables (analog to digital conversions) and hence to reduce implementation costs as well as program execution time.

Experimental output voltage and phase current waveforms during transient responses to step changes in resistive load are shown in Fig. 5.22 and 5.23. These waveforms exhibit low distortion after the fast transient interval time, which verifies compatibility of both new modified SVM and duty-cycle compensation with the single input control strategy. These transient results show that the current loop has settling time lower than three milliseconds whereas the voltage loop presents a settling time around six milliseconds.
Fig. 5.23. QSS-ZVZCS rectifier closed-loop response to step load disturbance (1.6 Ohm load switched in) with swapping and compensated duty cycles for 380V peak line voltage, 48V output voltage and 1.1 Ohm initial load.
Fig. 5.24. QSS-ZVZCS rectifier closed-loop response to step load disturbance (1.0 Ohm load switched in) with swapping and compensated duty cycles for 380V peak line voltage, 48V output voltage and 1.1 Ohm initial load
6. CONCLUSIONS

This dissertation presents a new systematic procedure to develop circuit oriented, continuous, large signal, average models for PWM converters and some applications of these models.

The modeling procedure is introduced in Chapter 2 and initially applied to the open loop buck converter to illustrate its usage in both CCM and DCM operation. Modifications of model equations to include close loop constraints are then discussed, which allow utilization of most of the open loop model.

The primary goals of this procedure are: a) to obtain input-output structured models that represent input and output impedance and/or loading characteristics as well as transfer characteristics, b) to produce circuit oriented models that provide physical insight and that can be easily used with circuit simulators and hence that take advantage of the tools available in those simulators to perform a complete analysis within the same simulation environment; c) to provide enough modeling versatility to include as much internal description of the converter as needed as well as to allow for detail and accuracy adjustments in the constraint equations according to the type and level of analysis. Despite the emphasis on averaged circuit models simple application of Kirchoff’s laws to these models provides a set of equations that can be used with any mathematical simulator for ordinary differential equation.

In Chapter 3 the new procedure is applied to the well-known ZVS-FB PWM converter. It is shown that low order Taylor’s series approximation of the constraint equations are enough to produce a large-signal average model that smoothly transitions between CCM and DCM operation and that very closely matches the moving average of the state-variables from the switching model. These characteristics were not seen in previous models for this converter. In addition a small-signal model is derived through linearization of the large signal counterpart and it correctly represents the intrinsic negative feedback effects extensively discussed in the literature.
The only reported average model for the saturable reactor based ZVZCS-FB PWM converter was also derived through the new procedure and it is presented in Chapter 4. The average model exhibits excellent matching of the dynamics shown by the moving average of switching-model state-variables, \textit{i.e.} pole frequency and damping factor, for various set of components values that lead to different types of transient responses, \textit{i.e.} under, critically and over-damped. This excellent matching is achieved by the simple and accurate heuristic approach of modeling the effects caused by an energy holding element through a dynamic constraint, which is also a new result. The physical insight provide by the model clearly explains the interaction between the saturable reactor and the blocking capacitor, \textit{i.e.} the energy holding component, that creates the positive feedback effects solely seen in this ZVZCS-FB converter and that were first reported together with the model.

Versatility and usefulness of the new modeling procedure are shown in Chapter 5 by applying it to a QSS, soft-switched three-phase buck rectifier based on the ZVZCS-FB converter in the previous chapter. This average model, the only one reported for this rectifier, revealed the cause of nonlinear transfer characteristics, \textit{i.e.} applied duty-cycles to output-variables relationship, for standard SVM operation, that induced strong distortion both in average input phase currents and average rectifier output voltage. This variable distortion prevented usage of this rectifier, with standard SVM operation, in the intended telecommunications applications since the feedback loop is not able by itself to counteract those nonlinearities. Physical insight provided by the average model lead to the development of a combined feedforward duty-cycle compensation and modified SVM scheme that very effectively and reliably reduces distortion both in input phase currents and output voltage. Moreover the new scheme is fully compatible with the inexpensive but simple and effective single loop control needed in this commercial application. Circuit simulations and experimental results verified model predictions for this rectifier with and without duty cycle compensation for SVM and the new modified SVM and for open loop and closed loop operation. All the experimental and analytical results presented in this work for the QSS three-phase buck rectifier are new findings.
# 7. REFERENCES

*Sorted by first author’s last name.*

**A**


**B**


C


D


E


**F**


**G**


**H**


I


J


K


M


N


O


P


NEW PROGRAM, DIFFERENT DOMAIN


R


S


KBM method for ripple calculation PWM only.


T


V


X


Y


A Saber Template and Schematics for Buck Converter

A1. Listing of Saber Template for Buck Converter Average Model

```plaintext
element template buck_duo_1 com ilf vout vin d1 d2 i_equiv v_equiv zeros = 
Ts,Lf

electrical com, ilf, vout, vin, d1, d2, i_equiv, v_equiv, zeros

number Ts, Lf

{ 
val v delta_ilf, ipk, d_off, vilf, vvout, vvin, vd1, vd2,
  v_vequiv, v_iequiv, v_zeros, vdeltaup, vdeltaupm 

var i i_iequi, i_vequi, i_zeros

values {
  vilf = v(ilf)-v(com)
  vvout = v(vout)-v(com)
  vvin = v(vin)-v(com)
  vd1 = v(d1)-v(com)
  vd2 = v(d2)-v(com)
  d_off = 1 - vd1
  vdeltaup = vd1*(vvin-vvout)*Ts/Lf
  vdeltaupm = vvout*d_off*Ts/Lf

  delta_ilf = (vdeltaup*vd1 + vdeltaupm*d_off)/2

  if (vilf - delta_ilf > 0 ) {
    ipk = vilf + delta_ilf
  } else {
    if ( vdeltaup - vdeltaupm > 0 ) {
      ipk = vilf + delta_ilf
    } else {
      ipk = 2*vilf/(vd1+vd2+1e-7)
    }
  }

  v_vequiv = vvin*vd1/(vd1+vd2+1e-7)
  v_iequiv = vilf*vd1/(vd1+vd2+1e-7)
  v_zeros = Ts*vd2*vvout - ipk*Lf

} # end of values section

equations {
  i(zeros->com) += i_zeros
  i_zeros : v(zeros) - v(com) = v_zeros
  i(i_equiv->com) += i_iequiv
```

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\[ i_{\text{iequi}} : v(i_{\text{equiv}}) - v(\text{com}) = v_{\text{iequiv}} \]

\[ i(v_{\text{equiv}} \rightarrow \text{com}) += i_{\text{vequi}} \]

\[ i_{\text{vequi}} : v(v_{\text{equiv}}) - v(\text{com}) = v_{\text{vequiv}} \]

} # end of equations section

} # end of template body
Fig. A.1. Saber schematics for Buck converter
B Listing of Saber templates for ZVS-FB PWM Converter
Average Models

B1. Previous Model

element template zvs_duo_PREVIOUS com ilf vout vin Don Dtrf D2 i_equiv v_equiv i_deviat zero_Dtrf zero_D2 = Ts, Lf, Llk, N

electrical com, ilf, vout, vin, Don, Dtrf, D2, i_equiv, v_equiv, i_deviat, zero_Dtrf, zero_D2

number Ts, Lf, Llk, N

{
val v delta_ilf, ipk, d_off, vilf, vvout, vvin, vDon, vDtrf, vDoff, VDch, vD2, v_vequiv, v_iequiv, v_ideviat, vzero_D2, v_zero_Dtrf, vdeltaup, vdeltaup, Lequiv, NTS
var i i_iequi, i_vequi, i_ienuat, i_zero_D2, i_zero_Dtrf
values {

vilf = v(ilf)-v(com)
vvout = v(vout)-v(com)
vin = v(cin)-v(com)
vDon = v(Don)-v(com)
vDtrf = v(Dtrf)-v(com)
vD2 = v(D2)-v(com)
Lequiv = Lf + Llk/N**2
vDoff = 1 - vDtrf
NTS = N*Ts
vdeltaup = vDtrf*(vvin/N-vvout)*Ts/Lequiv
delta_ilf = vdeltaup/2

if (vilf - delta_ilf/2 > 0) {

   ipk = vilf + delta_ilf

}
vDch = (Vilf)*2*Llk/vvin/NTS
}
else {

ipk = 2*vilf/(vDtrf+vD2+1e-7)
VDch = 0
}

v_ideviat = vDch*(vilf)
v_vequiv = vvin*vDtrf/(vDtrf+vD2+1e-7)/N
v_iequiv = vilf*vDtrf/(vDtrf+vD2+1e-7)/N
v_zero_D2 = Ts*vD2*vvout - ipk*Lf
v_zero_Dtrf = - vDon + vDch + vDtrf

}  # end of values section

equations {

i(zero_D2->com) += i_zero_D2
i_zero_D2 : v(zero_D2) - v(com) = v_zero_D2

i(zero_Dtrf->com) += i_zero_Dtrf
i_zero_Dtrf : V(zero_Dtrf) - v(com) = v_zero_Dtrf

i(i_equiv->com) += i_iequi
i_iequi : v(i_equiv) - v(com) = v_iequiv

i(i_deviat->com) += i_idевiat
i_idевiat : v(i_deviat) - v(com) = v_idевiat

i(v_equiv->com) += i_vequi
i_vequi : v(v_equiv) - v(com) = v_vequi

}  # end of equations section

}  # end of template body
B2. New Model

element template zvs_duo_2_rev2_4a com ilf vout vin Don Dtrf D2 i_equiv v_equiv i_deviat zero_Dtrf zero_D2 I1out I3out = Ts, Lf, Llk, N

electrical com, ilf, vout, vin, Don, Dtrf, D2, i_equiv, v_equiv, i_deviat, zero_Dtrf, zero_D2, I1out, I3out

number Ts, Lf, Llk, N

{
val v delta_ilf, deltap, deltadwn, ipk, d_off, vilf, vvout, vvin, vDon, vDch, vDtrf, vDoff, vD2,vDtrf1, AA, BB, CC,
    v_vequiv, v_iequiv, v_i_deviat, v_zero_D2,
    v_zero_Dtrf, m1, m2,m3, m4, IX, IY, IZ, IW, Lequiv, NTS

var i i_i_equiv, i_vequi, i_i_deviat, i_zero_D2, i_zero_Dtrf, i_I1out, i_I3out

values {
vilf  =  v(ilf)-v(com)
vvout =  v(vout)-v(com)
vvin  =  v(vin)-v(com)
vDon  =  v(Don)-v(com)
vDtrf =  v(Dtrf)-v(com)
vD2   =  v(D2)-v(com)

Lequiv = Lf + Llk/N**2

NTS    =  N*Ts

m1  = (vvin/N-vvout)/Lequiv
m2  = vvout/Lequiv
m3  = vvout/Lf
m4  = vvin*N/Llk

if ( vD2 >= 0 & vD2 <= 1-vDon ) {
    NTS    =  N*Ts
}
else {
    if ( vD2 <= 0 ) {
        vD2 = 0

199
else {
    vD2 = 1-vDon
}

if ( vilf > m1*vDtrf*Ts/2 | m1*vDtrf > m2*(1-vDon) ) {

    AA = -(m3+m1)
    BB = m4-vDoff*(2*m1-m3)+m3*vDon
    CC = vDoff*(m2*vDoff+m3*vDon)-m4*vDon+2*vilf/Ts

    v_zero_Dtrf = -AA*vDtrf**2 - BB*vDtrf - CC

    vDoff = 1 - vDon
    vDch = vDon - vDtrf

    IY = (m4-m3)*vDch*TS/2
    IX = IY + m1*vDtrf*TS
    IW = IX - m2*vDoff*TS
    IZ = IY + m3*vDch*TS

    v_vequiv = vvin*vDtrf/N
    v_iequiv = ((-IZ+IY)*vDch/2+(IY+IX)*vDtrf/2)/N
    v_ideviat = (IY+IY)*vDch/2
    v_zero_D2 = TS*vD2*m2 - IX
}

else {
    v_zero_D2 = TS*vD2*m2*(vDtrf+vD2)-2*vilf
    v_iequiv = vilf*vDtrf/(vDtrf+vD2+1e-10)/N
    v_ideviat =0

    v_vequiv = vvin*vDon/(vDon+vD2+1e-10)/N
}

} # end of values section
equations {
    i(zero_D2->com) += i_zero_D2
i_zero_D2 : v(zero_D2) - v(com) = v_zero_D2

    i(zero_Dtrf->com) += i_zero_Dtrf
i_zero_Dtrf : V(zero_Dtrf) - v(com) = v_zero_Dtrf

    i(i_equiv->com) += i_iequi
i_iequi : v(i_equiv) - v(com) = v_iequiv

    i(i_deviat->com) += i_ideviat
i_ideviat : v(i_deviat) - v(com) = v_ideviat

    i(v_equiv->com) += i_vequi
i_vequi : v(v_equiv) - v(com) = v_vequiv

    i(I1out->com) += i_I1out
i_I1out : v(I1out) - v(com) = IX

    i(I3out->com) += i_I3out
i_I3out : v(I3out) - v(com) = IY

    } # end of equations section

} # end of template body
C Analysis and Design Procedure of Saturable Reactor-Based Zero-Voltage Zero-Current Switched, Full-Bridge PWM Converter and Saber Template for its Average Model

C1. Introduction

This appendix presents general design procedure for the high power, high performance ZVZCS-FB-PWM converter.

Verification of design procedure is performed through both numerical solution of exact steady-state nonlinear equations and experimental implementation of a practical design example. The latter corresponds to a specific application: 10 kW, three-module, dc-dc system operating at 100 kHz.

C2. Review of Steady State Operation

Fig. C1 shows major topological stages for steady state operation of the ZVZCS converter, i.e. Blocking, Charging, Transfer, Resetting and Off, whose characteristics are summarized below.

**Blocking Stage.** Starts at $t_0$ when $V_{in}$ is applied between nodes $a$ and $b$, and ends at $t_1$ when the saturable reactor stops blocking any current. On the primary side, the sum of input voltage and the blocking capacitor voltage determines the rate of change of flux in the saturable reactor, while on the secondary side, the output voltage (assumed constant throughout the appendix) determines rate of change of current through the filter inductor, $L_f$.

**Charging Stage.** Starts at $t_1$ when current begins to flow on primary side and ends at $t_2$ when primary current equals reflected filter inductor current. Secondary side conditions remain the same as in the previous stage.

**Transfer Stage.** Starts at $t_2$ after primary current equals reflected filter inductor current with transformer in normal operation, and ends at $t_3$ when $V_{ab}$ becomes zero.

**Resetting Stage.** Starts at $t_3$ when $V_{ab}$ becomes zero and ends at $t_4$ when primary current becomes zero. Once again primary and secondary side are independent from one another.

**Off stage.** Starts at $t_4$ when primary current becomes zero and saturable reactor takes all blocking capacitor voltage as its flux rate of change, and ends at $T_s$ when $V_{ab}$ becomes $-V_{in}$. 


Fig. C1. ZVZCS converter and typical waveforms.
For each stage, nonlinear equations relating initial and final values of the state variables can be written. In order to form a complete set of equations two additional equations are required: one including output power and one describing filter inductor current ripple. This set, fully described in *Equation Set I*, will prove very useful later in this work for development and verification of the dc model.

### C3. Design Procedure

Having high closed-loop bandwidth as a major requirement forces the switching frequency to be very high. Since the ZVZCS topology is of forward type, its small-signal loop-gain bandwidth can be expected up to one fifth of effective switching frequency. In multi-module systems with interleaving the effective switching frequency is equal to the product of the number of parallel modules and the frequency of each module.

After switching frequency selection, converter voltage and current levels will determine the choice of semiconductor devices. Voltage stress for diodes on the secondary side will mainly depend on transformer turns ratio and rectifier configuration (center tap or full-bridge), as well as voltage ringing. The latter is due to diode reverse recovery characteristics and its interaction with parasitics and snubbers.

In the following design procedure it is assumed that the line and load ranges are known quantities and that the filter inductor current ripple and output voltage ripple are specified.

Design of the ZVZCS converter involves complex interactions between device characteristics, circuit parameters, and operating conditions. Therefore, the design has to start from several assumptions or estimates which are then iteratively corrected as the design proceeds. Let us first define duty-cycles of different operating stages in Fig. C1 as:

\[
\begin{align*}
\text{apparent:} & \quad D = \frac{t_j}{T_s}, \quad \text{(C.1)} \\
\text{blocking:} & \quad D_{bk} = \frac{t_l - t_g}{T_s}, \quad \text{(C.2)} \\
\text{charging:} & \quad D_{ch} = \frac{t_3 - t_i}{T_s}, \quad \text{(C.3)} \\
\text{transfer:} & \quad D_{trf} = \frac{t_3 - t_2}{T_s}, \quad \text{(C.4)} \\
\text{resetting:} & \quad D_{rs} = \frac{t_4 - t_3}{T_s}, \quad \text{(C.5)} \\
\text{off:} & \quad D_{off} = \frac{T_s - t_4}{T_s}. \quad \text{(C.6)}
\end{align*}
\]
Although the primary circuit is operated with apparent duty-cycle, $D$, the secondary duty-cycle, $D_{trf}$, is smaller by the loss of duty-cycle, $D_{bk}+D_{ch}$. During transfer stage, the secondary rectifier output voltage is equal $(V_{in}-V_{ch})/N$. Since the average value of the blocking capacitor voltage is approximately zero during this time interval, the output voltage is very closely given by

$$V_o = \frac{V_{in} \cdot D_{trf}}{N}.$$  \hfill (C.7)

The main design parameters are: transformer turns ratio, $N$, blocking capacitor value, $C_{blk}$, and saturable inductor blocking capability. The first major assumption in the design will be that it is desirable to have $N$ as large as possible in order to minimize the voltage rating of the secondary diodes as well as primary current peak value. Therefore it is desirable to use maximum possible value of the transfer duty-cycle, $D_{trfx}$. A reasonable assumption for the first iteration could be

$$D_{trfx}=0.8,$$  \hfill (C.8)

which leaves 10% for the minimum off duty-cycle, $D_{offx}$, in order to provide sufficient control authority during transients, and 10% for the sum of $D_{bk}+D_{ch}+D_{rs}$.

Second assumption that has to be made is the desired value of the peak blocking-capacitor voltage $V_{c(pk)}$. Small values of $V_{c(pk)}$ will increase the reset time (transformer leakage inductance is reset only by $V_{c(pk)}$) which will increase the primary current rms value and limit maximum value of $D_{trf}$. Large values of $V_{c(pk)}$ will increase secondary diode voltage rating, $(V_{in}+V_{c(pk)})/N$, and decrease the duration of the charging stage which will aggravate the secondary diode reverse recovery problems. Empirically determined reasonable choice was found to be

$$V_{c(pk)} \leq 0.2 \cdot V_{in}.$$  \hfill (C.9)

With assumptions (C.8) and (C.9) the first iteration of the design can be initiated. The transformer turns ratio can be found from as

$$N = \frac{V_{in_{\min}}}{V_o} \cdot D_{trfx}.$$  \hfill (C.10)

Knowing $N$, $D_{trfx}$, $V_o$, $I_{f}$, and switching frequency provides sufficient information for the transformer design. Once the transformer is designed, its leakage inductance, $L_{lk}$, can be estimated or measured. The transformer should be designed with minimum leakage in order to increase the frequency of the ringing in the secondary caused by the diode reverse recovery, so that it can be more easily suppressed with snubbers.
Blocking capacitor, \( C_{blk} \), is therefore estimated at low line and full load conditions [C11] by

\[
\begin{align*}
C_{blk} = & \frac{I_{if\ max} \cdot D_{gfk} \cdot T_s}{2 \cdot N \cdot V_{cpk}}.
\end{align*}
\]

(C.11)

ZCS operation in steady state requires volt-second blocking capability of saturable reactor to be greater than the product \( T_s \cdot V_{cpk} \cdot D_{off} \) at high line and full load conditions. Thus, the saturation flux of \( L_s \) should be

\[
\phi_{sat} > \frac{D_{off\ max} \cdot T_s \cdot V_{cpk}}{2 \cdot N_{sr}}.
\]

(C.12)

where \( N_{sr} \) is the number of turns in \( L_s \). However, ZCS operation during current limiting situations demands higher volt-second values from the saturable reactor since the product \( T_s \cdot V_{cpk} \cdot D_{off} \) becomes much larger than that in (C.12). Furthermore, should saturable reactor allow oscillation between \( L_{lk} \) and \( C_{blk} \) during off stage chaotic operation can occur and lead to transformer saturation. Therefore, a safe value for the saturation flux of \( L_s \) could be chosen as

\[
\phi_{sat} = \frac{T_s \cdot V_{cpk}}{2 \cdot N_{sr}}.
\]

(C.13)

At this moment the design should be checked against the original assumptions.

During the resetting stage, the primary current reduces with the slope of \( V_{cpk}/L_{lk} \), so that

\[
\begin{align*}
D_{rs} &= \frac{\left(I_{if} + \Delta I_f\right) \cdot L_{lk}}{N \cdot T_s \cdot V_{cpk}},
\end{align*}
\]

where \( \Delta I_f \) is the filter inductor current ripple specification.

During charging stage, the primary current increases with the slope of \( (V_{in} + V_{cpk})/L_{lk} \), and hence

\[
\begin{align*}
D_{ch} &= \frac{\left(I_{if} - \Delta I_f\right) \cdot L_{lk}}{N \cdot T_s \cdot \left(V_{in} + V_{cpk}\right)}.
\end{align*}
\]

(C.15)

During off time the primary current is kept at zero by the saturable inductor \( L_s \) with the voltage across it equal to \( V_{cpk} \). In the following blocking stage, the voltage across \( L_s \) increases to \( V_{in} + V_{cpk} \) so that the blocking stage duty-cycle can be found as
\[ D_{blk} = \frac{I}{V_{in} + V_{cpk}} \left( \frac{2 \cdot \phi_{sat}}{N_{sr} \cdot T_{s}} - D_{off} \cdot V_{cpk} \right) \]  \hspace{1cm} (C.16)

where it is assumed that

\[ D_{off} = 0.1. \]  \hspace{1cm} (C.17)

Now, the assumption (A.8) can be verified against

\[ D_{off} = 1 - D_{rs} - D_{ch} - D_{off} - D_{blk}. \]  \hspace{1cm} (C.18)

Additionally, in order to assure minimum turn-on loss in the lagging leg, i.e. complete zero-current turn-off, duration of off stage must be longer than the switch turn-off time [C11]. A reasonable assumption could be

\[ D_{rs} = 1.5 \cdot \frac{T_{off} + T_{tail}}{T_{s}}, \]  \hspace{1cm} (C.19)

where \( T_{off} \) and \( T_{tail} \) are IGBT parameters for full load, and \( T_{tail} \approx 0 \) for MOSFETs.

If there is only small discrepancy between the assumptions (C.8) and (C.19) and the results (C.18) and (C.14), it usually can be easily adjusted by changing the values of \( C_{blk} \) and \( V_{cpk} \). However, large differences may require changes in the transformer design (\( N \) and \( L_{lk} \)), and even change of the switching frequency or selection of active devices.

The design of the output filter is quite straightforward. \( L_f \) is normally determined by current ripple specifications unless very strong output impedance and large signal requirements make it irrelevant. Considering the first one, \( L_f \) must satisfy

\[ L_f \geq \frac{V_o \cdot (1 - D_{offs})}{2 \cdot \Delta L_{offs}} - \frac{L_{ik}}{N^2}. \]  \hspace{1cm} (C.20)

Filter capacitor is normally calculated from voltage ripple requirements but stringent output impedance specifications might override them. Assuming the former as determining factor, its value is given by

\[ C_f = \frac{\Delta V_o \cdot T_s}{2 \cdot m^2 \cdot \Delta V_o}. \]  \hspace{1cm} (C.21)
where $\Delta V_o$ is peak to peak output voltage ripple and $m_{\text{module}}$ is the number of paralleled interleaved modules.

It is worth noting that if the output voltage were to vary over a wide range, additional conditions, listed in Table C1, will have to be considered in the design procedure.

### Table C1. CONDITIONS FOR PARAMETER SELECTION

<table>
<thead>
<tr>
<th>Transformer Turns Ratio</th>
<th>Line Output Voltage</th>
<th>Output Current</th>
</tr>
</thead>
</table>
| Low                     | High                | Max
| High                    | Low                 | Max

Example: The ZVZCS converter shown in Fig. C1 is designed for the following specifications

$$V_{in} = 280 - 480 \text{V}, \quad V_o = 33 \text{V}, \quad P_o = 3.3 \text{kW},$$
$$\Delta I_f \leq 30 \text{A}, \quad \Delta V_o \leq 20 \text{mV}, \quad f_s = 100 \text{kHz}$$

Using the design procedure given above, following components are selected:

$$N = 6, \quad L_{lk} = 1 \mu \text{H}, \quad C_{blk} = 1 \mu \text{F},$$
$$\phi_{\text{sat}} \cdot N_{sv} = 60 \mu \text{N} - \text{s}, \quad L_f = 2 \mu \text{H}, \quad C_f = 200 \mu \text{F}.$$

### C3. DC Analysis

As stated above, dc voltage conversion ratio for the ZVZCS converter is almost entirely determined by transformer turns ratio and transfer duty-cycle. This is verified by calculating the voltage conversion ratio, for the converter parameters in the above example, using the exact nonlinear steady-state equations given in *Equation Set I*. As can
be seen from Fig. C2, the ratio is practically independent from input voltage and output power levels. It is interesting to note that this is true even though the blocking-capacitor peak voltage and peak primary current vary considerably with input voltage and output power, as shown in Fig. C3. The same figure also compares the results obtained by using approximate equations in *Equation Set III* with those obtained from exact non-linear equations in *Equation Set I*. As can be seen, at least for the numerical values from the example, there is very small disagreement between the two sets.

Therefore, the dc model is the same as buck converter model except that the switch duty-cycle (named here apparent duty-cycle, \(D\)) is replaced with the *transfer* duty-cycle, as shown in Fig. C4. Using simplified equations, it is derived in *Equation Set II* that the *transfer* duty-cycle is given by

\[
D_{trf} = \frac{D \cdot V_{in} \cdot T_s - 2 \cdot \phi_{sat} \cdot N_{sr} - \frac{2 \cdot L_{lk} \cdot I_{if}}{N}}{V_{in} \cdot T_s - \frac{(1-D) \cdot T_s^2}{2 \cdot N \cdot C_{blk}} \cdot I_{if}} \tag{C.22}
\]

It follows from (C.24) that the presence of \(L_s\), \(L_{lk}\), and \(C_{blk}\), introduces feedforward from \(V_{in}\) and feedback from \(I_{lf}\) into the open-loop model of the ZVZCS converter, similarly as in the ZVS-FB converter [V5].

However, unlike in the ZVS, the inductor current feedback in the ZVZCS converters can be positive. From (C.22) if

\[
\sqrt{(1-D) \left( D - \frac{2 \cdot \phi_{sat} \cdot N_{sr}}{V_{in} \cdot T_s} \right)} > \frac{\sqrt{L_{lk} \cdot C_{blk}}}{T_s} \tag{C.23}
\]

the *transfer* duty-cycle increases with the inductor current, resulting in positive feedback. Since \(L_{lk}\) and \(C_{blk}\) are much smaller in ZVZCS than in ZVS converters, condition (C.23) is satisfied in most cases. It is also important to note that (C.23) is a conservative condition due to the approximations used in the estimate for \(V_{cpk}\), and described in *Equation Set II*.

The above phenomenon can be further explored by analyzing the loss of duty-cycle,

\[
D - D_{trf} = D_{blk} + D_{ch}, \tag{C.24}
\]

for the ZVZCS converter. Fig. C5 shows dependence of the *blocking* and *charging* duty-cycles on the output power, i.e. average filter inductor current. Even though increase in duration of the *charging stage* takes place as expected and confirmed by Fig. C5, use of a lower \(C_{blk}\) value in the ZVZCS converter, as compared to that in the ZVS converter, allows a strong rise in \(V_{cpk}\) with \(P_o\) to take place, as it is clearly seen in Fig. C3. This in
turn makes the product $V_{\text{pk}} \cdot D_{\text{off}} \cdot T_s$ larger, which leads to a reduction in blocking stage duration, since saturable-reactor volt-second blocking capability is constant. At the end, this reduction counteracts for the increase in charging stage duration and produces the reduction in duty-cycle loss. The size of that reduction will strongly depend on blocking capacitor value and saturable reactor volt-second blocking capability. Furthermore, it is possible to have increase in duty-cycle loss for some component values, especially when they resemble those used in the ZVS converter.

C4. Experimental Results

Design values from the example were used to build a 10 kW, three-module, dc-dc power converter operating at 100 kHz with current sharing and interleaving.

With three modules working in parallel, the experimental primary current waveforms for low line and 40% load, and high line and 60% load conditions, are shown in Fig. C6 where excellent current sharing is clearly observed. This is achieved through simple and fast current injection control together with very good repeatability of transformer characteristics provided by printed-circuit-board-type windings. This control also provides the damping required to achieve as large closed-loop bandwidth as possible [R4].

Fig. C7 shows Bode plots of voltage loop-gain transfer function for the three-module power system operating at 60% load and $V_{in}=350$ V, where crossover frequency is about 25 kHz. Each module has its own local current loop and their reference is provided by a common voltage loop.

The most severe problem in the converter operation is reverse recovery of the secondary diodes, as can be clearly seen in Fig. C6. Since the leakage inductance is so small, the slope of the rectifier current reversal during charging stage is very steep. Therefore, rectifier snubber design and its layout are extremely important when dealing with reverse recovery effects at high currents. Fig. C8 shows voltage waveforms across one of the rectifiers for two different snubber layouts, $V_{in}=400$ V, and 100 A load. The big improvement in peak reduction comes from having the snubber placed right on top of rectifier which minimizes parasitics in the snubber itself. Even though this made duration of transfer stage in the primary side look longer, its duration on the secondary side followed predictions very closely.
Fig. A2. Voltage conversion ratio.

Fig. C3. Blocking-capacitor peak voltage, peak primary current for exact (solid) and approximate (dotted) equations.
Fig. C4. Dc model for ZVZCS converter.

Fig. C5. Duty-cycles of blocking and charging stages for exact (solid) and approximate (dotted) equations.
Fig. C6. Experimental primary currents from 3-module dc-dc power system with interleaving.

(a) Low line, 40% load  
(b) High line, 60% load

Fig. C7. Voltage loop-gain for the 3-module dc-dc power system at Vin=350 V and 6 kW resistive load.
Fig. C8. Voltage across rectifier for same snubber values but different layouts, at $V_{in}=400$ V and 100 A load.
C5. Nomenclature

\( V_{in}, V_o \): input and output voltages
\( I_f \): average output (filter inductor) current
\( P_o \): output power
\( L_{lk}, L_f \): primary leakage and filter inductors
\( D_{blk}, D_{ch}, D_{trf}, D_{rs}, D_{off} \): average value for blocking, charging, transfer, resetting and off duty-cycles.
\( D \): average apparent duty-cycle
\( V_{cb1}, V_{cb2}, V_{cb3}, V_{cb4} \): blocking-capacitor voltage at \( t_1, t_2, t_3 \), and \( t_4 \) in Fig. 1, respectively
\( I_{p2}, I_{p3} \): primary current at \( t_2 \) and \( t_3 \) in Fig. 1, respectively
\( V_{cpk} \): estimate of blocking-capacitor peak voltage
\( \phi_{sat} \): saturation flux of saturable inductor
\( \Delta \phi_{off} \): change of flux in saturable reactor during off stage.
\( \Delta \phi_{blk} \): change of flux in saturable reactor during blocking stage
\( N_{sr} \): turns in saturable reactor
\( N \): primary to secondary turns ration
\( f_s \): switching frequency
\( T_s \): switching period
\( L_{lk} \): primary leakage inductance
\( C_{blk} \): blocking capacitor
\( Z_1, \omega_1 \): characteristic impedance and resonant frequency during charging and resetting stages.
\( Z_2, \omega_2 \): characteristic impedance and resonant frequency during transfer stage

C6. Equation Set I

Steady-State Boundary Equations for Topological Stages

Blocking Stage:

\[
\Delta \phi_{blk} = \frac{D_{blk} \cdot T_s \cdot (V_{in} + V_{cb1})}{N_{sr}} \quad (CI-1)
\]

Charging Stage:

\[
I_{p2} = \frac{V_{in} \cdot V_{cb1}}{Z_1} \cdot \sin(\omega_1 \cdot D_{ch} \cdot T_s) \quad (Ci-2)
\]
\[
V_{cb2} = (V_{cb1} + V_{in}) \cdot \cos(\omega_1 \cdot D_{ch} \cdot T_s) - V_{in} \quad (CI-3)
\]
\[
Z_1 = \sqrt{L_{lk} / C_{blk}} \quad (CI-4)
\]
\[
\omega_1 = 1 / \sqrt{L_{lk} \cdot C_{blk}} \quad (CI-5)
\]
Transfer Stage:

\[ I_{p3} = I_{p2} \cdot \cos(\omega_2 \cdot D_{of} \cdot T_s) \]
\[ + \frac{V_m - N \cdot V_o + V_{cb2}}{Z_2} \cdot \sin(\omega_2 \cdot D_{of} \cdot T_s) \]  
\[ (CI-6) \]

\[ V_{cb3} = (V_{cb2} + V_m - N \cdot V_o) \cdot \cos(\omega_2 \cdot D_{bf} \cdot T_s) \]
\[ - (V_m - N \cdot V_o - I_{p2} \cdot Z_2 \cdot \sin(\omega_2 \cdot D_{bf} \cdot T_s)) \]  
\[ (CI-7) \]

\[ Z_2 = \left( \frac{4}{3} \cdot L_{lk} + N^2 \cdot L_f \right) / C_{blk} \]  
\[ (CI-8) \]

\[ \omega_2 = 1 / \sqrt{\left( \frac{4}{3} \cdot L_{lk} + N^2 \cdot L_f \right) \cdot C_{blk}} \]  
\[ (CI-9) \]

(It is assumed that secondary leakage inductance reflected to the primary is half of \( L_{lk} \).)

Resetting Stage:

\[ \frac{V_{cb1}}{Z_1} \cdot \sin(\omega_1 \cdot D_{rs} \cdot T_s) = I_{rk3} \cdot \cos(\omega_{in} \cdot D_{rs} \cdot T_s) \]  
\[ (CI-10) \]

\[ V_{cb4} = -V_{cb1} = V_{cb3} \cdot \cos(\omega_1 \cdot D_{rs} \cdot T_s) \]
\[ - I_{rk3} \cdot Z_1 \cdot \sin(\omega_1 \cdot D_{rs} \cdot T_s) \]  
\[ (CI-11) \]

Off Stage:

\[ \Delta \phi_{off} = \frac{V_{cb1} \cdot D_{off} \cdot T_s}{N_{sr}} \]  
\[ (CI-12) \]

Filter Inductor Current Ripple:

\[ \frac{V_o \cdot (1 - D_{off}) \cdot T_s}{L_f + \frac{L_{lk}}{N^2}} = (I_{p3} - I_{p2}) \cdot N \]  
\[ (CI-13) \]
Output Power:

\[
\frac{P_o}{V_o} = N \left[ I_{p1} \cdot \left( 1 - D_{trf} \right) + \frac{I_{p2} \cdot \sin(\omega_2 \cdot D_{off} \cdot T_s)}{\omega_2 \cdot T_s} \right] + \frac{V_o \left( 1 - D_{off} \right)^2}{2 \cdot L_f} + \frac{N \cdot \left( V_{in} - N \cdot V_o + V_{cb2} \right) \cdot \left[ 1 - \cos \left( \omega_2 \cdot D_{trf} \cdot T_s \right) \right]}{Z_2 \cdot \omega_2 \cdot T_s}
\]  

(CI-14)

Saturable Reactor Total Flux Change:

\[2 \cdot \phi_{sat} = \Delta \phi_{off} + \Delta \phi_{blk}\]  

(CI-15)

C7. Equation Set II

Average \( D_{trf} \) in Steady-State

Simplified equations for computation of average \( D_{trf} \) in terms of \( D \) after neglecting inductor current ripple, \( V_{cpk} \) with respect to \( Vin \), and contributions of charging and resetting stages to \( V_{cpk} \).

\[ D_{off} = 1 - \left( D + D_{rs} \right) \]  

(CII-1)

\[ D = D_{blk} + D_{ch} + D_{trf} \]  

(CII-2)

\[ 2 \cdot \phi_{sat} = \frac{\left( D_{off} \cdot V_{cpk} + D_{blk} \cdot V_{in} \right) \cdot T_s}{N_{sr}} \]  

(CII-3)

\[ D_{ch} = \frac{L_{ik} \cdot I_{lf}}{N \cdot V_{in} \cdot T_s} \]  

(CII-4)

\[ D_{rs} = \frac{L_{ik} \cdot I_{lf}}{N \cdot V_{cpk} \cdot T_s} \]  

(CII-5)

\[ V_{cpk} = \frac{I_{lf} \cdot D_{nfx} \cdot T_s}{2 \cdot N \cdot C_{blk}} \]  

(CII-6)
Solving (CII-1)-(CII-6) gives

\[
D_{trf} = \frac{D \cdot V_{in} \cdot T_s - 2 \cdot \phi_{sat} \cdot N_{sr} - \frac{2 \cdot L_{lk}}{N} \cdot I_{if}}{V_{in} \cdot T_s - \frac{(1 - D) \cdot T_s^2}{2 \cdot N \cdot C_{blk}} \cdot I_{if}} \quad \text{(CII-7)}
\]

C8. Equation Set III

Approximate Steady-State Equations

\[
2 \cdot \phi_{sat} = \left[ D_{off} \cdot V_{cpk} + D_{blk} \cdot \left( V_{in} + V_{cpk} \right) \right] \cdot T_s \quad \text{(CIII-1)}
\]

\[
D_{ch} = \frac{L_{lk} \cdot \left( I_{if} - \Delta I_{if} \right)}{N \cdot \left( V_{in} + V_{cpk} \right) \cdot T_s} \quad \text{(CIII-2)}
\]

\[
D_{rs} = \frac{L_{lk} \cdot \left( I_{if} + \Delta I_{if} \right)}{N \cdot V_{cpk} \cdot T_s} \quad \text{(CIII-3)}
\]

\[
D_{trf} = \frac{V_o \cdot N}{V_i} \quad \text{(CIII-4)}
\]

\[
\Delta I_{if} = \frac{V_{in} \cdot \left( 1 - D_{trf} \right) \cdot D_{trf} \cdot T_s}{N \cdot \left( L + \frac{L_{lk}}{N^2} \right)} \quad \text{(CIII-5)}
\]

\[
P_o = V_o \cdot I_{if} \quad \text{(CIII-6)}
\]
C9. Listing of Saber templates for New Model of ZVZCS-FB PWM Converter

C9.1 Template 1.

This template calculates charging and resetting duty-cycles, average controlled-voltage source, peak blocking-capacitor voltage and flux constraint equation.

element template dchrsdeviaveffcpkzero com In1 In2 In3 In4 In5 In6 In7 in8 Out1 Out2 Out3 Out4 Out5 Out6 = Ts, Lf, Llk, Cblk, N, phi_sat
electrical com, In1, In2, In3, In4, In5, In6, In7, In8, Out1, Out2, Out3, Out4, Out5, Out6

number Ts, Lf, Llk, Cblk, N, phi_sat

{ val v v1, v2, v3, v4, v5, v6, v7, v8, ilf, Dtrf, Doff, Dblk, ipk, ivall, delta_ilf, vin, vcpk, Lequiv, Zo, Wo, Dch, Drs, Idevia, veff, zero_satu, v_out1, v_out2, v_out3, v_out4, v_out5, v_out6
var i i_Out1, i_Out2, i_Out3, i_Out4, i_Out5, i_Out6

values {
  v1 = v(In1)-v(com)
  v2 = v(In2)-v(com)
  v3 = v(In3)-v(com)
  v4 = v(In4)-v(com)
  v5 = v(In5)-v(com)
  v6 = v(In6)-v(com)
  v7 = v(In7)-v(com)
  v8 = v(In8)-v(com)

  Lequiv = Lf + Llk/N**2

  Zo = (Llk/Cblk)**0.5
  Wo = 1/(Llk*Cblk)**0.5
ilf = v1  
Dtrf = v2  
ipk = v3  
ivall = v4  
delta_ilf = v5  
vin = v6  
Doff = v7  
Dblk = v8  

\[
\begin{align*}
v_{cpk} &= ilf \cdot Dtrf \cdot Ts/(2 \cdot N \cdot Cblk) + \\
&\quad (ilf + \delta_{ilf}/2) \cdot Llk/(2 \cdot N \cdot Ts) \\
Dch &= (ilf - \delta_{ilf}/2) \cdot Llk/(vin + v_{cpk})/N/Ts \\
Drs &= Llk \cdot (ilf + \delta_{ilf}/2) / (v_{cpk} \cdot N \cdot Ts + 1e-10) \\
I_{devia} &= (1 - Dtrf) \cdot ilf \\
veff &= vin \cdot Dtrf/N + ilf \cdot Llk/(2 \cdot N \cdot 2 \cdot Ts) \\
zero_{satu} &= \phi_{sat}/Ts - Doff \cdot v_{cpk} - (vin + v_{cpk}) \cdot Dblk \\
v_{out1} &= Dch \\
v_{out2} &= Drs \\
v_{out3} &= I_{devia} \\
v_{out4} &= veff \\
v_{out5} &= v_{cpk} \\
v_{out6} &= zero_{satu}
\end{align*}
\]

) \ # end of values section

equations {

i(Out1->com) += i_{Out1} 
i_{Out1} : v(Out1) - v(com) = v_{Out1}

i(Out2->com) += i_{Out2} 
i_{Out2} : v(Out2) - v(com) = v_{Out2}

i(Out3->com) += i_{Out3} 
i_{Out3} : v(Out3) - v(com) = v_{Out3}

i(Out4->com) += i_{Out4} 
i_{Out4} : v(Out4) - v(com) = v_{Out4}

}
i(Out5->com) += i_Out5
i_Out5 : v(Out5) - v(com) = v_Out5

i(Out6->com) += i_Out6
i_Out6 : v(Out6) - v(com) = v_Out6

} # end of equations section

} # end of template body

C9.2 Template 2.

This template calculates blocking and off duty-cycle, and peak and valley values for primary current.

element template pkvaldeltablkoff com In1 In2 IN3 In4 In5 In6 In7 Out1 Out2 Out3 Out4 Out5 = Ts, Lf, Llk, Cblk, N, phi_sat
electrical com, In1, In2, IN3, In4, In5, in6, iN7, Out1, Out2, Out3, Out4, Out5

number Ts, Lf, Llk, Cblk, N, phi_sat

{
val v v1, v2, v3, v4, v5, v6, v7, ilf, vin, vout, Don, Dch, Drs, Dtrf, Dblk, Doff, delta_up, delta_dwn, delta_ilf, Lemiv,
        Zo, Wo, ipk, ivalll, v_out1, v_out2, v_out3, v_out4, v_out5
var i i_Out1, i_Out2, i_Out3, i_Out4, i_Out5
values {
  v1 = v(In1)-v(com)
  v2 = v(In2)-v(com)
\[ v_3 = v(In3) - v(com) \]
\[ v_4 = v(In4) - v(com) \]
\[ v_5 = v(In5) - v(com) \]
\[ v_6 = v(In6) - v(com) \]
\[ v_7 = v(In7) - v(com) \]

\[ \text{Lequiv} = Lf + \frac{Llk}{N^2} \]
\[ Z_o = \sqrt{\frac{Llk}{Cblk}} \]
\[ W_o = \frac{1}{\sqrt{Llk \cdot Cblk}} \]

\[ \text{vin} = v_1 \]
\[ \text{vout} = v_2 \]
\[ \text{ilf} = v_3 \]
\[ \text{Dtrf} = v_4 \]
\[ \text{Don} = v_5 \]
\[ \text{Dch} = v_6 \]
\[ \text{Drs} = v_7 \]

\[ \text{delta}_\text{up} = \frac{(\text{vin}/N - \text{vout}) \cdot \text{Dtrf} \cdot TS}{\text{Lequiv}} \]
\[ \text{delta}_\text{dwn} = \frac{\text{vout} \cdot (1 - \text{Dtrf}) \cdot Ts}{Lf} \]

\[ \text{delta}_\text{ilf} = \text{delta}_\text{up} \]

\[ \text{Dblk} = \text{Don} - \text{Dch} - \text{Dtrf} \]
\[ \text{Doff} = 1 - \text{Don} - \text{Drs} \]

\[ \text{ipk} = \text{ilf} + \frac{\text{delta}_\text{ilf}}{2} \]
\[ \text{ivall} = \text{ilf} - \frac{\text{delta}_\text{ilf}}{2} \]

\[ \text{v}_\text{out1} = \text{ipk} \]
\[ \text{v}_\text{out2} = \text{ivall} \]
\[ \text{v}_\text{out3} = \text{delta}_\text{ilf} \]
\[ \text{v}_\text{out4} = \text{Dblk} \]
\[ \text{v}_\text{out5} = \text{Doff} \]

\}   # end of values section

\textbf{equations} \{ \]

\[ i(\text{Out1} \rightarrow \text{com}) += i_\text{Out1} \]
\[ i_\text{Out1} : v(\text{Out1}) - v(\text{com}) = v_\text{Out1} \]
i(Out2->com) += i_Out2
i_Out2 : v(Out2) - v(com) = v_Out2

i(Out3->com) += i_Out3
i_Out3 : v(Out3) - v(com) = v_Out3

i(Out4->com) += i_Out4
i_Out4 : v(Out4) - v(com) = v_Out4

i(Out5->com) += i_Out5
i_Out5 : v(Out5) - v(com) = v_Out5

}  # end of equations section
}  # end of template body
D Modified Equations for Cases 2 and 3 of QSS-ZVZCS Three-Phase Buck Rectifier Operation and for Compensated First Duty-Cycle for Case I

D1. Modified Constraint Equations for Case 2

\[ I_2^p = \left( \frac{V_{in}}{L_{lk}} \right) (t_2 - t_1) = \left( m_l \cdot D_{ch1} \cdot T_s \right), \quad (D1.9) \]

\[ I_2^f \neq I_2^p \cdot N, \quad (D1.10) \]

\[ I_3^f = I_3^p \cdot N, \quad (D1.10.a) \]

\[ d_1 \cdot T_s = (t_2 - t_0) = (D_{blk} + D_{ch1}) \cdot T_s. \quad (D1.11) \]

\[ I_3^f - I_2^f = \left( \frac{-V_0}{L_{lk}/N^2 + L_f} \right) \cdot (t_3 - t_2) = \left( N \cdot m_4 \right) \cdot (D_{ch2} \cdot T_s), \quad (D1.12) \]

\[ I_4^f - I_3^f = \left( \frac{V_{ac}/N - V_0}{L_{lk}/N^2 + L_f} \right) \cdot (t_4 - t_3) = \left( N \cdot m_3 \right) \cdot (D_{of2} \cdot T_s) \quad (D1.13) \]

\[ t_5 - t_4 = D_{res} \cdot T_s = \frac{1}{\sqrt{L_{lk} \cdot C_{blk}}} \cdot \arcsin \left( \frac{I_4^p}{V_{Cpk}} \cdot \sqrt{\frac{L_{lk}}{C_{blk}}} \right), \quad (D1.14) \]

\[ \Delta \phi_{off} = \frac{V_{Cpk} \cdot (1 - d_1 - d_2 - D_{res}) \cdot T_s}{N_{sr}}, \quad (D1.15) \]

\[ \Delta \phi_{blk} = 2 \cdot \phi_{sat} - \Delta \phi_{off}, \quad (D1.16) \]
\[ \Delta V_{c\text{-trf}} = \frac{I_L \cdot (D_{trf2}) \cdot T_s}{N \cdot C_{blk}} \]  
(D1.17)

\[ \Delta V_{c\text{-res}} = \frac{(I_4')^2 \cdot L_{ik}}{N \cdot I_L \cdot (D_{trf2}) \cdot T_s} \]  
(D1.18)

\[ V_{cpk} = \frac{\Delta V_{c\text{-trf}} + \Delta V_{c\text{-res}}}{2} \]  
(D1.19)

\[ I_L = \frac{I}{2} \left[ D_{trf2} \cdot (I_4' + I_3') + (I - D_{trf2}) \cdot (I_5' + I_4') \right] \]  
(D1.20)

\[ (I_5' - I_4') = \left( \frac{V_0}{L_f} \right) \cdot (I - D_{trf2}) \cdot T_s = m4 \cdot (I - D_{trf2}) \cdot T_s \]  
(D1.21)

\[ V_{s1} = 0 \]  
(D1.22)

\[ V_{s2} = \frac{V_{\text{line2}} + V_{cb} \cdot L_f + V_0 \cdot L_{ik}}{N \cdot \frac{L_{ik}}{N^2} + L_f} \]  
(D1.23)

\[ \bar{V}_s = \frac{V_{\text{line2}} \cdot D_{trf2} \cdot L_f + \left( \frac{V_0 \cdot L_{ik}}{N^2} + \frac{V_{cb} \cdot L_f}{N} \right) \cdot (D_{trf2})}{\frac{L_{ik}}{N^2} + L_f} \]  
(D1.24)

\[ \bar{V}_{cb} = V_{cpk} = \frac{I_L \cdot (D_{trf2}) \cdot T_s}{2 \cdot N \cdot C_{blk}} \]  
(D1.25)

\[ I_{\text{phase1}} = \frac{I_p}{2} \cdot D_{ch1} \]  
(D1.26)

\[ I_{\text{phase2}} = \frac{(I_5^p + I_4^p)}{2} \cdot D_{ch2} + \frac{(I_5^p + I_4^p)}{2} \cdot D_{trf2} \]  
(D1.27)
D2. Modified Constraint Equations for Case 3

\[ \Delta \phi_{blik} = (t_1 - t_0) \left( \frac{V_{\text{line1}} + V_{\text{cpk}}}{N_{sr}} \right) + (t_2 - t_1) \left( \frac{V_{\text{line2}} + V_{\text{cpk}}}{N_{sr}} \right) = (D_{blik} \cdot T_s) \left( \frac{V_{\text{line1}} + V_{\text{cpk}}}{N_{sr}} \right) + (D_{blik2} \cdot T_s) \left( \frac{V_{\text{line2}} + V_{\text{cpk}}}{N_{sr}} \right), \]  
\[ \Delta \phi_{blik} = (D_{blik} \cdot T_s) + (D_{blik2} \cdot T_s). \]  
\[ I^f_2 = 0, \quad (D2.9) \]
\[ I^f_2 \neq I^g_2 \cdot N, \quad (D2.10.a) \]
\[ I^f_3 \neq I^g_3 \cdot N, \quad (D2.10.b) \]
\[ I^f_4 = I^g_4 \cdot N, \quad (D2.10.c) \]
\[ d_1 \cdot T_s = (t_1 - t_0) = (D_{blik}) \cdot T_s. \]  
\[ d_2 \cdot T_s = (t_3 - t_1) = (D_{blik2} + D_{ch3} + D_{af3}) \cdot T_s. \]  
\[ I^f_3 - I^f_2 = \left\{ \frac{-V_0}{L_{lk}/N^2 + L_f} \right\} \cdot (t_1 - t_2) = (N \cdot m4) \cdot (D_{ch3} \cdot T_s), \]  
\[ I^f_4 - I^f_3 = \left\{ \frac{V_{ac}}{L_{lk}/N^2 + L_f} \right\} \cdot (t_3 - t_3) = (N \cdot m3) \cdot (D_{af3} \cdot T_s) \]  
\[ t_5 - t_4 = D_{res} \cdot T_s = \frac{1}{\sqrt{L_{lk} / C_{blik}}} \cdot \arcsin \left( \frac{I^f_4}{V_{\text{cpk}}} \cdot \sqrt{\frac{L_{lk}}{C_{blik}}} \right), \]  
\[ \Delta \phi_{off} = \frac{V_{\text{cpk}} \cdot (I - d_1 - d_2 - D_{res}) \cdot T_s}{N_{sr}}, \]  
\[ \Delta \phi_{blik} = 2 \cdot \phi_{sat} - \Delta \phi_{off}, \]  
\[ \Delta \phi_{off} = \frac{V_{\text{cpk}} \cdot (I - d_1 - d_2 - D_{res}) \cdot T_s}{N_{sr}}, \]  
\[ \Delta \phi_{off} = \frac{V_{\text{cpk}} \cdot (I - d_1 - d_2 - D_{res}) \cdot T_s}{N_{sr}}. \]
\[ \Delta V_{c-trf} = \frac{I_L \cdot (D_{trf3}) \cdot T_s}{N \cdot C_{blk}} \]  
(D2.17)

\[ \Delta V_{c-res} = \frac{(I_4')^2 \cdot L_{ik}}{N \cdot I_L \cdot (D_{trf3}) \cdot T_s}, \]  
(D2.18)

\[ V_{cpk} = \frac{\Delta V_{c-trf} + \Delta V_{c-res}}{2}. \]  
(D2.19)

\[ I_L = \frac{1}{2} \left[ D_{trf3} \cdot (I_4' + I_3') + (I - D_{trf3}) \cdot (I_5' + I_4') \right], \]  
(D2.20)

\[ (I_5' - I_4') = \left( \frac{V_0}{L_f} \right) \cdot (I - D_{trf3}) \cdot T_s = m4 \cdot (I - D_{trf3}) \cdot T_s, \]  
(D2.21)

\[ V_{s1} = 0 \]  
(D2.22)

\[ V_{s2} = \frac{V_{line2} + V_{cb} \cdot L_f + V_0 \cdot L_{ik}}{N \cdot \frac{L_{ik}}{N^2} + L_f}, \]  
(D2.23)

\[ \bar{V}_s = \frac{V_{line2} \cdot D_{trf3}}{N} \cdot L_f + \left( \frac{V_0 \cdot L_{ik}}{N^2} + \frac{V_{cb} \cdot L_f}{N} \right) \cdot (D_{trf3}) \]  
(D2.24)

\[ \bar{V}_{cb} = V_{cpk} \cdot \frac{I_L \cdot (D_{trf3}) \cdot T_s}{2 \cdot N \cdot C_{blk}}. \]  
(D2.25)

\[ I_{phase1} = 0 \]  
(D2.26)

\[ I_{phase} = \frac{I_5'}{2} \cdot D_{ch3} + \frac{(I_5' + I_5')}{2} \cdot D_{trf3} \]  
(D2.27)
D3. Simplified Equations for Compensated First Duty-Cycle in Case 1

Simplified equations for computation of applied $D_{1}$ in terms of $D_{nrf}$ after neglecting $V_{cpk}$ with respect to $Vin$, and contributions of charging and resetting stages to $V_{cpk}$.

\[ \Delta \phi_{blk} = \frac{D_{blk} \cdot T \cdot V_{line}}{N_{sr}} \]  \hspace{1cm} (1.b)

\[ D_{ch} \cdot V_{line} = \frac{I_{L} \cdot L_{y}}{N \cdot T_{s}}, \]  \hspace{1cm} (2.b)

\[ D_{nrf} = d_{1} - D_{blk} - D_{ch}. \]  \hspace{1cm} (4.b)

\[ D_{res} = \frac{L_{y} \cdot I_{L}}{N \cdot V_{cpk} \cdot T_{s}}. \]  \hspace{1cm} (7.b)

\[ V_{cpk} = \frac{I_{L} \cdot (D_{nrf} + d_{2}) \cdot T_{s}}{2 \cdot N \cdot C_{blk}}, \]  \hspace{1cm} (8.b)

\[ \Delta \phi_{off} = \frac{V_{cpk} \cdot D_{off} \cdot T_{s}}{N_{sr}}, \]  \hspace{1cm} (9.b)

\[ 2 \cdot \phi_{sat} = \Delta \phi_{off} + \Delta \phi_{blk}. \]  \hspace{1cm} (10.b)

\[ D_{off} = 1 - (d_{1} + d_{2} + D_{res}). \]  \hspace{1cm} (11.b)

Solving this set gives

\[ d_{1} = \frac{D_{nrf} + 2 \cdot \phi_{sat} \cdot N_{sr} - I_{g} \cdot \left[ T_{s} \cdot (1 - d_{2}) \cdot (D_{off} + d_{2}) - 2 \cdot L_{y} \right]}{\frac{V_{in} \cdot T_{s}}{N} \cdot \frac{2 \cdot C_{blk} \cdot V_{in}^{2}}{T_{s} \cdot V_{in}}} \]  \hspace{1cm} (17.b)

where $D_{nrf} = D_{pri}$ is the desired primary duty-cycle.
VITA

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From 1985 to 1991 he worked for Lab-Volt Systems, NJ as a Field Engineer in their Ecuadorian division and from 1999 to 2003 he was a design engineer with Dynamic Structures and Materials, Franklin, Tennessee.

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