3.3 Synthesizer

The synthesizer provides the local oscillators (LO) used in the radio. There are two LO synthesizers. One of the synthesizers produces the LO frequency at the transmitting band (1920-1980MHz). It is the RF synthesizer. The output of this synthesizer is split into three outputs, one for the transmitter modulator and the other two outputs are the first LO for each receiver. The other synthesizer produces an LO frequency at 260MHz. Its output is split for the 2\textsuperscript{nd} down-conversion of the two receivers.

The synthesizer consists of three units: the synthesizer board, the splitter board and the 10MHz voltage controllable temperature compensated crystal oscillator (VCTCXO). The VCTCXO is on the AFC board. The VCTCXO supplies the reference frequency for the synthesizer.

The synthesizer is a modified Harris HFA3524 evaluation board. The synthesizer board contains a Harris HFA3524 dual phase-lock-loop (PLL) chip. It provides the simultaneous radio frequency (RF) and intermediate frequency (IF) LO generation.

The splitter board splits and distributes the outputs of the synthesizer board to different parts of the radio. Figure 43 is the block diagram of the synthesizer.
3.3.1 Block Diagram

**Figure 43. Synthesizer block diagram.**

VCO - Voltage Controllable Oscillator
LPF - Low Pass Filter
AMP - Amplifier
ATT - Attenuator
3.3.2 Technical Specifications

The RF synthesizer is programmed for the transmitting frequencies from 1922.5 to 1977.5 MHz in 5MHz increments. The IF synthesizer provides a fixed frequency LO at 260MHz. The requirements for the two synthesizers are different but the design approach and the PLL architecture for each are the same. The discussion of the PLL architecture is based on the RF synthesizer; however the discussion is applicable to the IF synthesizer as well. The differences will be noted.

The 10MHz VCTCXO output is divided by four to obtain a 2.5MHz reference frequency for the RF and IF synthesizers. The frequency accuracy of the synthesizer outputs is equal to the accuracy of the VCTCXO output. The VCTCXO has a trim adjustment to facilitate the frequency setting. The frequency accuracy is set within ±1ppm to comply with the specifications. It also has an electronic adjustment for the AFC. The AFC may tune the VCTCXO ±2ppm from the nominal frequency. Therefore, the RF and IF synthesizer outputs can accommodate a ±2ppm frequency drift.

The splitter board amplifies and splits the LOs from the synthesizer board. The LO power level for the transmitter is –1dBm. This level is within the specified LO drive level of the RF2242 modulator device. The 1st LO power level for the SCM-2500 mixers of the receivers is 7dBm. The 2nd LO power level for the TUF-3SM mixers is 10dBm.

3.3.3 Synthesizer Board

3.3.3.1 Design Modifications

The component designators used in the discussion of this section refer to the schematic shown on the Harris application note AN9630 [22].
RF Synthesizer Modification

The RF synthesizer was originally designed for the 2132-2204 MHz frequency band [22]. The RF VCO was replaced with Zcomm SMV1960L for the desired operational band (1920-1980 MHz). The output attenuation pad was changed from -8dB to -2dB for 8dBm output power. Figure 44 shows the block diagram of the RF synthesizer and indicates the modified parts.

IF Synthesizer Modification

The IF oscillator, which is built on board, was modified from the original 560MHz oscillation frequency to the desired 260MHz. The oscillator is a common collector Colpitts oscillator. Figure 45 shows the oscillator with the frequency determining components.
Figure 45. Frequency determining components of the Colpitts oscillator.

The oscillation frequency is determined by the circuit inductance \( L \) and capacitance \( C \).

\[
f_o = \frac{1}{2\pi \sqrt{L \cdot C}}
\]

(3.3.1)

where

\[
L = L_1 - \frac{1}{(2\pi \cdot f_o)^2 \cdot (C_v + C_a)}
\]

(3.3.2)

\[
C = \frac{C_1 \cdot C_2}{C_1 + C_2}
\]

(3.3.3)

\( C_v \) is the capacitance developed by the varactor diode. It changes the capacitance, \( C_v \), based on the bias voltage from the loop filter. Thus, the oscillation frequency changes until the PLL locks to the target frequency of 260MHz. \( C_a \) provides a fine tune to the oscillator. \( C_1 \) and \( C_2 \) form a capacitive voltage divider to derive a feedback from the output to the base-emitter junction of the transistor. A closed oscillation loop is established. \( C_1 \) and \( C_2 \) are in series to give the circuit capacitance.
Evaluating (3.3.3) with $C_1 = C_2 = 15\, pF$ results in $C = 7.5\, pF$.

Evaluating (3.3.1) with $C = 7.5\, pF$ and $f_o = 260\, MHz$ results in $L = 50\, nH$.

Referring to the data sheet of the varactor, $C_v$ is estimated to be $20\, pF$.

Evaluating (3.3.2) with $L = 50\, nH$, $C_v = 20\, pF$, $C_a = 4.7\, pF$ and $f_o = 260\, MHz$ results in $L_i = 65\, nH$. A standard value, $68\, nH$ was chosen for $L_i$.

Additionally, the RF ($L_2$) choke for the oscillator was changed from $12\, nH$ to $680\, nH$ to give better isolation to the power supply.

The IF oscillator is followed with a three-section, $\pi$-Butterworth low pass filter (LPF). It is used to suppress the harmonic output from the oscillator. It was modified for the cutoff at $350\, MHz$. Figure 46 shows the block diagram of the IF synthesizer and indicates the modified parts.

![Figure 46. IF synthesizer block diagram and the modifications.](image)

**Miscellaneous Changes**

In order to unify the power supplies for the radio, the supply voltage of the synthesizer board is $5\, V$ which is different from the original $3\, V$ design. This change requires the
change of the PLL control signal levels (LE, Clock and Data). The resistors of RA\textsubscript{23}, RA\textsubscript{24}, and RA\textsubscript{25} were changed from 10K\textohm to 5.1\textohm to obtain the level shift.

The chosen VCTCXO is transistor-transistor-logic (TTL) compatible output. Therefore, the 50\textohm termination (R\textsubscript{REF}) at the reference input of the synthesizer board was removed.

As a summary, Table 12 lists all the changes of the components on the synthesizer board that were made to comply with the requirements of the radio.

Table 12. Component changes on the Harris synthesizer board.

<table>
<thead>
<tr>
<th>Part Designator</th>
<th>Was</th>
<th>Is</th>
<th>Change for</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO</td>
<td>Z-Comm SMV2100L</td>
<td>Z-Comm SMV1960L</td>
<td>RF Synthesizer</td>
</tr>
<tr>
<td>L\textsubscript{1}</td>
<td>12 nH</td>
<td>68 nH</td>
<td>IF Synthesizer</td>
</tr>
<tr>
<td>L\textsubscript{2}</td>
<td>12 nH</td>
<td>680 nH</td>
<td>IF Synthesizer</td>
</tr>
<tr>
<td>L\textsubscript{F1}</td>
<td>12 nH</td>
<td>39 nH</td>
<td>IF Synthesizer</td>
</tr>
<tr>
<td>C\textsubscript{F1}</td>
<td>5.6 pF</td>
<td>8 pF</td>
<td>IF Synthesizer</td>
</tr>
<tr>
<td>C\textsubscript{F2}</td>
<td>5.6 pF</td>
<td>8 pF</td>
<td>IF Synthesizer</td>
</tr>
<tr>
<td>RA\textsubscript{4}</td>
<td>20 \textohm</td>
<td>5.5 \textohm</td>
<td>RF Synthesizer</td>
</tr>
<tr>
<td>RA\textsubscript{5}</td>
<td>20 \textohm</td>
<td>5.5 \textohm</td>
<td>RF Synthesizer</td>
</tr>
<tr>
<td>RA\textsubscript{6}</td>
<td>51 \textohm</td>
<td>220 \textohm</td>
<td>RF Synthesizer</td>
</tr>
<tr>
<td>RA\textsubscript{21}</td>
<td>10 K\textohm</td>
<td>5.1 K\textohm</td>
<td>5V Supply</td>
</tr>
<tr>
<td>RA\textsubscript{23}</td>
<td>10 K\textohm</td>
<td>5.1 K\textohm</td>
<td>5V Supply</td>
</tr>
<tr>
<td>RA\textsubscript{25}</td>
<td>10 K\textohm</td>
<td>5.1 K\textohm</td>
<td>5V Supply</td>
</tr>
<tr>
<td>R\textsubscript{REF}</td>
<td>50 \textohm</td>
<td>Nil</td>
<td>VCTCXO TTL Output</td>
</tr>
</tbody>
</table>
3.3.3.2 Loop Filter

The loop filter is the most important part of the PLL design. It is the part available for designers to optimize the PLL performance, as the other parts are off-the-shelf components.

The loop filter was designed to obtain a 25KHz loop bandwidth and the 45° phase margin. The 25KHz loop bandwidth is a hundredth of the 2.5MHz loop reference. This provides good suppression of the reference and eliminates the modulation sidebands. The radio stays on the channel over the course of a conversation. Therefore, the lock in time of the loop is not a critical requirement. The stability of the loop becomes the design criterion. The phase margin of the loop provides the stability and was chosen to be 45°. The loop was chosen to be type-2, 4th-order. The required loop filter is shown in Figure 47.

![Figure 47. The realization of the loop filter.](image)

The transfer function for the loop filter is given by

$$K_f(s) = \frac{sR_1C_1 + 1}{s^2[R_1R_2C_0C_1C_2 + s(R_1C_0C_1 + R_2C_0C_2 + R_2C_1C_2 + R_1C_1C_2) + C_0 + C_1 + C_2]}$$

(3.3.4)
The detailed design procedure of a PLL can be found in [23]. Figure 48 and 49 are the simulated gain and phase response of the loop respectively.

**Figure 48.** Gain response of the type-2, 4th-order loop.

**Figure 49.** Phase response of the type-2, 4th-order loop.
The simulation is based on the loop response for the middle channel (1952.5MHz). The choice of the channel affects the N-divider values of the PLL. The divider values to program the PLL is given in Appendix E. The use of the standard component values produces the performance deviation between the target and simulation. The deviation is small and is not a problem. No potential instability of the loop was experienced in the laboratory evaluation.

### 3.3.4 Splitter Board

The splitter board has the RF and IF channels, and supplies the LOs at specified power levels and provides adequate reverse isolation. The full schematic is in Appendix C-6.

#### 3.3.4.1 RF Channel

Figure 50 is the block diagram of the RF channel.

![RF channel block diagram](image)

As shown in Figure 50, the RF synthesizer output level is 7dBm. The RF2422 modulator requires an LO power between –3 and 3dBm. The splitter is designed to deliver -1dBm to the transmitter. The splitter supplies the LOs at 7dBm to the receiver 1st mixer.

The first two stages of the channel are a 20dB attenuator (Appendix C-6: R350-352) and a 20dB gain block (Appendix C-6: U35). They provide a reverse isolation between the synthesizer and the modulator. Without the buffer, the modulation process in the
modulator caused a disturbance at the VCO output of the RF synthesizer. The loop will not compensate for any disturbance outside the loop bandwidth. The modulation sidebands of the disturbance developed at the synthesizer output. Since the receivers share the same synthesizer output, these sidebands became a noise source to the receivers. The attenuator and the gain block provide a total of 43dB reverse isolation. The ERA-3SM was selected for its small reverse transmission ($S_{12} = -23$dB).

Mini-Circuits LRPS-2-25 splitters were selected. One-to-two splitting causes the output to be 3dB lower than the input. The splitter has 1dB insertion loss. Therefore, the total signal attenuation of the splitter is 4dB. A splitter (Appendix C-6: U30) divides the RF signal into two outputs. One output is attenuated by 4dB (Appendix C-6: R300-302) and supplied to the transmitter modulator as shown in the upper chain of Figure 50. The power level of this output is –1dBm. The other output is further divided by a splitter (Appendix C-6, U32) into two to supply the two receivers as shown in the lower chain of Figure 50. A Mini-Circuits ERA-1SM amplifier (Appendix C-6: U33) compensates the loss due to the attenuator (Appendix C-6: R310-312) and the splitters so that the output power of the two outputs is 7dBm.

3.3.4.2 IF Channel

The IF channel provides one-to-two splitting for the IF synthesizer output. This channel has 2dB gain so that the IF LOs are 10dBm. Figure 51 is the block diagram of the IF channel.

![IF channel block diagram](image)

Figure 51. IF channel block diagram.
The splitter (Appendix C-6: U33) is different from the splitter used in the RF channel because the IF frequency is much lower than the RF frequency. The splitter is Mini-Circuits LRPS-2-1. The splitter causes 4dB signal attenuation. The resistive attenuator (Appendix C-6: R330-331) is a 6dB pad and the same ERA-1SM amplifier (Appendix C-6, U33) is used as the gain block. The total gain of the channel is 2dB; therefore, an 8dBm input produces a 10dBm output.