High-Level Synthesis and Implementation of Built-In Self-Testable Data Path Intensive Circuit

Han Bin Kim

Dissertation submitted to the Faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

Dong S. Ha, Chair
J. R. Armstrong
F. G. Gray
S. M. Henry
S. F. Midkiff

December 15, 1999
Blacksburg, Virginia
High-Level Synthesis and Implementation of
Built-In Self-Testable Data Path Intensive Circuit

Han Bin Kim

ABSTRACT

A high-level built-in self-test (BIST) synthesis is a process of transforming a behavioral
description into a register-transfer level structural description while minimizing BIST overhead.
Existing high-level BIST synthesis methods focus on one objective, minimizing either area
overhead or test time. Hence, those methods do not render exploration of a large design space,
which may result in a local optimum.

In this thesis, we present three methods, which aim to address the problem. The first
method tries to find a register assignment for each $k$-test session in a heuristic manner, where
$k=1,2,\ldots,N$ and $N$ is the number of modules of the circuit. Therefore, it offers a range of designs
with different figures of merit in area and test time. The second method is based on integer linear
programming (ILP). The proposed ILP based method performs the three tasks, assignments of
registers, interconnections, and BIST registers, concurrently to yield optimal or near-optimal
designs. We describe a complete set of ILP formulations for the three tasks. The ILP based
method achieves optimal solutions for most circuits in hardware overhead, but it takes long
processing time. The third method, the region-wise heuristic method. It partitions a given data
flow graph into smaller regions based on control steps and applies the ILP to each region
successively to reduce the processing time.

To measure the performance of BIST accurately and to demonstrate the practicality of
our BIST synthesis method, we implemented a DSP circuit; an 8×8 two-dimensional discrete
cosine transform (DCT) processor. We implemented two versions of the algorithm, one with
incorporation of our BIST method and the other without BIST, to verify the validity of our
simplified cost model to estimate BIST area overhead. The two major parts of the circuit, data
path and controller, were synthesized using our high-level BIST synthesis tool. All the circuits are implemented and laid out using an ASIC design flow developed at Virginia Tech.

Experimental results show that the three proposed high-level BIST synthesis methods perform better than or comparable to existing BIST synthesis systems. They indeed yield various designs that enable users to trade between area overhead and test time. The region-wise heuristic method reduces the processing time by several orders of magnitude, while the quality of the solution is slightly compromised compared with the ILP-based optimal method. The implementation of DCT circuits demonstrate that our method is applicable to industry size circuits, and the BIST area overhead measured at the layout is close to the estimated one.
Acknowledgements

I would first like to thank to Dr. Dong S. Ha, my advisor, for incessant support and guidance toward excel in this research and writing a paper. The achievements described in the dissertation were possible by numerous people’s help.

I would like to give thanks to people in Advantest, Mr. Yamaguchi Takahiro, Mr. Takeshi Takahashi, and Mr. Mashiro Ishida who involved with initiating and taking care of this High-Level BIST Synthesis project. Special thanks are directed to Mr. Takeshi Takahashi who was willing to help me in programming and setup the fundamental structure of the project.

One of the most valuable supports to solve a high-level synthesis problem comes from Dr. Tae Hyung Park who provides me a lot of guidance and insight involved with integer linear programming.

The library development project, although not research-oriented one, was one of the toughest tasks, accomplished with the help of Mr. Tae Hoon Kim and Mr. Jun Suk Kim at Cadence and Dr. Kwang Hyun Kim at Samsung. I also appreciate help from our group members, Carrie Aust, Jia Fei, Meenatchi Jagasivamani, and Jos Sulistyo. I’m also thankful to Andrew Bouldey in helping documentation of User’s Manual. I have enjoyed discussions and spent a lot of good time with our group members, Byung Ha Joo, Mohammed Osman, Prashanth Aprameyan, Kumaravel Jagasivamani, Ranpara Samirkumar, and Suk Won Kim. I also would like to thanks to my committee members for their valuable comments and feedbacks.

Finally, I would like to appreciate my family: Myung Joo Lee, my wife, Barron, my son and Ko Un, my daughter who spend their time not much with me but always welcome and support me.
# Contents

1 Introduction .................................................................................................................. 1

2 Background .................................................................................................................. 6
   2.1 High-Level Synthesis ............................................................................................... 6
      2.1.1 Control Data Flow Graph ............................................................................... 6
      2.1.1.1 DFG for Data Path Intensive Circuit ......................................................... 7
      2.1.1.2 CDFG for Controller-Intensive Circuits .................................................... 8
   2.1.2 Scheduling .......................................................................................................... 10
   2.1.3 Transformation .................................................................................................... 12
      2.1.3.1 Structural Pipelining ............................................................................... 12
      2.1.3.2 Functional Pipelining ............................................................................... 13
      2.1.3.3 Loop Folding ............................................................................................. 13
      2.1.3.4 Loop Unrolling ......................................................................................... 14
   2.1.4 Module Assignment ............................................................................................... 15
   2.1.5 Register Assignment ............................................................................................ 17
   2.1.6 Interconnection Assignment ................................................................................ 20
   2.2 Built-In Self-Test (BIST) ....................................................................................... 23
      2.2.1 Test Pattern Register (TPG) and Linear Feedback Shift Register (LFSR) ...... 25
      2.2.2 Signature Register (SR) .................................................................................. 26
      2.2.3 Built-In Block Observer (BILBO) .................................................................... 27
      2.2.4 Concurrent BILBO (CBILBO) ........................................................................ 27
      2.2.5 BIST Register Assignment .............................................................................. 28
   2.3 Integer Linear Programming ..................................................................................... 30
3.2.3 BIST Register Assignment .................................................. 62
  3.2.3.1 SR Assignment ......................................................... 62
  3.2.3.2 TPG Assignment ....................................................... 64
  3.2.3.3 BILBO and CBILBO Assignment .................................. 65

3.2.4 Constants ........................................................................ 67

3.2.5 Objective Function ............................................................ 68

3.2.6 Reduction of the Search Space ............................................. 69

3.3 Region-Wise ILP Based Approach ............................................ 71
  3.3.1 Motivation and Overall Procedure ...................................... 71
  3.3.2 Region-Wise System Register Assignment ............................. 75
  3.3.3 Region-Wise Interconnection Assignment .............................. 75
  3.3.4 Region-Wise BIST Register Assignment ................................. 77
    3.3.4.1 SR Assignment .......................................................... 77
    3.3.4.2 TPG Assignment ........................................................ 79
    3.3.4.3 BILBO and CBILBO Assignment ................................... 80

3.4 Constants ............................................................................ 82

3.5 Objective Function ............................................................... 83

4 Implementation of a test circuit ................................................ 85
  4.1 ASIC Design Flow ............................................................... 86
    4.1.1 Behavior and Logic Design .............................................. 87
    4.1.2 Circuit and Layout design ............................................... 88
  4.2 High-Level BIST Design ....................................................... 88
  4.3 Library Development ............................................................ 91
  4.4 Discrete Cosine Transformation (DCT) .................................... 93
    4.4.1 Fast DCT Algorithm ...................................................... 95
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>A.4 Register Assignment and Interconnection Assignment</td>
<td>140</td>
</tr>
<tr>
<td>A.4.1 CPLEX</td>
<td>140</td>
</tr>
<tr>
<td>A.4.2 Optimal Assignment</td>
<td>142</td>
</tr>
<tr>
<td>A.4.2.1 High Level Synthesizer</td>
<td>143</td>
</tr>
<tr>
<td>A.4.2.2 High Level BIST Synthesizer</td>
<td>143</td>
</tr>
<tr>
<td>A.4.3 Region by Region Assignment</td>
<td>144</td>
</tr>
<tr>
<td>A.4.4 Heuristic Assignment</td>
<td>144</td>
</tr>
<tr>
<td>A.4.4.1 Default Algorithm</td>
<td>145</td>
</tr>
<tr>
<td>A.4.4.2 Avra’s Algorithm</td>
<td>146</td>
</tr>
<tr>
<td>A.4.4.3 Parullkar’s Algorithm</td>
<td>146</td>
</tr>
<tr>
<td>A.5 Design Analysis</td>
<td>147</td>
</tr>
<tr>
<td>A.5.1 ilpformlist</td>
<td>147</td>
</tr>
<tr>
<td>A.5.2 gentabilp</td>
<td>148</td>
</tr>
<tr>
<td>A.5.3 form</td>
<td>148</td>
</tr>
<tr>
<td>A.5.4 gentab</td>
<td>149</td>
</tr>
<tr>
<td>A.6 Register Transfer Level VHDL Generation</td>
<td>150</td>
</tr>
<tr>
<td>A.6.1 Data Path VHDL Description</td>
<td>150</td>
</tr>
<tr>
<td>A.6.1.1 Multiplexer Description</td>
<td>150</td>
</tr>
<tr>
<td>A.6.1.2 Register Description</td>
<td>151</td>
</tr>
<tr>
<td>A.6.1.3 Module Description</td>
<td>151</td>
</tr>
<tr>
<td>A.6.1.4 Constant Description</td>
<td>152</td>
</tr>
<tr>
<td>A.6.1.5 Output Port Description</td>
<td>152</td>
</tr>
<tr>
<td>A.6.2 Controller VHDL Description</td>
<td>153</td>
</tr>
<tr>
<td>Appendix B: DSP Benchmark Circuits</td>
<td>156</td>
</tr>
<tr>
<td>B.1 Introduction</td>
<td>156</td>
</tr>
</tbody>
</table>
B.2 6th Order FIR Filter ................................................................. 157
B.3 3rd Order IIR Filter Cascade Connection .......................... 159
B.4 6-Tap Wavelet Filter ................................................................. 161
B.5 4-Point Discrete Cosine Transformation (DCT) ................ 163
B.6 Tseng .......................................................... 165
B.7 Paulin .......................................................... 166

Bibliography ............................................................................ 167
List of Tables

3.1 Possible optimal mergers for the data flow graph in Fig. 3.1(a) ........................................ 53
4.1 Lists in/out port of our 8×8 2-D DCT circuit................................................................. 99
4.2 Functionality of internally generated control signals....................................................... 101
4.3 Operating modes of 16-bit BILBO.................................................................................. 106
4.4 Operating modes of modified 16-bit BILBO................................................................. 106
4.5 Test modes and control signals......................................................................................... 109
5.1 Characteristics of the circuits.......................................................................................... 112
5.2 Number of transistors of 8-bit test registers and multiplexers........................................ 113
5.3 Performance of ADVAN.................................................................................................... 115
5.4 Performance of the proposed method ADVBIST............................................................. 117
5.5 Processing time (in seconds) of the proposed region-wise ILP method ...................... 119
5.6 Area overhead of the proposed heuristic.......................................................................... 120
5.7 Performance of various high-level BIST synthesis systems............................................. 123
5.8 Characteristics of the DCT circuit and performance of its BIST implementation........ 125
5.9 Characteristics of two chips.............................................................................................. 126
5.10 Test schedule.................................................................................................................... 128
# List of Figures

2.1  A 6th order FIR filter ........................................................................................................ 7  
2.2  Silage program of a 6th order FIR filter ........................................................................... 8  
2.3  Unscheduled data flow graph of a 6th order FIR filter ...................................................... 8  
2.4  Basic control data flow graph elements ............................................................................. 9  
2.5  GCD description ................................................................................................................ 9  
2.6  Paulin’s DFG .................................................................................................................... 11  
2.7  ASAP Scheduled DFG ....................................................................................................... 11  
2.8  ALAP scheduled DFG ........................................................................................................ 11  
2.9  List scheduled DFG ........................................................................................................... 11  
2.10 A scheduled DFG using structural pipelining ................................................................. 13  
2.11 A scheduled DFG using functional pipelining ............................................................... 13  
2.12 DFG for FIR ..................................................................................................................... 14  
2.13 DFG for IIR ...................................................................................................................... 15  
2.14 A data flow graph, given modules and incompatibility graph ........................................ 17  
2.15 A data flow graph and its incompatibility and compatibility graphs ................................ 18  
2.16 Left edge algorithm (a) variable intervals (b) assignment results ................................. 19  
2.17 Various data path architectures ......................................................................................... 21  
2.18 Input swapping: (a) compatibility graph (b) simplified interconnection ....................... 22  
2.19 Typical BIST structure .................................................................................................... 23  
2.20 LFSR for (a) generic case and, (b) n=4 .......................................................................... 25  
2.21 A schematic of signature register ..................................................................................... 26  
2.22 A schematic of BILBO ..................................................................................................... 27  
2.23 A schematic of CBILBO .................................................................................................. 28  
2.24 Self-adjacent register ....................................................................................................... 29  
2.25 Self-adjacent register and its reconfiguration to a SR .................................................... 29  
2.26 Allocation of signature registers ....................................................................................... 30  
2.27 A data flow graph and a synthesized data path ............................................................... 33  
2.28 Connections between pseudo-input ports and input ports ........................................... 35
2.29 Connections between pseudo-input ports and input ports.......................... 39
2.30 A structure of testable functional blocks......................................................... 41
2.31 Register assignment in Avra’s method.............................................................. 42
2.32 Data flow graph and its conflict graph.............................................................. 43
2.33 Data flow graph for Zone Scheduling............................................................... 45
2.34 Divided data flow graph in Zone Scheduling.................................................... 46
3.1 Example data flow graph and its data path....................................................... 50
3.2 A data flow graph with module assignment................................................... 56
3.3 Compatibility graphs before and after the merger......................................... 59
3.4 Merger of vertices a and g.............................................................................. 62
4.1 Design flow....................................................................................................... 87
4.2 High-level BIST synthesis system................................................................. 89
4.3 Library development process........................................................................... 91
4.4 JPEG system with DCT.................................................................................. 93
4.5 Data flow graph for 8-point DCT..................................................................... 97
4.6 Target data data/controller architecture for 1-D DCT..................................... 99
4.7 Timing diagram for external in/out port......................................................... 100
4.8 Schematic of 2-D DCT..................................................................................... 101
4.9 Timing diagram of row 1-D DCT..................................................................... 102
4.10 Schematic of the transposition memory....................................................... 102
4.11 Timing diagram between row and column 1-D DCT.................................... 103
4.12 Timing diagram of the last part of column 1-D DCT..................................... 104
4.13 A schematic for 16-bit TPG with $P(x) = x^{16} + x^5 + x^3 + x^2 + 1$........ 105
4.14 A schematic for 16-bit SR with $P(x) = x^{16} + x^5 + x^3 + x^2 + 1$........... 105
4.15 A schematic for generic 16-bit BILBO....................................................... 106
4.16 A schematic for modified 16-bit BILBO..................................................... 106
4.17 BIST configuration for testing of DCT data paths......................................... 107
4.18 BIST structure of the controller................................................................... 108
5.1 Layouts of 8×8 DCT....................................................................................... 126
5.2 BIST Configuration at session 0.................................................................... 128
5.3 Fault coverage of the adder.......................................................................... 129
5.4 Fault coverage of the subtractor..................................................................... 129
5.5 Fault coverage of the multiplier

5.6 Fault coverage of the controller

B.1 A 6th order FIR filter

B.2 Silage program of a 6th order FIR filter

B.3 Data flow graph of a 6th order FIR filter

B.4 A 3rd order IIR filter (cascade connection)

B.5 Silage program of a 3rd order IIR filter (cascade connection)

B.6 Data flow graph of a 3rd order IIR filter (cascade connection)

B.7 A 6-tap wavelet filter

B.8 Silage program of a 6-tap wavelet filter

B.9 Data flow graph of a 6-tap wavelet filter

B.10 Silage program of a 4-point discrete cosine transformation

B.11 Data flow graph of a 4-point discrete cosine transformation

B.12 Data flow graph of Tseng

B.13 Data flow graph of Paulin
Chapter 1

Introduction

The design process of a digital system, especially of a digital signal processing system, usually starts at a behavior level and descends to a structural level. Test synthesis is to incorporate design-for-testability features in the design process. Until the end of 80’s, testability was usually inserted into a structural level (mostly at the gate level) as a post processing of the logic design. However, the approach often fails to yield a good solution in terms of hardware overhead, fault coverage and testing time due to an inappropriate choice of hardware structure made in an earlier design stage.

In order to address the problem, researchers investigated the incorporation of testability into the front-end of the design process called high-level test synthesis [1]-[26]. High-level synthesis is to transform a behavioral description of a design into a structural implementation comprised of data path logic and control logic [27]. High-level test synthesis incorporates some testability feature(s) during the high-level synthesis, and the resultant circuit is easier to test than the original circuit in which testability is not considered. An excellent survey for high-level test synthesis is available in [1].

Design-for-testability (DFT) technique [28] deals with improving testability of a circuit under design. While improving the testability, it degrades some of design characteristics such as area, performance, and power consumption. However, DFT reduces test cost, improves product quality, and reduces time-to-market. DFT technique has, in generally, three different approaches: ad-hoc design-for-testability, scan-based design, and BIST-based design.

Most common ad-hoc DFT technique is a test-point insertion in which a hard-to-test node is identified and a dedicated access port is added to the node. Other ad-hoc technique includes abiding rules such as avoidance of asynchronous circuit and redundant logic. Scan-based DFT technique is most widely used. Some or all system registers are modified to be scannable by
which internal nodes can be controllable and observable from the outside. It results in better testability while sacrificing area and performance. Scan design is primarily for improving accessing of internal nodes. However, it is often hard to access I/O pins when a chip is embedded in a multiple-layered board. Scan design can be employed along I/O pins of a chip, which is referred to as boundary scan, or external scan. BIST-based DFT techniques becomes popular not only for embedded memory testing, but also logic circuit testing. Built-in self-test (BIST) is one of design-for-test (DFT) techniques in which a test pattern generator (TPG) and a signature analyzer (SA) are embedded on the same chip [28]. A BIST is necessary to test hard-to-access internal nodes such as embedded memory. Also it has other advantages such as i) at-speed testing is possible, ii) the need for test pattern generation and test data evaluation is eliminated, iii) expensive automatic test equipment (ATE) can be avoided, and iv) field testing is possible. Parallel BIST, which is based on random pattern testing, employs test pattern generators and test data evaluators for every module under test (which is usually a combinational circuit). Parallel BIST often achieves relatively high fault coverage compared with other BIST methods such as circular BIST [29].

High-level synthesis is a process of transforming a behavioral description into a structural description comprising data path logic and control logic [27]. First, a behavioral description is converted into a control data flow graph (CDFG). Then operations are scheduled in clock cycles (scheduling), a hardware module is assigned to each operation (module assignment), and registers are assigned to input and output variables (register assignment). The basic tasks in high-level synthesis area such as scheduling, transformation, module assignment, register assignment, and interconnection assignment are briefly described in the following.

Scheduling determines the precise start time of each operation for a given data flow graph [27],[30]. The start times must satisfy the original dependencies of the graph, which limit the amount of parallelism of the operations. Transformation such as pipelining and retiming is to modify a given DFG, while preserving the functionality of the original DFG. A transformed DFG usually yields a different hardware structure, which leads to a different structure for testability and power consumption. Assignment tasks in the high-level synthesis can be solved
by the graph coloring algorithm. There have been a number of algorithms for graph coloring, but, three most popular methods used in high-level synthesis are left edge algorithm [31], clique partitioning [32], and perfect vertex elimination scheme (PVES) [33]. All the methods mentioned above are based on heuristic to shorten the processing, thus, they do not guarantee an optimal solution.

Integer linear programming (ILP) has been used to perform specific tasks in high-level synthesis. Hafer and Parker pioneered in formulating high-level synthesis problems into an ILP model in 1983 [35]. Since then, many researchers investigated ILP models to address synthesis problems [36]-[39]. Some recent works include Gebotys and Elmasry [38] and Rim et al. [39]. Gebotys and Elmasry [38] applied an ILP to architectural synthesis where a scheduling and a module/register allocation are performed concurrently. Rim et al. presented an ILP model to solve the binding problem with focus on minimizing hardware resources (such as modules, registers, and wires) [39]. Various ILP formulations for scheduling and binding problems are available in literature [30]. A major advantage of an ILP based approach is that the obtained solution is optimal though computationally intensive due to the inherent nature of ILP, which involves an exhaustive search.

High-level test synthesis generates register-transfer level data paths with enhanced testability. Depending on the testability schemes incorporated, high-level test synthesis systems can be classified into three groups. The first group of high-level test synthesis systems aims to improve the controllability and/or the observability of the circuit [3]-[8]. The methods are ones such as insertion of test points, minimization of cycles and/or sequential depth. The second group of high-level test synthesis systems incorporates the scan technique [9]-[16]. While incorporating the scan technique, the systems try to minimize sequential depth and/or cycles, and maximize the number of input and output registers. The third group of high-level test synthesis systems employs built-in self-test (BIST), specifically parallel BIST [17]-[26]. Parallel BIST, which is based on random pattern testing, employ test pattern generators and test data evaluators for every module under test (which is usually a combinational circuit). Parallel BIST often achieves relatively high fault coverage compared with other BIST methods such as circular BIST [29].
this thesis, we present a high-level BIST synthesis method that employs the parallel BIST structure.

In this thesis, we describe our three different methods for a high-level BIST synthesis system; heuristic based method, ILP based optimal method, and region-wise ILP based method. We describe our methods briefly in the following.

The existing high-level BIST synthesis methods, described in the section 1.3, focus on one objective, minimizing either the area overhead [17]-[24] or the test time [25], [26]. Hence, those methods do not render exploration of large design space, which may result in a local optimum. Another aspect that was overlooked in those methods is that area overhead and test time are often traded in BIST (as well as other design-for-testability methods). Therefore, it is more desirable to offer various design alternatives (with different area overhead and test time) to the designer, and let the designer choose a proper design for his/her needs. Our method intends to address those two problems.

For a scheduled and module-assigned data flow graph, our heuristic based method allocates signature registers which guarantee the circuit be tested in $k$-test session, where $k$ is 1, 2, ..., N, and N is the number of modules. Our method [40] tries to find an optimal design (which incurs the smallest area overhead) for each $k$-test session. Hence, it explores a far larger design space compared with other methods. It also allows designers to trade area and test time. A designer whose concern is only area overhead can choose the most area efficient design among N designs, while one concerned with only test time chooses the design for $k=1$.

Another proposed method is based on ILP, which generates an optimal solution. The focus of high-level BIST synthesis is register assignment, which involves three subtasks, system register assignment, BIST register assignment and their interconnections (called interconnection assignment). To reduce the complexity involved in the assignment process, existing high-level BIST synthesis methods decouple the three subtasks and perform the subtasks sequentially at the cost of global optimality. We present ILP formulations for high-level BIST synthesis with an objective of minimizing the area for each $k$-test session where $k$ is 1, 2, ...N and N is the number of modules. Hence, our ILP based method tries to find N optimal (in area) BIST circuits of
which a BIST circuit for a $k$-test session tests the entire modules in exactly $k$ sub-test sessions. Hence, like our heuristic method presented in [40], our ILP-based method [41] offers a range of designs with different figures of merit in area and test time. Our experimental results show that the proposed approach successfully synthesizes BIST circuits for each test session for all six circuits experimented. All the BIST circuits are better in area overhead than those generated by existing BIST synthesis methods.

The last proposed method is a region-wise ILP method [42], which intends to reduce the processing time for our ILP, based method. The heuristic divides a given data flow graph into sub-regions and applies an ILP for each region successively. Our experimental results show that the proposed heuristic reduces the processing time by several orders of magnitude, while the quality of BIST designs is compromised moderately.

To evaluate our proposed high-level synthesis system, we implemented one of widely used DSP circuits; an $8 \times 8$ two-dimensional discrete cosine transform (DCT) processor. A brief overview of implementation of DCT circuit and related topics such as design flow and library development are presented in Chapter 4.

The thesis is organized in the following manner. We briefly explain high-level BIST synthesis, an ILP model, and describe necessary terms in Chapter 2. We present our three methods for high-level BIST synthesis, the heuristic based method, the ILP based method, and the region-wise ILP method in Chapter 3. In Chapter 4, we describe implementation of an $8 \times 8$ two-dimensional discrete cosine transform (DCT) processor, and an ASIC design flow. Chapter 5 contains experimental results for the three methods. The performance of our method is compared with other BIST synthesis methods. We also present results on a large BIST circuit synthesized by the proposed method and layout through a standard cell design approach. Chapter 6 concludes the thesis.