Modeling and Design of Digitally Controlled Voltage Regulator Modules

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(Abstract)

It can be expected that digital controllers will be increasingly used in low voltage, high-current and high frequency voltage regulator modules (VRMs) where conventional analog controllers are currently preferred because of the cost and performance reasons. However, there are still remaining two significant challenges for the spread of the digital control techniques: quantization effects and the delay effects.

Quantization effects might introduce the limit cycle oscillations (LCOs) to the converter, which will generate the stability issues. Actually, LCOs can not be totally eliminated theoretically. One way to reduce the possibilities of LCOs is to employ a high resolution Digital Pulse-Width-Modulator (DPWM). However, designing such a DPWM which can meet the requirements of VRMs application requires ultra-high system clock frequency, up to several GHz. Such high frequency is impractical due to huge power consumption. Hybrid DPWM might be an alternative solution but will occupy large silicon area. Single phase digital constant on-time modulation method is another good candidate to improve the DPWM resolution without adding too much cost. However, directly extending this method to multi-phase application, which is the prevalent structure in VRMs application, will introduce some issues. With more phases in parallel, the duty cycle resolution will drop more.
To solve the mentioned issue, this work proposed a multi-phase digital constant on-time modulation method. The proposed method will control the control voltage to alternate between two adjacent values, or dither, within one switching period. The outcome is that the phase duty cycle’s resolution is improved and independent on phase number. Compared with conventional constant frequency modulation method, the proposed method can achieve about 10 times higher duty cycle resolution for the VRM application. The effectiveness of the proposed method is verified by the simulation as well as the experiment results.

Delay effect is another concern for the digital controlled VRMs. There exist several types of delays in the digital feedback loop, including the ADC conversion delay, digital compensator calculation delay, DPWM delay as well as some propagation delays. Usually these delays are inside the digital controller and it is hard to know the exact values. There are several papers talking about the small signal models of the digital voltage mode control. These models are valid only if all the delay terms are known exactly since each delay is considered separately. Actually, this process is not easy. Moreover, there is no literature talking about the complete small signal model of the digital VRMs. But in reality, different implementations of the sampling process will give different impacts to the loop.

This work proposed the small signal signal models of digital VRMs. The analysis is based on the assumptions that DPWM is a double-edge modulation and the sampling instants are aligned with the middle of one phase’s off time. At first, the conversion and calculation delay is neglected. The focus of the modeling is on the small signal model of the current sampling methods and the DPWM delay. This model is valid for those digital
controllers which have fast ADC and fast calculation capabilities. It is shown that even with a “fast” controller, the current sampling and DPWM might introduce some delay to the loop.

After that, the conversion and calculation delay are considered into the modeling. Two time periods, $T_{tg}$ and $T_{1r}$, are employed to describe the total delay effects in the control loop. It is observed that the total delay in the loop is integral times of sampling periods, which is never reported by any other literatures. Therefore, the proposed model only includes one delay term and the value of this delay can be found through a pre-determined lookup table. Finally, the complete small signal model of the digital VRMs considering the conversion and calculation delay is proposed. This model is helpful for the researchers to find the delay effects in their control loop based on the range of the total physical delay in the controller.

With the derived small signal models of digital VRMs, the design guideline for AVP control are presented. The digital active-droop control is employed and it borrows the concept of constant output impedance control from the analog world. Two design examples are provided for the verification.
TO MY PARENTS

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1.1 Digital control for DC/DC converters

With the development of semiconductor technology and increasing demanding for system level power management, the digital control is playing a more and more important role in the power electronics world. Over the last two decades, digital control methods and digital controllers based on general-purpose micro-processors, digital signal processors (DSP’s), or programmable logic devices become pervasive in applications such as motor drives and three-phase power converters for utility interfaces [1, 2]. In these applications, control and monitoring tasks are often very complex, while the power semiconductor devices are operated at relatively low switching frequencies, e.g., at tens of kilohertz.

Based on recent innovations in digital DC/DC converter control methods, architectures and circuit implementation techniques, together with the continued rapid advances semiconductors and digital VLSI technology, possibilities are now open for a new generation of simple and practical, yet high-performance digital controllers for DC-DC converters.

Potentially, the advantages with the digital techniques applied for DC/DC converters can be summarized as:

- Low sensitivity to parameter variations.
- Programmability and monitoring.
- Friendly Graphic User Interface (GUI) design tool.
- Reduction or elimination of external passive components,
- Implementation of advanced control, calibration or protection algorithms,
- Auto-tuning capability for system identifications and compensation design.

Attributing to these merits, industry began to shift their focus from traditional mature, analog control to digital control for DC/DC converters. Currently, there are quite a few industry products of digital controllers for Point of Load (POL) converters, including Texas Instrument, Primarion, Zilker Lab, Silicon Lab, On-Semi, Volterra, Chil Semiconductors, Micro-chip, iWatt, et..

In a typical voltage mode digitally controlled DC-DC converter as shown in Figure 1.1, the feedback control loop contains a voltage Analog-to-Digital Converter (ADC), a digital compensator as well as a Digital Pulse-Width-Modulator (DPWM) [3-10].

![Figure 1.1 Digitally Controlled DC-DC Converters](image)

In the feedback loop, the ADC serves as the interface between the analog world and the digital world: it performs two tasks on the signals: sampling and quantization. The key waveforms of a voltage ADC is shown in Figure 1.2, where $\Delta V_{ADC}$ represents the resolution.
Digital compensator performs as the function of error amplifier in the analog control. Normally, difference equation is employed to describe the digital compensator, which is shown as:

$$v_c[n] = a_1 \cdot v_c[n-1] + a_2 \cdot v_c[n-2] \cdots + b_0 \cdot v_e[n] + b_1 \cdot v_e[n-1] + \cdots$$  \hspace{1cm} (1-1)

where $v_c[n]$ and $v_e[n]$ represent the control signal and the sampled error signals at $n$ instant. For a DC-DC converter, usually a digital PID type compensator is utilized, which has a form of:

$$v_c[n] = v_c[n-1] + b_0 \cdot v_e[n] + b_1 \cdot v_e[n-1]$$  \hspace{1cm} (1-2)

It can be seen from (1-2), the implementation of a digital PID compensator needs several multiplications and additions. One way to implement this compensator is performing these calculations by the digital controllers itself, which requires fast calculation capability of the controllers. The alternative is employing a look-up table to do the compensation job, which is much faster than previous one [11]. The disadvantages of this method include limit error range and simple compensator’s structure.
Digital Pulse-Width-Moulator (DPWM) transfer the control signal $v_c[n]$, which is the output of the digital compensatoetr, to a continuous duty cycle signal, $d$. A trailing edge DPWM is shown in Figure 1.3: (a) shows the structure and (b) shows the operation principle.

(a) DPWM structure
(b) Operation principle of DPWM

Figure 1.3 Structure and operation principle of a trailing edge DPWM

In this example, the $N$-bit counter will count the number of clocks, which equivalently build a digital ramp as shown in Figure 1.3 (b). The digital compare will compare the digital ramp with the control voltage. When $V_c[n]$ reaches the value of the digital ramp, the trailing edge of one duty cycle is generated. Similar to the analog pulse-width-modulator, DPWM has trailing edge, leading edge, double edge, constant on-time and constant off-time modulation methods.

1.2 Challenges of Digital Control for VRMs

Besides the merits, there are still remaining several challenges for the digital control of high frequency DC-DC converters: quantization effects and delay effects. Quantization effects may introduce the limit cycle oscillations (LCOs) to the system and delay effects may hurt the dynamic performance of the converter.
With the increasing speed of the microprocessor and its demand for far more power, the method for powering the microprocessors for our computers becomes an important issue. The requirements of the Voltage Regulator (VR/VRM) for the future generation of microprocessors can be summarized as [12]:

1) Low output voltage (1.0-1.8V),

2) High load current (more than 150A),

3) Stringent voltage regulation (<5%),

3) Fast transient response with a current slew rate higher than 2A/ns.

For a digitally controlled VRM, if the limit cycle oscillation occurs, the voltage regulation is very likely to fail; if large delay resides in the control loop, the dynamics of VR will be vitally hurted. Therefore, quantization and delay effects must be considered for the digitally controlled VRMs.

1.2.1 Quantization Effects

In the digitally controlled DC-DC converters, two quantizers co-exist in the feedback loop: the voltage ADC and DPWM. It is known that if the DPWM’s resolution is not high enough, the limit cycle oscillations will occur. Assume the voltage ADC’s resolution is $\Delta V_{ADC}$, and the DPWM’s resolution is $\Delta D$. When quantized duty cycle is sent to the power stage, the output voltage will also appear with the quantized values. Denote the output voltage’s resolution is $\Delta V_o$. For a buck converter, $\Delta V_o = V_{in} \cdot \Delta D$.

To illustrate the generation of the LCOs, two examples are given in Figure 1.4. If we have a DPWM with low resolution, which means $\Delta V_o > \Delta V_{ADC}$, there is no proper duty
cycle command which can control the output voltage to reside in the zero-error bin of the voltage ADC. Hence, the control will force duty cycle to oscillate to track the reference. This kind of oscillation is called limit cycle oscillation.

![Figure 1.4 Comparison of low DPWM resolution and high DPWM resolution](image)

(a) low DPWM resolution  
(b) high DPWM resolution

**Figure 1.4 Comparison of low DPWM resolution and high DPWM resolution**

However, if we have a DPWM with higher resolution, which means \( \Delta V_o < \Delta V_{ADC} \), at least one duty cycle command control the output voltage to reside in the zero-error bin of the voltage ADC. Therefore, there is no limit cycle oscillation for this case. Based on the similar analysis, [2] proposed the static necessary conditions for no-limit-cycle as:

\[
\Delta V_o < \Delta V_{ADC} \quad (1-3)
\]

For digitally controlled VRMs, LCOs are not desired since they may ruin the voltage regulation and enlarge the voltage ripple. Hence, a high resolution DPWM which can satisfy (1-3) is necessary.

### 1.2.2 Delay Effects

Delay effect is another concern for the digital controlled VRMs. There exist several types of delays in the digital feedback loop, including the ADC conversion delay, digital
compensator calculation delay, DPWM delay as well as some propagation delays, as shown in Figure 1.5.

Figure 1.5 Delays in digitally controlled VRMs

Delay in the feedback will slow down the dynamics performance of the converter.

Figure 1.6 gives a load dynamics comparison of two VRs to illustrate the importance of the delay: (a) shows the case of analog controlled VRMs and (b) shows the case of digitally controlled VRM with total delay equal to half of the switching period. For the two cases, the power stages are same.

It is clearly shown in Figure 1.6 that the delay will cause voltage spike during load transients to be much higher than that of analog (no delay) case. Therefore, how to accurately find the delay in the feedback loop and then how to do the controller design are necessary for the digitally controlled VRMs.
Chapter 1. Introduction

1.3 Thesis Objectives and Outline

The objective of this work is to study the quantization effects and delay effects of digital control for VRMs, so that a better understanding of DPWM and feedback design can be achieved. To achieve this objective, a high-resolution digital multi-phase duty cycle modulation method is proposed in detail; the complete small-signal model of the digitally controlled VRM is proposed and based on this model, the AVP design guideline is explored.

In the next chapter, a review of previous work about digital PWM methods will be firstly presented. Then in order to find a high resolution duty cycle methods for multi-phase VRMs, a digital multi-phase constant on-time modulation method is proposed. After that, the implementation issues and simulation as well as experiment results are presented.
In Chapter 3, the small signal signal models of digital VRMs are proposed. The analysis is based on the assumptions that DPWM is a double-edge modulation and the sampling instants are aligned with the middle of one phase’s off time. At first, the conversion and calculation delay is neglected. The focus of the modeling is on the small signal model of the current sampling methods and the DPWM delay. This model is valid for those digital controllers which have fast ADC and fast calculation capabilities. After that, the conversion and calculation delay are considered into the modeling. Two time periods, $T_{iff}$ and $T_{irs}$, are employed to describe the total delay effects in the control loop. The proposed model only includes one delay term and the value of this delay can be found through a pre-determined lookup table. Finally, the complete small signal model of the digital VRMs considering the conversion and calculation delay is proposed.

With the derived small signal models of digital VRMs, the design guideline for AVP control are presented in Chapter 4. The digital active-droop control is employed and it borrows the concept of constant output impedance control from the analog world. Two design examples are provided for the verification.

Chapter 5 is the summary of the thesis.

2.1 Introductions

One of the major challenges in digital control for DC-DC converters is to design a high resolution, high frequency DPWM to avoid limit cycle oscillations (LCOs) [1, 2, 13-17]. Figure 2.1 shows a typical voltage mode digitally controlled single phase buck converter. It is observed that two quantizers existing in the voltage feedback loop: the first one is the voltage analog-to-digital converters (ADC), which aims to transfer the analog error voltage $v_{err}$ to a digital signal $v_{err}[n]$, with the resolution of $\Delta V_{ADC}$. The second quantizer is the digital pulse-width-modulator (DPWM), which will turns the control signal $v_c[n]$ to the continuous duty cycle.

![Figure 2.1 Two quantizers exist in feedback loop of digitally controlled converters](image)

Figure 2.1 Two quantizers exist in feedback loop of digitally controlled converters
The DPWM's resolution is called $\Delta D$. When this discrete duty cycle signal outputs to the power stage, discrete command for the output voltage will be obtained, which means that the output voltage should be also quantized, which has a resolution of $\Delta V_o$. For buck converters,

$$\Delta V_o = V_{in} \cdot \Delta D$$  \hspace{1cm} (2-1)

As described above, two quantizers co-exist in the feedback loop, which might introduce limit cycle oscillations to the converter. In [2] and [18], the authors summarized the static necessary conditions for reduce the limit cycle oscillations, which is

$$\Delta V_o < \Delta V_{ADC}$$  \hspace{1cm} (2-2)

Hence, DPWM’s resolution should be higher than voltage ADC’s resolution to reduce LCOs. Many efforts are made to achieve high DPWM resolution [1, 2, 14-16, 19-26]. The counter-based DPWM is one common practice, which is shown in Figure 2.2.

(a) Structure of counter-based DPWM  \hspace{0.5cm} (b) Operation principle

Figure 2.2 Counter-based DPWM

Counter-based DPWM usually consists of an $N$-bit digital counter and a digital comparator. With the system clock input, the counter will count the number of clocks for one switching period, and build the “ramp”, whose concept is widely adopted by industry
in analog control. When the ramp intersects with the control signal \( v_c[n] \), which comes from the digital compensator, the digital comparator will output the duty cycle signal, as shown in Figure 2.2 (b). According to this concept, the duty cycle for counter-based DPWM can be written as:

\[
D = \frac{m \cdot T_{clk}}{n \cdot T_{clk}} = \frac{m}{n}
\]  

(2-3)

where \( D \) indicates duty cycle value, \( T_{clk} \) is system clock period, \( m \) and \( n \) represent the number of clocks for on time \( (T_{on}) \) and switching period \( (T_{sw}) \).

The DPWM resolution is referred to the smallest step between two adjacent duty cycle values [16]. With the counter-based DPWM, \( \Delta D \) is

\[
\Delta D = \frac{T_{clk}}{T_{sw}} = \frac{1}{n}
\]  

(2-4)

Hence, \( \Delta D \) for counter-based DPWM is determined by the ratio between \( T_{clk} \) and \( T_{sw} \), which means with given \( T_{sw} \), in order to obtain high DPWM resolution, system clock frequency needs to be much higher. The requirements for system clock in VR application are summarized in Figure 2.3.

For VR application, output voltage resolution is normally selected to be 3mV due to the DC regulation tolerance. With this value, \( \Delta D \) at least should be 0.025\%, which can be calculated by (2.1). This is shown in Figure 2.3 (a). Then, in order to achieve this DPWM resolution, requirements for system clock with different switching frequency can be found in Figure 2.3 (b) or (2.4). For example, if \( F_{sw} = 300\text{kHz} \), which is the mainstream design for state-of-the-art VR, \( F_{clk} \) should be higher than 1.2GHz. If \( F_{sw} \) is further pushed to 1MHz, \( F_{clk} \) needs to be as high as 4GHz. Such high system clock is not feasible for
practical implementation due to large power consumption[16]. Therefore, there is a demand for new DPWM schemes which can lower down the requirement for system clock frequency.

![Figure 2.3](image)

**Figure 2.3** Requirements for system clock in VR application. (a) relationship between $\Delta D$ and $\Delta V_o$; (b) relationship between $\Delta D$ and $F_{\text{clock}}$.

### 2.2 Review of Digital Duty Cycle Modulation Schemes

Because of the aforementioned unacceptable system clock frequency issues for digitally controlled VR application, many new DPWM schemes are proposed to solve this problem. Generally speaking, there are two schemes to improve the DPWM resolution, one is from hardware improvement, which utilizes delay line technique to directly improve the resolution [16, 19-21]; the other is by means for pre-processing duty cycle command to increase the effective DPWM resolution, which includes digital dithering method[2], $\Sigma$-$\Delta$ modulation, digital constant on-time modulation as well as the digital nearly constant frequency modulation [27]. In the following part, a brief introduction of these DPWM methods will be reviewed.
2.2.1 Review of Hybrid DPWM

One way to increase the DPWM resolution while avoiding ultra-high system clock frequency is utilizing the techniques of delay line as depicted in Figure 2.4.

![Figure 2.4 Delay-line DPWM](image)

This circuit takes advantage of the linear propagation of a given pulse from the system clock through the delay cells connected in cascade, to select a given pulse width quantized as a function of the selected number of cells [16]. A signal will take a finite time to pass through each component, so by tapping their individual outputs to the inputs of a multiplexer it is possible to choose an amount by which to delay the signal. A pulsewidth modulated output may be generated by setting an SR-latch high when a pulse enters the delay-line and low again when the pulse appears at the multiplexer output, having been delayed by an amount determined by the selected tap. This delay-line DPWM can greatly reduce the requirements for clock frequency but need much larger silicon area including the large number of delay cells and the multiplexer.
Hybrid DPWM combines the merits of counter-based DPWM and delay line DPWM, shown in Figure 2.5, and requires a relatively low frequency system clock with a short delay-line and, thus, a reduced-area multiplexer.

For hybrid DPWM, the system clock will be sent to the counter as well as the delay line together, which is shown in Figure 2.5 (a). The counter counts the number of clocks of on time and the switching frequency, which provides a “rough” modulation for the on time and one switching period. Meanwhile delay line, which has a much smaller time slot ($t_{delay}$ in Figure 2.5 (b)), will provide the “fine” modulation for duty cycle. Assume that $n$ delay cells are cascaded to build a delay line, $t_{delay}$ is defined as:

$$t_{delay} = \frac{T_{clk}}{n}$$  \hspace{1cm} (2-5)
It is clearly shown in (2-5) that one system clock period is “divided” into $n$ smaller time slot. The DPWM resolution of hybrid DPWM is calculated as:

$$\Delta D = \frac{t_{\text{delay}}}{T_{\text{sw}}} = \frac{1}{n} \cdot \frac{T_{\text{clk}}}{T_{\text{sw}}}$$  \hspace{1cm} (2-6)$$

According to (2-6), with $n$ delay cells in one delay line, the DPWM resolution can be increased to $n$ times higher compared with counter-based DPWM.

Hybrid DPWM methods can be easily extended to multi-phase applications, such as VRMs[19]. In a $M$-phase paralleled converter, it usually needs $M$ identical sets of counter and delay lines to construct the DPWM, which requires large silicon area.

Faster system clock frequency will introduce larger power consumption, and more delay cells will occupy larger silicon area. Hence, in practical design, there is a trade-off between clock frequency and number of delay cells. Nevertheless, hybrid DPWM’s architecture is compact, power-efficient and can be used to easily implement multiphase PWM.

### 2.2.2 Review of Digital Dithering Methods

Digital dithering method is a pre-processing method to increase the effective resolution of a DPWM module without increasing the hardware resolution, which is proposed in [2]. Figure 2.6 gives an example of digital dither method for a single phase and 1-bit dither case.
In the top part of Figure 2.6, $V_{c1}$ and $V_{c2}$ are two adjacent control signal values, and $D_{c1}$ and $D_{c2}$ are corresponding duty cycles. Therefore, the DPWM resolution, $\Delta D$, is the difference of these two values. Note here that $D_{c1}$ and $D_{c2}$ are two hardware level duty cycles; hence $\Delta D$ is also the hardware level DPWM resolution. The bottom part of Figure 2.6 shows the concept of digital dithering. The control signal is purposely varying between two adjacent quantized duty cycle values, $D_{c1}$ and $D_{c2}$, every next switching period. Thus, an intermediate level can be implemented by averaging over two switching periods, resulting in an increase of the effective DPWM resolution by 2 times. For DC/DC converters, the averaging action is implemented by using an output filter. Ideally, if $n$-bit digital dithering is employed, $2^n$ times higher DPWM resolution can be achieved. However, the increasing DPWM resolution is not coming for free. Digital dithering method will introduce additional dithering ripple to the output voltage [2]. Figure 2.7 shows some simulation results with different type of digital dithering. It can been seen
from these figures, the more digital dither bits, the more severe low frequency output voltage ripple. Therefore, there is a trade-off between output voltage low frequency oscillation and DPWM resolution in the design of digital dithering methods.

![Digital Dither](image)

(a) No dither  
(b) 4-bit dither  
(c) 8-bit dither

**Figure 2.7 Digital dither introduces dithering ripple to output voltage**

Digital dithering method is also applicable to multi-phase case[2], as shown in Figure 2.8. For example, in a four-phase paralleled converter, Phase 1 is selected to be the master phase, and its duty cycle will follow the digital dither rule as illustrated above. For the other three phases, which are selected as salve phases, will follow the duty cycle type of the master one, and shift the phase by 90°, 180° and 270° respectively. Consequently, each phase’s DPWM resolution is certainly same with the master’s, which is higher than the conventional cases.
Figure 2.8 Multi-phase digital dithering method.

There still several issues with this type of multi-phase DPWM methods. At first, only master phase is modulating and all the others just track master’s duty cycle, which means that the equivalent sampling frequency for the whole system is equal to switching frequency. However, this is undesirable for a digital multi-phase converter, since it will introduce large delay and limit the bandwidth of the control loop. Moreover, the dithering ripple issues remain in multi-phase digital dithering methods.

Nevertheless, digital dithering method is still a good solution for digital multi-phase DC/DC converters when the dynamic requirement is not so stringent. Silicon Lab’s digital controller for DC/DC converters has this digital dithering feather.

2.2.3 Review of Digital Constant On-time Modulation Scheme (Method #1)

Voltage mode digital constant on-time modulation scheme [27] is a very simple but effective way to achieve high DPWM resolution with low system clock frequency, as shown in Figure 2.9.
In the method #1, \( m \) is constant while \( n \) is variable, and duty cycle is expressed by (2-3). The duty cycle resolution can be obtained from Figure 2.9, as:

\[
\Delta D = \frac{m}{n} - \frac{m}{n+1} = \frac{m}{n+1} \cdot \frac{1}{n} \approx D \cdot \frac{1}{n}
\]  
(2-7)

Comparing with constant frequency modulation, the smaller the duty cycle is, the higher the resolution for digital constant on-time modulation. Assuming \( F_{clk} = 150\text{MHz} \), \( F_{sw} = 300\text{KHz} \), duty cycle resolution comparison is shown in Figure 2.10.

![Figure 2.10 DPWM resolution comparison for Method #1](image-url)
For Voltage Regulation (VR) application, steady state duty cycle is around 0.1, which means that about 10 times improvement can be achieved by changing the modulation scheme with the same system clock frequency.

2.2.4 Review of Digital Nearly Constant Frequency Modulation Scheme

(Method #3)

The main drawback of Method #1 is the switching frequency variation. For different duty cycle values, the switching frequency is varying greatly, which is undesirable for magnetic design. To overcome this drawback, [27] proposed digital nearly constant frequency modulation method (Method #3). Figure 2.11 shows this modulation method.

With Method #3, duty cycle is still expressed by (1), but both $m$ and $n$ are variable: at first, change $m$ for coarse regulation; and then change $n$ for the fine regulation. The duty cycle resolution is same with Method #1, which is expressed by (3). Because there is only a small variation on variable $n$, the switching frequency is almost constant for different duty cycle values.
2.3 Proposed Multi-phase Digital Duty Cycle Modulation Schemes

The previous section provides the review of current DPWM modulation methods which can reduce the demand for ultra-high system clock frequency requirement. For state-of-the-art VR design, most of the industry products use multi-phase buck converter as the main circuit. Therefore, finding a suitable digital PWM method is one of the key technologies to build successful digitally controlled VRMs. For hybrid DWPM method, multi-phase converters need identical delay line for each phase, which will occupy large silicon area; for digital dithering method, multi-phase dithering suffers the sampling frequency and the control bandwidth, which is unacceptable for VR application. Digital constant on-time and nearly constant frequency modulation methods might be good solutions. But whether it can be extended to multi-phase case is questionable. In the following sections, the novel digital multi-phase constant on-time modulation method are presented and discussed.

2.3.1 Issues with Multi-phase Implementation of Method #1 and #3

As mentioned in 2.2.3 and 2.2.4, digital constant on-time modulation (Method #1) and nearly constant frequency modulation (Method #3) can improve the duty cycle resolution in single phase converter case. To make them applicable for VR application, multi-phase operation is needed. However, when we directly extend them to multi-phase case, the resolution is varying with different phase numbers. Here, we take Method #1 as an example to illustrate this issue. Figure 2.12 shows one implementation of digital constant on-time modulation method for 2-phase case.
In Figure 2.12 (a), a total PWM signal, \( g_{\text{tot}} \), is generated by comparing duty cycle command \( V_c[n] \) with the digital ramp. Notice that here the frequency of the digital ramp is twice of each phase switching frequency, that is, the period for \( g_{\text{tot}} \) is \( kT_{\text{clk}} \), and the switching period for \( g_1 \) and \( g_2 \) is \( 2kT_{\text{clk}} \). The total PWM signal is then distributed into two phase as phase PWM signal. The phase PWM duty cycle in this case, \( D_1 \), is calculated as:

\[
D_1 = \frac{m \cdot T_{\text{clk}}}{2k \cdot T_{\text{clk}}} = \frac{m}{n}, n = 2k
\]  

(2-8)
Where, \( m \) and \( n \) represents the number of clocks for on time and switching period for one phase. Figure 2.12(b) shows the case of duty cycle command is \( V_c[n]+1 \), which is the adjacent value of \( V_c[n] \). In this situation, the phase duty cycle is:

\[
D_2 = \frac{m \cdot T_{clk}}{2(k+1) \cdot T_{clk}} = \frac{m}{n+2}, n = 2k
\]  

(2-9)

Hence, the duty cycle resolution of phase PWM signal is the difference of \( D_1 \) and \( D_2 \), as:

\[
\Delta D = D_1 - D_2 = \frac{m}{2 \cdot k} - \frac{m}{2 \cdot (k+1)} \approx D \cdot \frac{1}{k} = 2 \cdot \frac{D}{n}
\]

(2-10)

Comparing (2-10) and (2-7), it is found that with 2 phases interleaving, each phase’s duty cycle resolution is decreased by two times. This phenomenon can also be understood by Figure 2.13. The horizontal axis is the available control signal values, and the dots represent the corresponding discrete duty cycle values. Let us take 2-phase as an example, as shown in Figure 2.13 (b), it is clear that with quantized \( V_c \) values, the quantization level of duty cycles is larger than that of single phase case. This is due to lacking of the intermediate duty cycle levels, for example \( m/(n\pm1) \), \( m/(n\pm3) \)…. If more phases are interleaved, more intermediate duty cycle levels will be lost, and the duty cycle resolution will be more suffered, as shown in Figure 2.13 (c) and (d).
A summary of the relationships of duty cycle resolution and the phase number for constant switching frequency modulation and constant on-time modulation is shown in Figure 2.14. The comparison is based on VR application with steady state $D$ is equal to 0.1. Considering state-of-the-art VR design with phase number from 3 to 6, constant on-time modulation can only achieve 1.5 to 3 times higher duty cycle resolution. Hence, there is little benefit for applying Method #1 for VR application.
2.3.2 Proposed Digital Multi-phase Constant On-time Modulation

As discussed in previous section, multi-phase operation of constant on-time modulation has lower duty cycle resolution compared with single phase case. This is because that multi-phase operation will lose the minimum quantized duty cycles which can be obtained by single phase. To solve this issue, a novel digital multi-phase constant on-time modulation method is proposed. The basic concept of proposed method is to use some mechanism to recover these missing duty cycles for multi-phase operation to achieve the same duty cycle resolution with the single phase case. Figure 2.15 gives a 2-phase example to illustrate the proposed concept: (a) shows the constant on time modulation and (b) shows the proposed method.

Figure 2.14 Duty cycle resolution comparison between constant frequency and constant on time modulation schemes

Duty Cycle Resolution Vs. Phase Number

\[ \Delta D \]

Constant Fsw Modulation

Constant Ton Modulation

Phase Number

1  2  3  4  5  6  7  8
In Figure 2.15 (b), the round dots represent the original duty cycles of constant on-time modulation, and the triangle dots represent the inserted duty cycle values. To note here, these inserted duty cycles are not arbitrarily selected, but can be obtained by single phase constant on-time modulation, for example \( m/(n\pm1) \), \( m/(n\pm3) \). With the inserted duty cycle values, the duty cycle resolution for the multi-phase constant on-time modulation is increased to be \( D_1*1/n \), as shown in Figure 2.15 (b). In order to get these inserted duty cycle values, some equivalent intermediate control signal values, \( V_c \pm 0.5 \), \( V_c \pm 1.5 \), ..., should be obtained.

The proposed method uses a “pseudo-dither” concept to achieve this goal. The principle of this method is illustrated in (b) \( D_2=m/(n+1), n=2k \).

Figure 2.16 (a) and (b). Here, we assume 2 phases are interleaved, and the duty cycle command is updating at rising edge of the total PWM signal, \( t_0, t_1, t_2 \). In Figure 2.16 (a) shows the situation in one steady state, which control signal is \( V_c[n] \). In this case, the phase’s duty cycle is defined as: \( D_1 = m/n, n=2k \). Then, in order to obtain the same duty cycle resolution with the single phase case, it is desired that \( D_1 \)’s adjacent duty cycle, \( D_2 \),
has a value of \( D_2 = m/(n+1) \). According to previous discussion, an equivalent intermediate level of control signal, \( V_c + 0.5 \), must be achieved. The proposed method here purposely makes the control signal to alternate between two adjacent quantized values, \( V_c[n] \) and \( V_c[n]+1 \), in each switching period, as shown in Figure 2.16 (b). Therefore, in the average sense, the intermediate level \( V_c[n]+0.5 \) is obtained.

With the proposed method, the duty cycle resolution for each phase is:
\[ \Delta D = D_1 - D_2 = \frac{m}{2k} - \frac{m}{2k+1} = \frac{m}{2k+1} \cdot \frac{1}{2k} \approx D \cdot \frac{1}{n} \]  

(2-11)

From (2-11), it is found by for 2-phase operation, the duty cycle resolution of proposed method is exactly same with single phase digital constant on-time modulation, which is expressed in (2-11). It means that with proposed multi-phase constant on-time modulation method, the duty cycle resolution is independent on phase number.

A comparison of proposed method with constant frequency modulation and constant on-time modulation is shown in Figure 2.17. The comparison is based on VR application with steady state \( D \) is equal to 0.1. It is shown that compared with constant frequency modulation methods, proposed method can achieve 10 times higher duty cycle resolution; compared with constant on-time modulation, the duty cycle resolution of proposed modulation method is independent on phase number, which makes it applicable for VR applicatoin.

![Duty Cycle Resolution Vs. Phase Number](image)

**Figure 2.17** Duty cycle resolution comparison of proposed method with constant frequency and constant on-time modulation
It is worthwhile to note here, the proposed method has a significant difference with the digital dithering method. For digital dithering method, the control signal is alternating over several switching periods, and duty cycle is also dithering from period to period. Moreover, a low frequency dithering ripple is introduced. However, with the proposed method, the control signal is alternating only within one switching period, and phase’s duty cycle is constant. Since there is no duty cycle dithering, no dither ripple is introduced to the converter.

2.3.3 Experiment Verification of Proposed Methods

A. Experiment Verification with Open Loop Operation

The proposed digital multi-phase constant on-time modulation is implemented on a prototype 2-phase digitally controlled buck converter. The controller is implemented by Xilinx Spartan II FPGA. The experiment parameters are as follows: $V_{in} = 12\text{V}$, $T_{on} = 0.33\mu\text{s}$, $F_{clk} = 150\text{MHz}$, $L_1 = L_2 = 2\mu\text{H}$ and $C = 3.9\text{mF}$.

In the open loop operation, the duty cycle is purposely changing continually with smallest step. Figure 2.18(a) shows the output voltage ($V_o$) with constant frequency modulation; (b) shows the case with constant on-time modulation, and (c) shows the case of proposed method. The output voltage resolution is defined as by (2-1).

The voltage resolution of for these three modulation methods are as:

- Constant frequency modulation: $\Delta V_o = 24\text{mV}$
- Constant on-time modulation: $\Delta V_o = 4.8\text{mV}$
- Proposed Method: $\Delta V_o = 2.4\text{mV}$
It can be observed that compared with constant frequency modulation method, digital constant on-time modulation without pseudo-dither method can achieve 5 times higher duty cycle resolution. With proposed method, the duty cycle resolution is 10 times higher than constant frequency case and will not change with phase number.

B. Experiment Verification with Closed Loop Operation

To verify the closed loop operation, a voltage ADC is employed as shown in Figure 2.1, with the resolution $\Delta V_{ADC}$ equals to 3mV, $F_{sample} = 600$kHz. In closed loop test, $L$ is selected to be 300nH, which is the common practice in VR application. The designed bandwidth is around 30kHz, the phase margin is 65 deg and gain margin is 10.2dB.

Output voltage resolution should be higher than ADC resolution to avoid limit cycle oscillations. With constant frequency modulation method, $\Delta V_o$ is equal to 24mV which is much larger than $\Delta V_{ADC}$, so there is severe limit cycle oscillation in the loop. Error! Reference source not found. (a) shows the output voltage of this case and the total voltage ripple is around 20.6mV. For digital constant on-time modulation, $\Delta V_o$ is improved to be...
4.8mV, but still larger than $\Delta V_{ADC}$, so LCOs can be observed at $V_o$. Error! Reference source not found. (b) shows this case and total voltage ripple is around 12.8mV. With proposed method, $\Delta V_o$ is improved to be 2.4mV, which is smaller than $\Delta V_{ADC}$. Therefore the limit cycle oscillation is greatly reduced as shown in Error! Reference source not found. (c).

![Figure 2.19 Closed loop experiment results: (a) constant frequency modulation, (b) digital constant on-time modulation and (c) proposed method.](image)

2.4 Summary

For digitally controlled VRMs, in order to avoid the limit cycle oscillations (LCOs), a high resolution Digital Pulse-Width-Modulator (DPWM) is required. However, designing such a DPWM requires ultra-high system clock frequency, which is impractical due to huge power consumption. Hybrid DPWM might be an alternative solution but will occupy large silicon area. Digital constant on-time modulation method is a good candidate to improve the DPWM resolution without much cost. However, directly extending this method to multi-phase application, which is the prevalent structure in VRMs application,
will introduce some issues. With more phase in parallel, the duty cycle resolution will drop more.

To solve the mentioned issue, this chapter proposed a multi-phase digital constant on-time modulation method. The proposed method will control the control voltage to alternate between two adjacent values, or dither, within one switching period. The outcome is that the phase duty cycle’s resolution is improved and independent on phase number. Compared with conventional constant frequency modulation method, the proposed method can achieve about 10 times higher duty cycle resolution for the VRM application. The effectiveness of the proposed method is verified by the simulation as well as the experiment results.
Chapter 3. Modeling of Digital VRMs

3.1 Introductions

Voltage Regulator (VR/VRM) for the future generation of microprocessors is a special Point of Load (POL) converter with high specifications: (1) low output voltage (1.0-1.8V), (2) high load current (more than 150A), (3) stringent voltage regulation (<5%) and (4) fast transient response with a load current slew rate higher than 2A/ns.

It can be expected that digital controllers will be increasingly used in low voltage, high-current and high frequency VRMs where conventional analog controllers are currently preferred. This trend might be attributed to the prominent advantages of digital control: low cost, programmability, easy monitoring, system identification and ease to implement advanced control schemes. Several companies already released the commercial digital VR controllers, such as Volterra [28], Chil Semiconductors [29], Intersil, and Primarion [30].

To design a successful digitally controlled VRM, the delay effects should be carefully considered. It is well known that large delay in the control loop will greatly downgrade the dynamics performances. The modeling of the delay effects in a voltage mode digitally controlled DC/DC converter is reported in [3, 4, 6-10]. To use these models, it is necessary to know the accurate delay inside the loop, which is not very easy to be extracted by an ASIC chip. Moreover, to meet the VR specifications, Adaptive Voltage Positioning (AVP) control is required, which normally requires the current mode control. There is no existing model to describe a digitally controlled VRM with the AVP control. To better understand the delay effects and provide a complete design guideline for a
digitally controlled VRM, this chapter proposed the small signal model of the digital VRMs. This chapter is organized as following: at first, the conversion and calculation delay is neglected. The focus of the modeling is on the small signal model of the current sampling methods and the DPWM delay. This model is valid for those digital controllers which have fast ADC and fast calculation capabilities. After that, the conversion and calculation delay are considered into the modeling. Two time periods, $T_{iff}$ and $T_{irr}$, are employed to describe the total delay effects in the control loop. The proposed model only includes one delay term and the value of this delay can be found through a pre-determined lookup table. Finally, the complete small signal model of the digital VRMs considering the conversion and calculation delay is proposed.

### 3.2 Description of Digital VRMs’ Structure

In this work, Primarion’s $PX3538$ digital VR11.x controller is selected as the modeling target. A typical VR application with PX3538 is shown in Figure 3.1. The blocks inside the dashed box are in the digital controller. In the voltage feedback, there are an anti-aliasing filter, a voltage ADC, a ripple, a digital compensator and a DPWM. The anti-aliasing filter is to eliminate the frequency component up higher than half of the sampling frequency to avoid the aliasing phenomenon in the sampling [31]. The output voltage, $V_o$, will be subtract from a reference voltage, $V_{ref}$, to get the error voltage, $V_e$. $V_e$ will be then sent to voltage ADC to be transferred to the digital signals $v^*[n]$, which will be then used by the digital compensator. The sampling frequency for the voltage ADC is as:
\[ F_{sv} = 2 \cdot N \cdot F_{sw} \quad (3-1) \]

where \( F_{sw} \) is the switching frequency, \( N \) is phase number and \( F_{sv} \) is the sampling frequency of voltage ADC. (3-1) means that the error voltage will be sampled twice per phase’s switching period. The calculation frequency and DPWM’s updating frequency is equal to the sampling frequency of the voltage ADC.

Figure 3.1 Digital VRMs with PX3538

The control of current loop consists the current ADC, a gain block Ki, the digital compensator and the DPWM. The current sampling in Figure 3.1 works as this way: for each phase, the current will be sampled once per switching period and the sampling instant is fixed at the middle of OFF time. The sampling frequency for the current ADC is as:

\[ F_{siphase} = F_{sw} \quad (3-2) \]
where $F_{siphase}$ is the sampling frequency of current ADC. With this kind of current sampling method, the DC value of the phase current can be obtained. This information can be used for AVP control, current sharing control as well as the circuit overcurrent protection. Since all the phases are normally interleaved, which means the phase angle between the adjacent phases will be $360^\circ/N$, the sampling instants for all the phases in one switching period will be evenly distributed. And moreover, at each sampling point, only one phase’s current will be sampled at one sampling instant. A more detailed drawing of this current sampling method for 2-phase buck converter is shown in Figure 3.2.

![Figure 3.2 Current sampling principle (2-phase)](image-url)
To meet the loadline requirement of VR’s specifications, the load current’s information should be known. The total current current information \( i_*L \), is obtained by adding all sampled phases’ current at each sampling instant. Hence, the sampling frequency for \( i_*L \):

\[
F_{si} = N \cdot F_{sw}
\]  

(3-3)

where \( F_{si} \) is the sampling frequency for total load current and \( N \) is the phase number. Since at each sampling instant, only one phase’s current is sampled, and all the other phases’ currents are previously sampled values, \( i_*L \) will contains some “old” current information, which will appear as a delay effect in the feedback loop.

For the current loop, the calculation frequency and DPWM updating frequency will be aligned with the current sampling, which will be \( N*F_{sw} \).

### 3.3 Small Signal Model of Current Loop in Digital VRMs without \( T_{con} \) and \( T_{cal} \)

Before starting the derivation of the small signal model of the digital current loop, simplification of a digitally controlled multi-phase buck is performed. Based on description of the digital VRMs shown in Figure 3.1, all phases are assumed to be evenly interleaved. Meanwhile, all the phases identical, including the power stage and control blocks. Therefore, in the average sense, all the phases are equivalent. Then borrowing the concept from analog control, the small signal model of a multi-phase buck can be simplified to the small signal model of a single phase buck, as shown in Figure 3.3.
With the simplified model of Figure 3.3(b), the modeling objective is to find the transfer functions of current sampling (from $i_L$ to $i^*_L$) and DPWM from ($v^*_c$ to $d$). Note here, although the sampling frequency for each phase’s current is equal to switching frequency, the total sampling rate for load current which will be used for AVP control is equal to $N*F_{sw}$. Hence, during the simplification from multi-phase to single-phase, the sampling frequency for load current should be equal to $N*F_{sw}$, which is highlighted in Figure 3.3.
There are several assumptions for the current loop modeling:

- Voltage loop is open;
- Sampling instant for each phase’s current is at the middle of OFF time;
- Current ADC conversion time and calculation time is neglected;
- The non-linear effect of the quantization is neglected.

### 3.3.1 Small Signal Model of Current Sampling

The current sampling unit serves to transfer the analog current information to its digital form. As described in the previous section, digital VRMs samples the phases’ current and adding them together to obtain the load current. To illustrate this process clearly, a 2-phase example is given in Figure 3.4.

![Figure 3.4 Adding phase currents to obtain load current](image)
In Figure 3.4, \(i_{L1}\) and \(i_{L2}\) represent the analog phases’ currents; \(i^*_{L1}\) and \(i^*_{L2}\) represent the sampled phases’ currents; and \(i^*_L\) represent the sampled load current. In such a system, sampling frequency for \(i^*_{L1}\) and \(i^*_{L2}\) is \(F_{sw}\), while the sampling frequency for \(i^*_L\) is \(2*F_{sw}\), then how to describe the relationship between these two sampled signals is a problem. Laplace analysis is the general tool to analyze this kind of sampled-data system [31], but it is not straightforward to apply Laplace analysis to this sampling process due two sampling rate co-exist in the loop. To facility describing this sampling process, the interpolation method is applied to \(i^*_{L1}\) and \(i^*_{L2}\) to make its sampling frequency equal to \(i^*_L\)’s so that the classical Laplace analysis may apply. The detailed derivation is shown in Appendix I. Here only gives the final result of the transfer function of current sampling unit.

The transfer function from load current \(i_L(s)\) to the sampled load current \(i^*_L(s)\) in Laplace-domain is calculated as:

\[
G_{ad} (s) = \frac{i^*_L(s)}{i_L(s)} = \frac{1}{T_{sw}} \left(1 + e^{-sT_r}\right) = \frac{1}{2T_{si}} \left(1 + e^{-sT_r}\right) \tag{3-4}
\]

(3-4) describe the transfer function of the “current sampling” blocks in Figure 3.3 (b). It has a very straightforward and simple physical meaning: at each \(i^*_L\) sampling instant, the total sampled load current is the sum of one phase’s current from this instant and the other phase’s from previous sampling instant, which will include one sampling period delay. Therefore, the transfer function from \(i_L\) to \(i^*_L\) will contain a delay effect. Then replace that block with the derived transfer function, and obtain Figure 3.5.
All the derivations above are based on 2-phase case. It is easy to extend this modeling method for multi-phase case. For an \( N \)-phase buck converter, the current sampling’s transfer function is calculated as:

\[
G_{\text{add}}(s) = \frac{i_L^*(s)}{i_L(s)} = \frac{1}{T_{\text{sw}}} \left( 1 + e^{-sT_s} + e^{-s2T_s} + \cdots + e^{-s(N-1)T_s} \right)
\]

(3-5)

### 3.3.2 Small Signal Model of DPWM in Current Loop

Previous section discussed the delay effect in the current loop due to the current sampling function. Another delay effect in the current feedback loop is coming from the DPWM part, as shown in Figure 3.3(b). It is assumed that the sampling frequency for the total load current is equal to \( N \cdot F_{\text{sw}} \) for \( N \)-phase interleaved buck converters. Although the digital compensator and DPWM’s updating frequency is twice of that frequency, it is limited by the lowest sampling frequency in the system, which is still \( N \cdot F_{\text{sw}} \). Before the derivation for the DPWM’s transfer function, the assumptions for this analysis are clarified here:

- Voltage loop is open;
Sampling instant for each phase’s current is at the middle of OFF time and Current ADC conversion time and calculation time is neglected, hence the DPWM’s updating point is right at the middle of the OFF time.

The non-linear effect of the quantization is neglected.

To describe the working principle of DPWM, a 2-phase buck converter’s example is shown in Figure 3.6.

![Figure 3.6 DPWM for a 2-phase buck converter](image)

For each phase, the control voltage, $v^*_c$, will be updated twice in one switching period. Since the two phases’ ramps are 180° interleaved, meanwhile the updating instants are also 180° interleaved and aligned with the ramps, the two phases are perfect symmetrical. Therefore, in the average sense, there is no difference for all the phases. Actually, the 2-phase buck converter working in this style is exactly equivalent to a single-phase buck converter with DPWM’s updating frequency equal to $2 \cdot F_{sw}$, as shown in Figure 3.7.
In such a single phase buck converter, the sampling frequency and DPWM’s updating frequency are equal to $2 \cdot F_{sw}$. The updating instants are evenly distributed in one switching period and aligned with the ramp.

There are several literatures talking about the modeling of a single phase buck converter with multiple sampling frequencies [3-5, 7-10]. Also, the quantization effects are neglected. Here, a brief introduction of this modeling method is presented.

To investigate the transfer function of the DPWM, an equivalent circuit is built, as shown in Figure 3.8 and the key waveforms are shown in Figure 3.9.
The input of the modulator $v_c(t)$ is separated into a steady part $V_c$ and a perturbation $\hat{v}_c(t)$, or

$$v_c(t) = V_c + \hat{v}_c(t)$$  \hspace{1cm} (3-6)

This input is sampled at the sample frequency $F_{si}=2F_{sw}$ and then divided into two subseries with the sampling frequency of $F_{sw}$:

$$\begin{align*}
\hat{v}_{c1}(t) &= \sum_{n=-\infty}^{+\infty} \hat{v}_{c1}(nT_s) \delta(t - nT_{sw}) \\
\hat{v}_{c2}(t) &= \sum_{n=-\infty}^{+\infty} \hat{v}_{c2}(nT_s) \delta(t - nT_{sw} - T_s)
\end{align*}$$  \hspace{1cm} (3-7)

Figure 3.9 Key waveforms of a uniform-sampled pulse-width-modulator
The response of the modulator to these separate subseries is different. If we consider an impulse in the first subseries at time zero:

$$\hat{v}_{c_1}(t) = \hat{v}_{c_1}(t) \cdot \delta(t)$$  \hspace{1cm} (3-8)

The response of the modulator can be approximated by an impulse:

$$\hat{d}_1(t) = \hat{v}_{c_1}(t) \cdot T_s \delta(t - T_{1r})$$  \hspace{1cm} (3-9)

where $T_{1r}$ is defined the period from the sampling instant to the rising edge of the duty cycle. In steady state, $T_{1r} = 1/2(1-D) \cdot T_{sw}$.

An impulse in the second subseries:

$$\hat{v}_{c_2}(t) = \hat{v}_{c_2}(t) \cdot \delta(t)$$  \hspace{1cm} (3-10)

yields approximately the output:

$$\hat{d}_2(t) = \hat{v}_{c_2}(t) \cdot T_s \delta(t - T_{1f})$$  \hspace{1cm} (3-11)

where $T_{1f}$ is defined the period from the sampling instant to the falling edge of the duty cycle. In steady state, $T_{1f} = 1/2D \cdot T_{sw}$.

By considering the above, the output of the double edge modulator can be expressed in the Laplace domain as

$$\hat{d}(s) = \hat{d}_1(s) + \hat{d}_2(s) = T_s \left( e^{-sT_{1r}} v^*_{c_1}(s) + e^{-sT_{1f}} v^*_{c_2}(s) \right)$$  \hspace{1cm} (3-12)

Now consider the input signals in the Laplace domain. Based on the theory of sample-data system, the input signals can be represented as:
\[
\begin{align*}
\dot{v}_c^*(s) &= \frac{1}{T_{sw}} \sum_{k=-\infty}^{\infty} \hat{v}_c(s-jk\omega_{sw}) \\
\ddot{v}_c^*(s) &= \frac{1}{T_{sw}} \sum_{k=-\infty}^{\infty} e^{-jk\omega_{sw}T} \hat{v}_c(s-jk\omega_{sw})
\end{align*}
\]  
(3-13)

Substituting (3-33) into (3-32) yields:

\[
\hat{d}(s) = \frac{1}{2} e^{-sT_{1r}} \sum_{k=-\infty}^{\infty} \hat{v}_c(s-jk\omega_{sw}) + \frac{1}{2} e^{-sT_{1f}} \sum_{k=-\infty}^{\infty} (-1)^k \hat{v}_c(s-jk\omega_{sw})
\]  
(3-14)

For DC-DC converters, the frequency considered is about up to half of the switching frequency. Hence, if considering limit to Nyquist frequency, (3-34) can be re-written as:

\[
\hat{d}(s) = \frac{1}{2} e^{-sT_{1r}} \hat{v}_c(s) + \frac{1}{2} e^{-sT_{1f}} \hat{v}_c(s)
\]  
(3-15)

\(\hat{v}_c(s)\) is the virtual analog signal and does not exist in the digital controlled converters. Instead, \(\hat{v}_c^*(s)\) is considered. Based on theory of sample-data system, \(\hat{v}_c^*(s)\) has a relationship with \(\hat{v}_c(s)\), as:

\[
\hat{v}_c^*(s) = \frac{1}{T_{si}} \hat{v}_c(s)
\]  
(3-16)

Substituting (3-36) into (3-35) and moving \(\hat{v}_c^*(s)\) to the left side of the equation yields the DPWM transfer function:

\[
G_{DPWM}(s) = \frac{\hat{d}(s)}{\hat{v}_c^*(s)} = \frac{T_{si}}{2} \left( e^{-sT_{1f}} + e^{-sT_{1r}} \right)
\]  
(3-17)

The DPWM function is an average of two delays, \(T_{1f}\) and \(T_{1r}\), but its exact physical meaning is not straightforward. Eular equation can be used to replace the exponential term.
to give a more clear understanding of the delay term. The expression of Euler equation is as:

\[ e^{j\omega t} = \cos(\omega T) + j \cdot \sin(\omega T) \]  

(3-18)

where \( \omega \) is the radian frequency and has a relationship with \( s \) in the Laplace-domain as: \( s = j \cdot \omega \). Combining with (3-38) and (3-37) generates:

\[ G_{DPWM}(j\omega) = \cos\left(\frac{\omega(1/2 - D)T_{si}}{2}\right) \angle \left(-\omega \frac{T_{si}}{2}\right) \]  

(3-19)

(3-39) reveals the physical meaning of the transfer function of DPWM. The gain varies with the frequency with a cosine function, and phase angle varies with the frequency with a linear relationship. For the low frequency range (up to \( \frac{1}{2}F_{sw} \)), (3-37) can be simplified as:

\[ G_{DPWM}(s) = \frac{\hat{d}(s)}{\hat{v}_c(s)} \approx T_{si} \cdot e^{-\frac{T_{si}}{2}} \]  

(3-20)

Here, the \( G_{DPWM}(s) \) is simplified to a constant gain with a delay. This delay is dependent on duty cycle and is fixed at \( T_{si}/2 \). All the derivation above is for single phase double edge modulator with sampling frequency equal to \( 2F_{sw} \). It is necessary to extend this model to multiple sampling cases. A double-edge DPWM with sampling frequency equal to \( 3F_{sw} \) is shown in Figure 3.10 with different duty cycles. Table 3-1 shows the \( T_{ir} \) and \( T_{if} \) values under different duty cycle conditions.
Figure 3.10 DPWM with sampling frequency equal to $3F_{sw}$.

Table 3-1 $T_{1f}$ and $T_{1r}$ values for DPWM with $3F_{sw}$

<table>
<thead>
<tr>
<th>$D$</th>
<th>$T_{1r}$</th>
<th>$T_{1f}$</th>
<th>$T_{1r} + T_{1f}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0 \leq D &lt; 1/3$</td>
<td>$(1-D)T_{sw}/2-T_{si}$</td>
<td>$(1+D)T_{sw}/2-T_{si}$</td>
<td>$T_{si}$</td>
</tr>
<tr>
<td>$1/3 \leq D &lt; 2/3$</td>
<td>$(1-D)T_{sw}/2$</td>
<td>$DT_{sw}/2-T_{si}$</td>
<td>$T_{si}$</td>
</tr>
<tr>
<td>$2/3 \leq D &lt; 1$</td>
<td>$(1-D)T_{sw}/2$</td>
<td>$DT_{sw}/2-T_{si}$</td>
<td>$T_{si}$</td>
</tr>
</tbody>
</table>

It can be observed from Table 3-1, for different duty cycles, $T_{1f}$ and $T_{1r}$’s values are varying. This can be seen from Figure 3.10. However, the sum of these two periods is a constant value, equal to the sampling period, which is $1/3T_{sw}$ in this case. The same conclusion can be extended to DPWM with sampling frequency equal to $NF_{sw}$.

The derived DPWM transfer function is verified through the SIMPLIS simulation. The simulation setup for 2-phase case is shown in Figure 3.11.
In Figure 3.11, DPWM is simulated by sampling the control voltage with $2 \cdot F_{sw}$. Looking at the measurement of the transfer function from $v_c$ to $i_L$, it contains several parts, as:

$$
\frac{i_L(s)}{v_c(s)} = G_{ad}(s) \cdot G_{DPWM}(s)
$$

(3-21)

The simulation results are shown in Figure 3.12. It can be found the model is pretty accurate.
Figure 3.12 Simulation results of $i_L(s)/v_c(s)$
Previous sections derive the transfer functions of current sampling and the DPWM separately. Then the small signal model of complete digital current loop without conversion and calculation delay can be obtained, which is shown below:

![Figure 3.13 Small signal model of digital current loop without conversion and calculation delay](image)

where $F_m$ represents the modulation gain of the DPWM unit. There are two delay units inside the loop: one is from the current sampling and the other is coming from the DPWM.

### 3.4 Small Signal Model of Voltage Loop in Digital VRMs without $T_{con}$ and $T_{cal}$

The small signal model of the digital voltage loop can be derived similarly to that of the current loop. The block diagram of the digital voltage loop is shown in Figure 3.14.

![Figure 3.14 Block diagram of the digital voltage loop](image)
The voltage loop consists of the anti-aliasing filter, voltage ADC, the digital compensator as well as the double-edge DPWM. The key waveforms of the voltage loop (2-phase) are shown in Figure 3.15.

![Figure 3.15 Key waveforms of the voltage loop](image)

The sampling frequency for the output voltage is equal to $2*N*F_{sw}$, where $N$ is the phase number. This indicates the voltage ADC will take $2*N$ samples per phases’ voltage. Compared with the current loop, the voltage loop’s sampling frequency is twice that of the current loop. Another difference is that for the current loop, phase’s currents are sampled and then added to get the load current’s information, hence there is one sampling period ‘s delay in current sampling part. But for the voltage loop, the total voltage is sampled. Therefore, there is no such delay effects in the voltage sampling unit. Based on the
sampling theory and ignoring the non-linear quantization effects, the voltage ADC can be modeled as a pure gain, as:

$$\frac{v_c^*(s)}{v_e(s)} = \frac{1}{T_{sv}}$$  \hspace{1cm} (3-22)

where $T_{sv} = 1/(2\cdot N\cdot T_{sw})$.

The digital compensator’s calculation frequency and the DPWM’s updating frequency are also equal to $2\cdot N\cdot F_{sw}$.

The transfer function of DPWM can be derived similarly to the current loop case, which is shown in Figure 3.16.

![Figure 3.16DPWM operation of the voltage loop](image-url)
The DPWM operation principle is similar to the current loop. Hence, the transfer function is calculated as:

$$G_{DPWM}(s) = \frac{d(s)}{v_e(s)} = T_{sv} \frac{1}{2} \left(e^{-sT_{1r}} + e^{-sT_{1f}}\right)$$  \hfill (3-23)

Here, $T_{1f}$ and $T_{1r}$ are defined as the periods from the effective sampling instants to the falling edge and to the rising edge respectively. With different duty cycle values, expressions of $T_{1f}$ and $T_{1r}$ may vary, but the sum of these two is constant, as:

$$T_{1f} + T_{1r} = T_{sv} = \frac{T_{sw}}{N}$$  \hfill (3-24)

The DPWM transfer can be simplified as:

$$G_{DPWM}(s) = \frac{d(s)}{v_e(s)} \approx T_{sv}e^{-\frac{\tau_v}{2}} = T_{sv}e^{-\frac{\tau_{sw}}{2N}}$$  \hfill (3-25)

The DPWM delay in the voltage loop is approximately equal to half of the voltage loop sampling frequency, which is also $T_{sw}/2N$.

Considering about the transfer functions of the voltage ADC and the DPWM, the small signal model of the voltage loop is obtained as:

![Figure 3.17 Small signal model of digital voltage loop without conversion and calculation delay](image)

55
3.5 Complete Small Signal Model of Digital VRMs without \( T_{\text{con}} \) and \( T_{\text{cal}} \)

In previous sections, the small signal models of current loop and voltage loop are derived respectively. In a complete digital VRMs circuit, the two loops co-exist in the feedback control. The complete small signal model of the digital VRMs without conversion and calculation delay is obtained as shown in Figure 3.18.

![Figure 3.18 Complete small signal model of digital VRMs without \( T_{\text{con}} \) and \( T_{\text{cal}} \)](image)

Basically speaking, there are two sampling frequencies in the digital VRMs. The sampling frequency for the current loop is slower and the sampling frequency for the voltage loop is faster. Therefore, if ignoring the conversion and calculation delay, the DPWM delays for the two loops are different, even if the two loops share one DPWM.

3.6 Small Signal Model of Current Loop in Digital VRMs with \( T_{\text{con}} \) and \( T_{\text{cal}} \)

In previous three sections, the small signal model of the digital VRMs without the ADC’s conversion and digital compensator’s calculation delay is derived. This model is
valid for the applications where the switching frequency is relatively low while the digital controller’s speed is fast enough. In this case, with given sampling command for the ADC, the sampled value will be generated instaneo usly; with the sampled signals, the digital compensator update its control voltage also instaneously.

However, this is not always true for today’s most industry’s products. In most cases, the conversion time ($T_{con}$) and calculation time ($T_{cal}$) can not be neglected. With Primarion’s controller, the voltage ADC’s conversion time is about 42ns and the calculation time is even longer. For a 4-phase 1MHz buck VRM, steady state duty cycle is around 0.1, as shown in Figure 3.19. If $T_{con}$ and $T_{cal}$ are short enough, $t_3$’s information will be used to update the rising edge of the duty cycle and $t_4$’s will be used for the falling edge.

![Figure 3.19 Key waveforms of a 4-phase digital VRMs](image)

As defined in previous sections, $T_{1f}$ is only equal to half of the on time, which means 50ns. Therefore, considering $T_{con}$ and $T_{cal}$, it is very likely that $t_4$’s information will take more than 50ns to be converted to the control voltage, that will cause the falling edge will
be updated based on previous sampling instant’s information. To conclude, in current products of digital VRMs, $T_{con}$ and $T_{cal}$ should be considered into the model.

In the following three sections, the small signal model of the digital VRMs with $T_{con}$ and $T_{cal}$ will be derived. The structure of the digital VRM is same with Figure 3.1. Figure 3.20 gives the system diagram of this system considering $T_{con}$ and $T_{cal}$.

![Figure 3.20 System diagram of digital VRMs with $T_{con}$ and $T_{cal}$](image)

The key waveforms of the digital current loop are shown in Figure 3.21. With given sampling instant for each phase current, the ADC will take $T_{con}$ to finish the conversion. The sampled phase currents will be then added together to generate the total load current’s information. The digital compensator will take $T_{cal}$ to generate $v^*_c$ according to the sampled current and error voltage. Here, $T_{1f}$ and $T_{1r}$ represent the period from the control voltage, $v^*_c$, updating instant to the falling edge or rising edge.

Based on previous knowledge, the transfer functions of each block in the current loop can be obtained by Figure 3.21. The transfer function of the current sampling is:

$$G_{ad}(s) = \frac{i^*_L(s)}{i_L(s)} = \frac{1}{T_{si}} e^{-s(0.5T_{si} + T_{con})}$$

(3-26)
The current sampling’s delay contains two parts: one is from adding phase currents to get the load current; the other is a pure time delay coming from the conversion time.

The transfer function of the digital compensator containing calculation delay is:

$$\frac{v^*_c(s)}{i^*_L(s)} = e^{-sT_{cal}} \cdot K_i \cdot G_{PID}(s)$$  \hspace{1cm} (3-27)

The transfer function of the DPWM unit is:

$$\frac{d(s)}{v^*_c(s)} = F_m \cdot T_{sl} \cdot \frac{1}{2} \left( e^{-sT_{ff}} + e^{-sT_{rf}} \right) \approx F_m \cdot T_{sl} \cdot e^{-s0.5(T_{rf} + T_{ff})}$$  \hspace{1cm} (3-28)
The small signal model of the digital control with $T_{con}$ and $T_{cal}$ are reported in [4], which is shown in Figure 3.22.

![Diagram of the previous model of digital current loop with $T_{con}$ and $T_{cal}$](image)

**Figure 3.22** Previous model of digital current loop with $T_{con}$ and $T_{cal}$

To know the transfer function the DPWM, it is critical to know the exact values of $T_{1f}$ and $T_{1r}$. According to different phase number, duty cycle, $T_{con}$ and $T_{cal}$, $T_{1f}$ and $T_{1r}$ should be calculated for each case. The sum of $T_{1f}$ and $T_{1r}$ is no more a constant. To use this model, every time delay should be known accurately. However, most of the delay is inside the digital controller which is hard to obtain. Therefore, it is not easy to use this model for the design.

This work proposed a new method to model the digital current loop which has a straightforward and clear meaning and easy to use. At first, two new time periods are defined in Figure 3.21: $T_{1ff}$, which is from the falling edge of a duty cycle to its effective sampling instant and $T_{1rr}$, which is from the rising edge of a duty cycle to its effective sampling instant. The detailed expression of $T_{1ff}$ and $T_{1rr}$ are as:

$$T_{1ff} = T_{1f} + T_{con} + T_{cal}$$

$$T_{1rr} = T_{1r} + T_{con} + T_{cal}$$

Then, we can counts all the delay times in the digital current feedback loop, as:
It is found that the total delay inside the digital current loop contains two parts: one is \(0.5T_{si}\), which comes from the adding phases currents to get the load current; the other is the average of \(T_{1ff}\) and \(T_{1rr}\).

Therefore, the problem becomes simpler. To know the exact time delay in the current loop, it only needs to find the time period from falling edge, rising edge to their corresponding sampling instants, not constrained to exact value of \(T_{con}\) and \(T_{cal}\).

There are some fixed relationships between the sum of \(T_{1ff}\) and \(T_{1rr}\) and conversion and calculation time. Let us still use a 2-phase as an example here.

If \(T_{con}\) and \(T_{cal}\) are in the range of \([0, 0.5DT_{sw}]\) as shown in Figure 3.23, falling edge and rising edge are determined by their closed sampling instants.

\[
e^{-s(0.5T_{si}+T_{con})} \cdot e^{-sT_{cal}} \cdot e^{-s0.5(T_{1ff}+T_{1rr}-2T_{con}-2T_{cal})} = e^{-s0.5T_{si}} \cdot e^{-s0.5(T_{1ff}+T_{1rr})}
\] (3-31)

**Figure 3.23** \(T_{1ff}\) and \(T_{1rr}\) when \((T_{con}+T_{cal})<0.5DT_{sw}\)

In this case, \(T_{1ff}\) and \(T_{1rr}\) can be calculated as:
If $T_{con}$ and $T_{cal}$ are in the range of $[0.5DT_{sw}, 0.5(1-D)T_{sw}]$ as shown in Figure 3.24, rising edge is still determined by the closest sampling instant, but the falling edge has to be determined by previous sampling instant due to longer conversion and calculation time.

![Diagram](image)

**Figure 3.24 $T_{1ff}$ and $T_{2ff}$ when $0.5DT_{sw}<(T_{con}+T_{cal})<0.5(1-D)T_{sw}$**

In this case, $T_{1ff}$ and $T_{1rr}$ can be calculated as:

$$T_{1rr} = 0.5(1-D)T_{sw} \quad \text{and} \quad T_{1ff} = 0.5(1+D)T_{sw} \quad (3-33)$$

If $T_{con}$ and $T_{cal}$ are in the range of $[0.5(1-D)T_{sw}, 0.5(1+D)T_{sw}]$ as shown in Figure 3.25, rising edge can not be updated by its closed sampling instant because of the even longer conversion and calculation time, which means that $T_{1rr}$ will be increased by one sampling period. $T_{1ff}$ is same with previous case.
In this case, $T_{1ff}$ and $T_{1rr}$ can be calculated as:

$$T_{1rr} = 0.5(2 - D)T_{sw} \quad \text{and} \quad T_{1ff} = 0.5(1 + D)T_{sw}$$

(3-34)

Following the same methodology, $T_{1ff}$ and $T_{1rr}$ can be calculated under different $T_{con}$ and $T_{cal}$ cases. The results for the 2-phase and $D=0.1$ case are summarized in Table 3-2.

<table>
<thead>
<tr>
<th>$0 \leq T_c \leq T_1$</th>
<th>$T_{1ff}$</th>
<th>$T_{1rr}$</th>
<th>$T_{1ff} + T_{1rr}$</th>
<th>Total delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>($T_c = 0.5DT_{sw}$)</td>
<td>$0.5DT_{sw}$</td>
<td>$T_s - 0.5DT_{sw}$</td>
<td>$T_s$</td>
<td>$e^{-0.5T_s} \cdot e^{0.5(T_{1ff} + T_{1rr})}$</td>
</tr>
<tr>
<td>$T_1 \leq T_c \leq T_2$</td>
<td>$T_s + 0.5DT_{sw}$</td>
<td>$T_s - 0.5DT_{sw}$</td>
<td>$2T_s$</td>
<td>$e^{-0.5T_s} \cdot e^{T_s}$</td>
</tr>
<tr>
<td>($T_c = 0.5(1-D)T_{sw}$)</td>
<td>$T_s + 0.5DT_{sw}$</td>
<td>$2T_s - 0.5DT_{sw}$</td>
<td>$3T_s$</td>
<td>$e^{-0.5T_s} \cdot e^{1.5T_s}$</td>
</tr>
<tr>
<td>$T_2 \leq T_c \leq T_3$</td>
<td>$T_s + 0.5DT_{sw}$</td>
<td>$2T_s - 0.5DT_{sw}$</td>
<td>$4T_s$</td>
<td>$e^{-0.5T_s} \cdot e^{2T_s}$</td>
</tr>
<tr>
<td>($T_c = T_s + 0.5DT_{sw}$)</td>
<td>$2T_s + 0.5DT_{sw}$</td>
<td>$2T_s - 0.5DT_{sw}$</td>
<td>$k \cdot T_s$</td>
<td>$e^{-0.5T_s} \cdot e^{0.5kT_s}$</td>
</tr>
<tr>
<td>$T_3 \leq T_{con} + T_{cal} \leq T_4$</td>
<td>$2T_s + 0.5DT_{sw}$</td>
<td>$2T_s - 0.5DT_{sw}$</td>
<td>$4T_s$</td>
<td>$e^{-0.5T_s} \cdot e^{2T_s}$</td>
</tr>
</tbody>
</table>

$k = 1, 2, 3, \ldots$
where \( T_c = T_{cal} + T_{con} \). It can be found from Table 3-2 that:

when \( T_c \) is within one range, \( T_{iff} \) and \( T_{irr} \) are constant values and the sum of these two values is integral times of sampling period. Hence, the delay should be considered in the loop is \( 0.5kT_{si} \) plus the sampling delay, where \( k \) is integers.

When \( T_c \) is continuously increasing, the total delay in the loop is increasing discretely.

The relationship between the \( (T_{con} + T_{cal}) \) and the total delay in the loop can be represented graphically, as shown in Figure 3.27.

![Figure 3.26 Total delay in the current loop with different \((T_{con} + T_{cal})\)](image)

The horizontal axis is the normalized conversion and calculation time and vertical axis is the total delay in the loop. Based on this graph, the total delay considered in the loop model can be directly obtained from Figure 3.27.
Previous derivation is for the 2-phase case, and the similar conclusions can be applied for any phase application. The key waveforms for 3-phase and D = 0.1 case are in Figure 3.27 $T_{1ff}$ and $T_{2ff}$ for 3-phase case and the results are summarized in Table 3-3.

![Figure 3.27 $T_{1ff}$ and $T_{2ff}$ for 3-phase case](image)

\[
T_c = T_{cal} + T_{cons}, T_{si} = \frac{1}{3}T_{sw}, T_1 = 0.5T_{si} - 0.5DT_{sw}, T_2 = 0.5T_{si} + 0.5DT_{sw}, T_3 = T_{si}.
\]

Table 3-3 $T_{1ff}$ and $T_{1rr}$ for 3-phase and D= 0.1

<table>
<thead>
<tr>
<th>$0 \leq T_c \leq T_1$</th>
<th>$T_{1ff}$</th>
<th>$T_{1rr}$</th>
<th>$T_{1ff} + T_{1rr}$</th>
<th>Total delay</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$0.5T_{si} + 0.5DT_{sw}$</td>
<td>$0.5T_{si} - 0.5DT_{sw}$</td>
<td>$T_{si}$</td>
<td>$\eta \cdot T_{si}$</td>
</tr>
<tr>
<td>$T_1 \leq T_c \leq T_2$</td>
<td>$0.5T_{si} + 0.5DT_{sw}$</td>
<td>$1.5T_{si} - 0.5DT_{sw}$</td>
<td>$T_{si}$</td>
<td>$\eta \cdot T_{si}$</td>
</tr>
<tr>
<td>$T_2 \leq T_c \leq T_3$</td>
<td>$1.5T_{si} + 0.5DT_{sw}$</td>
<td>$1.5T_{si} - 0.5DT_{sw}$</td>
<td>$T_{si}$</td>
<td>$\eta \cdot T_{si}$</td>
</tr>
<tr>
<td></td>
<td>$\cdots$</td>
<td>$\cdots$</td>
<td>$\cdots$</td>
<td>$k \cdot T_{si}$</td>
</tr>
</tbody>
</table>

Based on the derivation above, the proposed small signal model of the digital current with conversion and calculation time is shown in Figure 3.28.
In the proposed model, the ADC conversion delay, digital compensator delay as well as the DPWM delay are lumped together as a single delay term. Then based on the range of the $T_{\text{con}} + T_{\text{cal}}$ values, the corresponding delay can be selected by Table 3-2 or Figure 3.26 to for the model.

**3.7 Small Signal Model of Voltage Loop in Digital VRMs with $T_{\text{con}}$ and $T_{\text{cal}}$**

Some literatures report the detailed small signal model of the digital voltage loop including the conversion and calculation time as shown in Figure 3.29. In this model, every delay term should be known to get the accurate model.

**Figure 3.28 Proposed small signal model of digital current loop with $T_{\text{con}}$ and $T_{\text{cal}}$**

**Figure 3.29 Previous small signal model of digital voltage loop with conversion and calculation delay**
It is not inconvenient to use this model since Tcon and Tcal are not easy to extract and \( T_{if} \) as well as \( T_{ir} \) need to be calculated based on previous values. Following the same derivation process of current loop, the small signal model of the digital voltage loop with conversion and calculation delay can be obtained, as shown in Figure 3.30.

\[
\text{Figure 3.30 Proposed small signal model of digital voltage loop with } T_{\text{con}} \text{ and } T_{\text{cal}}
\]

Compared with previous model, all the delays in the loop are lumped as one delay. This delay is discrete values with increasing of the conversion and calculation time.

\[
\text{Figure 3.31 Total delay in the voltage loop with different } (T_{\text{con}} + T_{\text{cal}})
\]
3.8 Complete Small Signal Model of Digital VRMs with $T_{con}$ and $T_{cal}$

In previous sections, the small signal models of current loop and voltage loop are derived respectively. In a complete digital VRMs circuit, the two loops co-exist in the feedback control. The complete small signal model of the digital VRMs shown in Figure 3.18, without conversion and calculation delay is obtained as shown in Figure 3.18.

![Figure 3.32 Complete small signal model of digital VRMs with $T_{con}$ and $T_{cal}$](image)

Basically speaking, there are two sampling frequencies in the digital VRMs. The sampling frequency for the current loop is slower and the sampling frequency for the voltage loop is faster. Therefore, if ignoring the conversion and calculation delay, the DPWM delays for the two loops are different, even if the two loops share one DPWM.
3.9 Summary

In a digitally controlled VRM, there are ADC conversion delay, digital compensator delay and the DPWM delay. The delays will introduce additional phase lag to the current loop and the voltage loop, which might give trouble for a successful VRM design. Therefore, modeling the delay effect in the loop is necessary.

In this chapter, a new small signal model of the digital VRMs is proposed. Firstly, the conversion and the calculation delay are assumed to be neglected. In this case, two delays are involved in the current loop. One delay comes from adding the sampled phase currents to get the sampled load currents. The other delay comes from the DPWM delay. The similar process is applied for the voltage loop. Therefore, a complete small signal model of digital VRMs is obtained.

After that, the conversion and calculation delay are considered into the modeling. Two time periods, $T_{iff}$ and $T_{ivr}$, are employed to describe the total delay effects in the control loop. It is observed that the total delay in the loop is integral times of sampling periods, which is never reported by any other literatures. Therefore, only one delay term will be included in control loop and the value can be found through a pre-determined lookup table. Finally, the complete small signal model of the digital VRMs considering the conversion and calculation delay is proposed.
Chapter 4. Design of Digitally Controlled VRMs

4.1 Introductions

In Chapter 3, a new small signal model of the digital VRMs with conversion and calculation time is proposed. In the proposed model, all the delay in the control loop will be lumped as one delay term which has discrete values according to different values of the conversion and calculation delays. In this chapter, the Adaptive Voltage Positioning design guideline of digital VRMs based on the proposed model is presented.

This chapter is organized as following: in section 4.2, a brief review of analog adaptive voltage positioning (AVP) control is introduced. The constant output impedance concept is employed to achieve AVP control. In section 4.3, the design guideline for digitally controlled VRMs is presented, which borrows the concept of the analog AVP control. Then in Section 4.4, two design examples are introduced. One example is the digitally controlled 4-phase buck VRM, with no conversion and calculation delays. The other example is digitally controlled 12V self-driven VRMs. In this example, the conversion and calculation delays are approximately equal to one fourth of the switching period. Then the experimental results are used to verify the design.

4.2 Review of Analog Adaptive Voltage Positioning Control

As a special power supply for the microprocessor, the VRM must maintain a low output voltage within a tight tolerance range during operation with a large current step change and high slew rate. To meet such transient requirements, the VRM must use many output capacitors, which increase its size and cost. To reduce the demand of capacitors,
Adaptive voltage position (AVP) is a necessary function for VRM control design. The basic idea to achieve AVP is to design the output impedance of the VRM to be a constant value\[32\]. Figure 4.1 shows the method of constant output impedance to achieve AVP, where $VID$ is determined by system $VID$ value, $R_{droop}$ is the droop resistor which is determined by Intel’s load line specification.

![Figure 4.1 Constant impedance for AVP](image)

Therefore, the static loadline specification is defined as:

$$V_o = VID - I_o \cdot R_{droop} \quad (4-1)$$

Figure 4.2 (a) and (b) show the steady state loadline requirement and the dynamic requirement for the AVP control of VRMs.
Active droop control is a good solution to achieve the constant output impedance design for VRMs [32]. Figure 4.3 shows the active-droop control concept. The inductor current information is sensed and fed back to adjust the output voltage reference according to the droop requirement. Larger current means smaller voltage reference. (As a result, this control method is also referred to as current-injection control.) Then, the feedback control forces the output voltage to follow the voltage reference. The infinite DC gain of the feedback compensator $A_v$ ensures that the values of the output voltage and the voltage
reference are equal. Since the output voltage droop is related to the output load current, it can be controlled perfectly.

![Figure 4.3 The concept of active-droop control](image)

Figure 4.3 clarifies the definitions of the output impedances for the active-droop control. $Z_{oi}$ is the output impedance of VRM with current loop closed while the voltage loop is open. $Z_{oc}$ is the output impedance with both current loop and voltage loop closed.

![Figure 4.4 Output impedance definitions of active-droop control](image)

Figure 4.4 clarifies the definitions of the output impedances for the active-droop control. $Z_{oi}$ is the output impedance of VRM with current loop closed while the voltage loop is open. $Z_{oc}$ is the output impedance with both current loop and voltage loop closed.

The control object is to make $Z_{oc}$ to be equal to $R_{droop}$. 
Figure 4.5 shows the small-signal block for active-droop control. $A_i$ represents the current-sensing function, and $A_v$ is the voltage-loop compensator transfer function. It is very clear that the active-droop control is a dual-loop feedback system. The current loop $T_i$, voltage loop $T_v$, and $T_2$ are defined as:

$$T_i = A_v \cdot F_m \cdot G_{id} \cdot A_i$$

(4-2)

$$T_v = A_v \cdot F_m \cdot G_{vd}$$

(4-3)

$$T_2 = \frac{T_v}{1 + T_i}$$

(4-4)

If the bandwith of the current loop is higher than that of the voltage loop, then within the current loop’s bandwidth, the inductor current can track the reference well, which means that the inductor can be treated as a ideal current source, as shown in Figure 4.6.
With current loop closed, $Z_{oi}$, is equal to the output impedance of the output capacitors, as:

$$Z_{oi} = \frac{1}{sC} + ESR = \frac{1 + s/\omega_{ESR}}{sC}$$  \hspace{1cm} (4-5)

Assume that all the output capacitors are ceramic capacitors, so the ESR zero is around MHz range, which is higher than the control loop bandwidth. The magnitude of $Z_{oi}$ is shown in Figure 4.7. The objective of the active-droop control is to shape $Z_{oc}$ to be equal to $R_{droop}$ up to the $T_2$ bandwidth. In Figure 4.7, it clear indicates that to achieve this goal, the magnitude of $T_2$ should be a straight line with the slope to be -20dB/decade. Moreover, the intersection point of $R_{droop}$ and $Z_{oi}$ is the desired $T_2$ bandwidth.
Assume a high bandwidth current loop is available, then (4-4) will become:

\[
T_2 = \frac{\omega_c}{s} \approx \frac{F_m \cdot G_{id}(s) \cdot A_v(s)}{F_m \cdot G_{id}(s) \cdot R_{droop} \cdot A_v(s)} \approx \frac{\omega_c}{s}
\]  

(4-6)

(4-6) indicates that with an \( A_v \) design enabling the high bandwidth current loop, the desired \( T_2 \) can be automatically obtained.

### 4.3 Design Guideline for Digitally Controlled VRMs

The digital active droop control is employed in the designed digital VRMs. Still borrowing the concept of analog control, the digital active-droop control is intended to achieve constant output impedance. To achieve this goal, a high bandwidth current loop design is required.

The design guidelines for the digital active-droop control are as:
Based on the phase number and steady state duty cycle as well as the worst case of 
\((T_{cal}+T_{con})\), select the corresponding delay for the current loop model. The delay can be 
found from the curves shown in Figure 3.26.

Select \(K_i = R_{droop}\). This is to guarantee the correct DC value to meet the loadline 
requirement.

Use a proper compensator to achieve the high bandwidth current loop design. 
Guarantee that the phase margin is larger than 60deg and gain margin is larger than 6dB. 
Normally, if the delay is larger than one switching period, a 3-pole 2-zero compensator is 
enough, as:

\[
A_p(s) = K \cdot \frac{(1+s/\omega_{z1}) \cdot (1+s/\omega_{z2})}{s \cdot (1+s/\omega_{p1}) \cdot (1+s/\omega_{p2})}
\]

Use bilinear transformation method to transfer the Laplace-domain \(A_v(s)\) to the 
discrete form. Then, the parameters of the discrete compensator are obtained.

4.4 Design Examples

In order to verify the model derived in Chapter 3 and the design guidelines proposed 
above, two design examples are given here.

4.4.1 Design Example 1

The first example is a digital VRM of 4-phase buck without conversion and 
calculation delay. The circuit is shown in Figure 4.8 and the parameters are summarized in 
Table 4-1.
Table 4-1 Parameters of the 4-phase digitally controlled VRM

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>12V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>1.2V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>700kHz</td>
</tr>
<tr>
<td>Voltage ADC sampling frequency</td>
<td>5.6MHz</td>
</tr>
<tr>
<td>Current ADC sampling frequency</td>
<td>2.8MHz</td>
</tr>
<tr>
<td>Rdroop</td>
<td>1mΩ</td>
</tr>
<tr>
<td>Inductor</td>
<td>100nH/phase</td>
</tr>
<tr>
<td>Capacitor</td>
<td>2mF</td>
</tr>
<tr>
<td>T_{con} + T_{cal}</td>
<td>0</td>
</tr>
<tr>
<td>Steady state Duty Cycle</td>
<td>0.1</td>
</tr>
<tr>
<td>Desired bandwidth f_c</td>
<td>1/(2π·Rdroop·C)</td>
</tr>
<tr>
<td></td>
<td>110kHz</td>
</tr>
</tbody>
</table>

The small signal model of this example is shown in Figure 4.9. In this example, the anti-aliasing filter as well as the ripple filter is neglected. Since there is no conversion or calculation delay, for the current loop, the total delay is 2\( T_{si} \), consists of \( T_{si}/2 \) for the DPWM delay and \( 3/2 T_{si} \) for the current sampling delay.
Based on the model of Figure 4.9, the current loop design result is shown in Figure 4.10. The bandwidth is 120kHz which is higher than $f_c$ and the phase margin is 70deg.

This design is verified by SIMPLIS simulation. Figure 4.11(a) shows the $T_2$ comparison between the model and the simulation results. The solid line is the model the the dashed line is the simulation result. It ban be found that the model is pretty accurate.
Figure 4.11(b) shows the time domain load transient waveforms. The simulation waveforms tell the with the proposed design guideline, the dynamics specifications can be satisfied.

(a) comparison of bode plot of T2  
(b) time domain load transient simulation

Figure 4.11 Simulation results of design for 4-phase digital VRM

4.4.2 Design Example 2

The second example is a digitally controlled 12V self-driven VRM. The circuit is shown in Figure 4.12 and the parameters are summarized in Table 4-2 Parameters of the digitally controlled 12V self-driven VRM.
Figure 4.12 Digitally controlled 12V self-driven VRM

(a) Circuit diagram of digitally controlled 12V self-driven VRM

(b) Picture of digitally controlled 12V self-driven VRM
### Table 4-2 Parameters of the digitally controlled 12V self-driven VRM

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>12V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>700kHz</td>
</tr>
<tr>
<td>Output voltage</td>
<td>1.2V</td>
</tr>
<tr>
<td>Voltage ADC sampling</td>
<td>5.6MHz</td>
</tr>
<tr>
<td>Current ADC sampling</td>
<td>2.8MHz</td>
</tr>
<tr>
<td>Rdroop</td>
<td>1.25mΩ</td>
</tr>
<tr>
<td>Inductor</td>
<td>60nH/phase</td>
</tr>
<tr>
<td>Capacitor</td>
<td>2mF</td>
</tr>
<tr>
<td>T_{con}+T_{cal}</td>
<td>300ns</td>
</tr>
<tr>
<td>Steady state Duty Cycle</td>
<td>0.4</td>
</tr>
<tr>
<td>Desired bandwidth $f_c$</td>
<td>$\frac{1}{2\pi \cdot R_{droop} \cdot C}$</td>
</tr>
<tr>
<td></td>
<td>90kHz</td>
</tr>
</tbody>
</table>

The 12V self-driven VRM is proposed in [33]. The operation principle of this circuit is similar to a 4-phase interleaved buck converter with steady state duty cycle equal to 0.4. Therefore, for simplicity, we can directly use a 4-phase buck converter’s small signal model for the design. The complete small signal model is shown in Figure 4.13. Based on 300ns conversion and calculation delay, the total delay considered in the loop model can be found in Figure 4.13.

![Figure 4.13 Small signal model of digitally controlled 12V self-driven VRM](image)
The conversion and calculation time is located at the star point in Figure 4.14. Therefore, according to this curve, the total delay for the current loop is around $0.7T_{sw}$. This value will be used for the loop design.

The design is verified by the experiment results. Figure 4.15 shows the $T_2$ comparisons between the model and the experiment results. Figure 4.16 shows the time domain load dynamics waveforms. The model matches the experiment measurements well. And also, the output voltage during the load transient can meet the VR 11.0 dynamic specifications.
BW = 144kHz
PM = 72deg

Solid lines: experiment results
Dashed lines: model

Figure 4.15 $T_2$ measurements of digitally controlled 12V self-driven VRM

Figure 4.16 Time domain waveforms of dynamic load change
4.5 **Summary**

AVP control is required by the current VRM’s specifications.

With the derived small signal models of digital VRMs, the design guideline for AVP control are presented in Chapter 4. The digital active-droop control is employed and it borrows the concept of constant output impedance control in the analog world. Two design examples are provided for the verification. The simulation and experimental results shows the validity of proposed models and design methods.
Chapter 5. Summary

It can be expected that digital controllers will be increasingly used in low voltage, high-current and high frequency voltage regulator modules (VRMs) where conventional analog controllers are currently preferred because of the cost and performance reasons. However, there are still remaining two significant challenges for the spread of the digital control techniques: quantization effects and the delay effects.

Quantization effects might introduce the limit cycle oscillations (LCOs) to the converter, which will generate the stability issues. Actually, LCOs can not be totally eliminated theoretically. One way to reduce the possibilities of LCOs is to design a high resolution Digital Pulse-Width-Modulator (DPWM). However, designing such a DPWM which can meet the requirements of VRMs application requires ultra-high system clock frequency, up to several GHz. Such high frequency is impractical due to huge power consumption. Hybrid DPWM might be an alternative solution but will occupy large silicon area. Digital constant on-time modulation method is a good candidate to improve the DPWM resolution without much cost. However, directly extending this method to multi-phase application, which is the prevalent structure in VRMs application, will introduce some issues. With more phase in parallel, the duty cycle resolution will drop more.

To solve the mentioned issue, this work proposed a multi-phase digital constant on-time modulation method. The proposed method will control the control voltage to alternate between two adjacent values, or dither, within one switching period. The outcome is that the phase duty cycle’s resolution is improved and independent on phase number. Compared with conventional constant frequency modulation method, the proposed method
can achieve about 10 times higher duty cycle resolution for the VRM application. The effectiveness of the proposed method is verified by the simulation as well as the experiment results.

Delay effect is another concern for the digital controlled VRMs. There exist several types of delays in the digital feedback loop, including the ADC conversion delay, digital compensator calculation delay, DPWM delay as well as some propagation delays. Usually these delays are inside the digital controller and it is hard to know the exact values. There are several papers talking about the small signal model of the voltage mode control. These models are only valid if all the delay terms are known exactly since each delay is considered separately. Actually, this process is not easy. Moreover, there is no literature talking about the complete small signal model of the digital VRMs. But based on the analysis of Chapter 3, different implementations of the sampling process will give different impacts to the loop.

In Chapter 3, the small signal signal models of digital VRMs are proposed. The analysis is based on the assumptions that DPWM is a double-edge modulation and the sampling instants are aligned with the middle of one phase’s off time. At first, the conversion and calculation delay is neglected. The focus of the modeling is on the small signal model of the current sampling methods and the DPWM delay. This model is valid for those digital controllers which have fast ADC and fast calculation capabilities. It is shown that even with a “fast” controller, the current sampling and DPWM might introduce some delay to the loop.

After that, the conversion and calculation delay are considered into the modeling. Two time periods, $T_{iff}$ and $T_{irr}$, are employed to describe the total delay effects in the
control loop. It is observed that the total delay in the loop is integral times of sampling periods, which is never reported by any other literatures. Therefore, only one delay term will be included in control loop and the value can be found through a pre-determined lookup table. Finally, the complete small signal model of the digital VRMs considering the conversion and calculation delay is proposed. This model is helpful for the researchers to find the delay effects in their control loop based on the range of the total physical delay in the controller.

With the derived small signal models of digital VRMs, the design guideline for AVP control are presented in Chapter 4. The digital active-droop control is employed and it borrows the concept of constant output impedance control in the analog world. Two design examples are provided for the verification. The simulation and experimental results shows the validity of proposed models and design methods.
Appendix I

In order to derive the small signal model of the current sampling unit which contains two different sampling rates, the interpolation method is employed, which is shown in Figure A.1 with 2-phase as an example.

![Interpolation method to describe current sampling process](image)

**Figure A.1 Interpolation method to describe current sampling process**

The interpolation method is a common tool in digital signal processing to increase the sampling frequency of a digital signal. In our application, we employ the interpolation
method to sampled phases’s current \( (i_{L1}^* \text{ and } i_{L2}^*) \) to increase its sampling frequency equal to that of \( i_L^* \).

Since \( i_L^* \)'s sampling frequency is twice of that of \( i_{L1}^* \) and \( i_{L2}^* \), we only need to add one zero point between two adjacent sampling instant of \( i_{L1}^* \) and \( i_{L2}^* \). In Figure A.1, \( i_{L1}^{**} \) and \( i_{L2}^{**} \) are the new signals after the interpolation. It is clearly shown that the sampling frequency for \( i_{L1}^{**} \) and \( i_{L2}^{**} \) is equal to that of \( i_L^* \).

Now, we can apply the classical z-transform analysis to the current sampling process.

The time domain expressions of the interpolated signals are calculated as:

\[
i_{L1}^{**}(nT_{si}) = \begin{cases} i_{L1}(t)\delta(t-nT_{si}) & n = 2k \\ 0 & n = 2k-1 \end{cases}
\] (A-1)

\[
i_{L2}^{**}(nT_{si}) = \begin{cases} 0 & n = 2k \\ i_{L2}(t)\delta(t-nT_{si}) & n = 2k-1 \end{cases}
\] (A-2)

Therefore, the total load current can be calculated by (A-1) and (A-2):

\[
i_L^*(n) = i_{L1}^{**}(n) + i_{L1}^{**}(n-1) + i_{L2}^{**}(n) + i_{L2}^{**}(n-1)
\] (A-3)

It can be seen from (A-3), \( i_L^*(n) \) can be described directly by the interpolated signals in the time domain with one single equation. Similarly, we can write the expression of sampled total load at \((n-1)T_{si}\) instant, as:

\[
i_L^*(n-1) = i_{L1}^{**}(n-1) + i_{L1}^{**}(n-2) + i_{L2}^{**}(n-1) + i_{L2}^{**}(n-2)
\] (A-4)

Then, the difference equation of \( i_L^* \) can be obtained by (A-3) and (A-4):

\[
i_L^*(n) - i_L^*(n-1) = i_{L1}^{**}(n) - i_{L1}^{**}(n-2) + i_{L2}^{**}(n) - i_{L2}^{**}(n-2)
\] (A-5)
The z-transformation of this difference equation is calculated as:

\[
i^*_L(z) - i^*_L(z) \cdot z^{-1} = i^{**}_{L1}(z) - i^{**}_{L1}(z) \cdot z^{-2} + i^{**}_{L2}(z) - i^{**}_{L2}(z) \cdot z^{-2}
\]  \hspace{1cm} (A-6)

Re-organize the equation of (A-6) and the following result is obtained:

\[
i^*_L(z) = \left(1 + z^{-1}\right)i^{**}_{L1}(z) + i^{**}_{L2}(z)
\]  \hspace{1cm} (A-7)

Equation (A-7) reveals the z-domain relationship between the re-sampled signals and the total sampled signals. \(z^j\) denotes a unit delay of a sampling period. It can be observed here that when adding the \(i^{**}_{L}\) signal to get \(i^*_L\), there is an average delay effect in it.

It is helpful to translate (A-7) into the Laplace-domain. Theoretically, the definition of \(z\) is:

\[
z = e^{sT_s}
\]  \hspace{1cm} (A-8)

where \(T_s\) denotes the sampling period. With this definition, (A-7) can be directly transferred into the \(S\)-domain equation as:

\[
i^*_L(s) = \left(1 + e^{-sT_s}\right)i^{**}_{L1}(s) + i^{**}_{L2}(s)
\]  \hspace{1cm} (A-9)

With Equation (A-9), the \(S\)-domain relationship between the two discrete signals is presented. However, (A-9) cannot be directly put in the loop model since the relationship between the interpolated signals and the analog original signal are not clear. The next step is to build a bridge between these two signals. Following the definition of the Laplace-transformation, \(i^{**}_{L1}(s)\) can be directly derived with the time domain expression (A-1), as:

\[
i^{**}_{L1}(s) = \int_{t=-\infty}^{\infty} i^{**}_{L1}(t)e^{-st} \, dt = \int_{t=-\infty}^{\infty} i_{L1}(t) \sum_{k=-\infty}^{\infty} \delta(t - 2kT_s)e^{-st} \, dt
\]  \hspace{1cm} (A-10)
According to the theory of a sample-data system [31], the impulse series can be rewritten in the form of Fourier series, as:

\[ i_{L1}^{**}(s) = \int_{t=-\infty}^{\infty} i_{L1}(t) \sum_{k=-\infty}^{\infty} \delta(t - 2kT) e^{-st} dt = \int_{t=-\infty}^{\infty} i_{L1}(t) \left( \frac{1}{T_{sw}} \sum_{n=-\infty}^{\infty} e^{-\frac{jn2\pi}{T_{sw}}} \right) e^{-st} dt \quad (A-11) \]

Where \( n \) is the order of harmonics of switching frequency \( F_{sw} \). Change the sequence of the integration and addition in (A-11) and the Laplace-transformation of \( i_{L1}^{**} \) can be obtained, as:

\[ i_{L1}^{**}(s) = \frac{1}{T_{sw}} \sum_{n=-\infty}^{\infty} i_{L1}(t) e^{-\frac{2\pi}{T_{sw}}} \left( s - \frac{jn2\pi}{T_{sw}} \right) dt = \frac{1}{T_{sw}} \sum_{n=-\infty}^{\infty} i_{L1}(s - jn\frac{2\pi}{T_{sw}}) \quad (A-12) \]

Similar derivation can be applied for phase 2’s interpolated current, \( i_{L2}^{**} \):

\[ i_{L2}^{**}(s) = \frac{1}{T_{sw}} \sum_{n=-\infty}^{\infty} i_{L2}(s - jn\frac{2\pi}{T_{sw}}) \quad (A-13) \]

(A-12) and (A-13) reveal the relationship of the interpolated phase’s currents and their original analog forms in the Laplace-domain. Note here that these equations are valid only for up to half of the sampling frequency [31]. According to the sample-data system’s theory, aliasing effects will take effects for frequency components higher than the Nyquist frequency. Moreover, for digitally controlled VRMs, crossover frequency of the voltage loop is much lower than this frequency, normally from 1/10 to 1/3 of the switching frequency. Hence, it is safe to limit (A-12) and (A-13) to Nyquist frequency, which will give:

\[ i_{L1}^{**}(s) \approx \frac{1}{T_{sw}} i_{L1}(s) \quad (A-14) \]
\[ i_{L2}(s) \approx \frac{1}{T_{sw}} i_{L2}(s) \]  
\[ (A-15) \]

Substituting (A-14) and (A-15) back into (A-9) and the relationship between the analog phase currents and sampled load current in Laplace-domain is achieved:

\[ i^*_L(s) = \frac{1}{T_{sw}} \left( 1 + e^{-st_{sw}} \right) (i_{L1}(s) + i_{L2}(s)) \]  
\[ (A-16) \]

For the multi-phase buck converters, the load current is obtained by adding all phase’s current, as:

\[ i_L(s) = i_{L1}(s) + i_{L2}(s) \]  
\[ (A-17) \]

Therefore, substitute (A-17) into (A-16) and move the \( i_L(s) \) to the left side of the equation, the transfer function from load current \( i_L(s) \) to the sampled load current \( i^*_L(s) \) in Laplace-domain is finally achieved:

\[ G_{add}(s) = \frac{i^*_L(s)}{i_L(s)} = \frac{1}{T_{sw}} \left( 1 + e^{-st_{sw}} \right) = \frac{1}{2T_{si}} \left( 1 + e^{-st_{sw}} \right) \]  
\[ (A-18) \]
References


