Chapter 1
Introduction

Today’s computing devices are capable of implementing more functions in a single chip, while the system designers are able to integrate more application chips into one single board than ever before. With the ever-increasing clock frequency, the microprocessor’s supply voltage is dropping quickly. Meanwhile, the requirement on the supply current is mounting at an unprecedented rate. The future supercomputer power system calls for 1.8V/1200A on board power modules; and the upcoming microprocessor power supply demands a voltage around 1.2V at a current of about 70A. The board space allocated for the power supply, however, has not increased.

The advancement of technologies in computing and communications has challenged power electronics researchers to develop a very high efficiency, extremely high density, and very low profile power module. An application example would be in an aircraft computing system, which has called for an isolated card-mounted power module with an ultimate size of 1.5” x 1.5” x 0.18” for 3.3V and 30A output. The most challenging design aspect is to achieve high power density and low profile along with very high efficiency, 90%, at the required output. The ultimate power density of this design is 300W/in³. The state-of-the-art high density power supply usually provides up to 40W/in³ and 80% efficiency. One of this kind of power supply employing Insulated Metal Substrate and surface mount components is able to provide 80% efficiency, 0.315” profile, and 20W/in³ power density for 3.3V/20A output. Another typical example using direct-bond-copper on a ceramic substrate packaging technique and bare dies can provide up to 78% efficiency, 0.4” profile, and 40W/in³ power density for 3.3V/20A output.

The two largest technical challenges presented in these applications are the contradictory requirements of high density and high efficiency. High efficiency for low voltage, high
current output applications requires the use of large synchronous rectifying MOSFETs and thick conductors. Lower switching frequency is preferred in order to minimize the switching loss in semiconductor devices, high frequency ac loss in the conductors, and power loss in the magnetic cores [D1, D3, D5, D6]. Lower switching frequency usually results in the larger magnetics and more capacitor devices for the conventional techniques. It is difficult to meet high density requirement. Therefore, the key technique in this type of applications is to achieve the small size of the magnetic device and capacitor device at relatively low switching frequency, as shown in Figure 1-1.

Figure 1-1 Technical challenges in designing high efficiency, high density, low voltage power supply

In the past, the integrated magnetic (IM) technique has been shown [B1-B20] to be able to reduce the size of the magnetics and capacitor without increasing switching frequency. The magnetic integration approaches presented in [B1, B2, B4, B5, B16, B17] utilize the voltage waveforms to derive the relationships between ac fluxes of different magnetic cores. The core integration is achieved based on the flux relationship. The overall size of the magnetic cores is reduced. However, most of these prior art IM techniques have neglected winding integration.

At high current output applications, the conduction loss in the output side windings is not negligible. A proper winding integration can significantly reduce the size and power loss in the windings, and simplify the fabrication complexity of the IM devices. The prior-art magnetic integration approaches [B1, B2, B4, B5, B16, B17] cannot readily achieve winding integration. Therefore, it is necessary to develop a new magnetic integration procedure, which is able to achieve the integration of both windings and cores.
As a result of applying this new magnetic integration procedure, several improved version of IM circuits are developed to meet the high efficiency, high density requirement for low voltage, high current output applications. Two typical circuits are shown in Figure 1-2 and Figure 1-3 [B20, C27]. As will be shown in Ch. 2, these circuits are the improved versions of the conventional current doubler rectifier circuits. Compared to the conventional current doubler rectifier circuit, an additional transformer N1:N2 is used. By properly designing the turns ratio of N1:N2, the voltage/current stress of the semiconductor devices are reduced and the practical input voltage range is increased [C27]. By applying the proposed magnetic integration procedure, the integrations of both cores and windings are achieved. The numbers of cores, windings, and high-current interconnections are minimized. The size and the power loss of the magnetic device are therefore reduced. The size of filter capacitor can also be minimized by the inherent ripple current cancellation technique.

The proposed techniques have achieved good experimental results in a number of applications. A typical example features a 3.3V/30A output power supply with an efficiency of 90%, a profile of 0.21”, and a power density of 130W/in³.
Figure 1-2 Proposed HB circuit with improved IM circuit [B20, C27], (a) improved HB current doubler circuit with wider duty cycle range, (b) IM structure
Figure 1-3 Circuit diagram of proposed Forward circuit with improved IM technique: (a) electrical circuit diagram, (b) IM circuit
1.1. Prior-Art and Related Work

In the past, much research effort has been spent to improve power density. The most active research activities in the 1980s and early 1990s involved the resonant converter technique and the soft-switching technique advocated by VPEC researchers [A1-A12]. This type of technique is devoted to reducing the switching loss of the semiconductor devices in an effort to alleviate the thermal stress of the semiconductor devices at high switching frequency operations. A power density of about 80W/in$^3$ was achieved for 5V/50W output [A9]. Another distinct effort is the IM technique [B1-B19]. This technique was intended to reduce the core size without increasing switching frequency. Synchronous rectification is proven to be a must technique for low voltage, high current output applications because it minimizes the conduction loss in the rectifiers.

1.1.1. Resonant Power Conversion and Soft-Switching

All the resonant power converters and soft-switching techniques require at least one extra resonant component (either a parasitic element or an external element) to discharge the voltage across the device before its turn-on [A3, A6, A7, A10, A11], or to divert its current to zero before its turn-off [A8, A12]. By doing so, the switching loss of the semiconductor devices can be minimized. The parasitic element is absorbed, making it easier for high frequency packaging. Since the switching loss is reduced, it is possible to switch the semiconductor devices at very high frequency. However, there are several limitations of this type of technique:

i. High voltage/current stress for the resonant power converters. For example, the technique used to achieve zero-voltage switching (ZVS) usually increases the current stresses of the main device as well.

ii. Under certain circumstances, the size increase caused by the extra resonant components, and sometimes by the additional auxiliary semiconductor devices may offset the size reduction of the filter due to increasing the switching frequency.

iii. The small resonant period required in the soft-switching technique usually causes a large “duty cycle loss” at high switching frequency. This happens, for example, in a
phase-shift PWM controlled full bridge converter, at high switching frequency. Sometimes, the resulting duty cycle range is not optimized for circuit operation (increased device voltage stress, ripple requirement, etc.).

1.1.2. Integrated Magnetic Technique

There are three types of core integration. The first type is to integrate the cores with the same ac flux. One well-known application example is the integrated magnetic Cuk converter [B1, B2], as shown in Figure 1-5. Since the voltage waveform on each inductor of the Cuk converter is almost identical, the ac fluxes of two inductors are the same if two inductor windings have the same number of turns. So two inductor cores can be integrated together. The overall size of the magnetic components is reduced without increasing the switching frequency. The power loss associated with cores is also decreased.

In an isolated Cuk converter, two inductors and the isolated transformer can be integrated into one magnetic structure, as shown in Figure 1-5. By implementing the ripple steering technique, the winding leakage inductance is utilized to reduce the size of the filter capacitor. The gaps in two outer legs are adjusted to achieve zero ripple currents on both the input and output terminals. However, the isolated Cuk converter is not suitable for high current, low voltage applications because a dc capacitor is present in the secondary-side high current path. The power dissipated in the ESR of the secondary-side dc blocking capacitor will lower the efficiency and degrade the reliability of the capacitor. Accurate control of winding leakage inductance may also increase the complexity of fabricating the magnetic devices.

The second type of core integration deals with the cores whose fluxes are linearly related. A typical example is the prior-art IM structure for current doubler rectifier circuit [B16, B17, C1, C4, C7], as shown in Figure 1-6. The current doubler rectifier is attractive in low voltage, high current applications because two filter inductors split the output load current. In some cases, the conduction loss in the secondary windings is reduced [C4]. More importantly, the ripple currents of two inductors are out of phase. The overall output ripple current is dramatically reduced, resulting in a small output filter capacitor.
As shown in Figure 1-6(a), transformer secondary voltage equals to the difference of two inductor voltages. By choosing \( N_{L1} = N_{L2} = N_s \), the ac fluxes in three magnetic components is linearly related:

\[
\phi_c = \phi_2 - \phi_1
\]

\textbf{Eq. 1-1}

Therefore, an E-core, with two outer legs hosting two inductor windings and the center post hosting two transformer windings, can be adopted to implement this magnetic structure, as shown in Figure 1-6(c). The IM technique provides a loss reduction in the magnetic materials. However, each core window has to contain three windings, the profile of the IM device is higher than that of the transformer in the discrete magnetic circuit. In order to utilize the self-driven synchronous rectification, the asymmetrical PWM duty cycle control is usually adopted for HB configuration. The practical input range of HB circuit using asymmetrical duty cycle control is relatively narrow.

Figure 1-7 shows the converter topology and its IM implementation as proposed by Bassett [B14]. This integrated magnetic technique represents the third type of core integration. Because the voltage waveforms of the transformer and inductor are not proportional, the ac fluxes of these two magnetic components cannot be the same. An additional core leg is needed to provide a path for the difference of two ac fluxes. As shown in Figure 1-7(c), the inductor winding is located on one outer leg and the transformer windings are located on the center post. It is noted that the transformer in this circuit must be gapped. The primary side conduction loss is, therefore, higher than the regular forward converter with active clamp. The similar magnetic integration approach can be applied to the regular forward converter [B4, B5].

Therefore, all of these magnetic integration techniques are intended for core integration. The winding integration has been neglected.
Figure 1-4 Cuk converter and its IM structure [B1, B2]
Figure 1-5  Isolated Cuk converter and its IM structure with ripple steering technique [B1, B2]
The dual-transformer circuit [B13, B19, C28]] is also suitable for high current application. This circuit employs two transformers with low magnetizing inductance. Each low magnetizing transformer device can function as an ideal transformer and an energy storage device. At one stage of steady state operation, one transformer device functions as an ideal transformer and releases its stored energy to the output at the same time, and the other device receives energy from the input source. The function of output filter inductance is therefore realized. Apparently, each transformer device in this circuit is already an integration of transformer and inductors in terms of functionality. Since the two transformers are identical, the manufacturing cost might be lowered and the thermal management simplified. A very low profile transformer design can be easily achieved. However, the overall footprint of the discrete magnetic devices is still large. To improve power density, the IM structure can be adopted [B13, B19]. Figure 1-8 shows the full-bridge type implementation [B19]. Figure 1-8(a) shows the discrete magnetic circuit, which features two identical transformers, each storing half of the energy to supply the output load. Figure 1-8(b) shows one implementation of two transformers on an E-core. By sharing the same core leg, the overall size of the magnetic devices is reduced. Since the two transformers are identical, \( N_{p1} = N_{p2} = N_p \). The primary side voltage is expressed as

\[
V_p = V_{p1} + V_{p2} = N_{p1} \frac{d\phi_1}{dt} + N_{p2} \frac{d\phi_2}{dt} = N_p \frac{d(\phi_1 + \phi_2)}{dt} = N_p \frac{d\phi_c}{dt} \tag{Eq. 1-2}
\]

Therefore, two primary side windings on the outer legs can be combined into a single winding and migrated to the center post. The integrated magnetic structure, shown in Figure 1-8(c), is obtained. Two outer legs of the E core in this circuit store the same amount of energy. When two outer leg windings have the same number of turns, the proposed IM structure shown in Figure 1-2 and Figure 1-3 appears to be the same as that shown in Figure 1-8(c). But the proposed IM circuit, as shown in Ch. 2, is derived from the current doubler circuit through a different magnetic integration procedure. The two outer legs in the proposed IM circuits do not store the same amount of energy. This difference will result in the different approaches of designing IM structure. In the proposed IM structure, the turns ratio of two outer leg windings is also adjusted to
implement the additional transformer N1:N2, as shown in Figure 1-2 and Figure 1-3. A proper choice of N1/N2 can reduce voltage stress and current stress in the semiconductor devices and extend the practical input voltage range. These features were not addressed in the prior art IM techniques for dual transformer circuits and current doubler rectifier circuit.

Figure 1-6 Current doubler rectifier and its integrated magnetics [B16, B17]
Figure 1-7 Bassett converter and its integrated magnetics structure (Ns=N_L) [B14]
Figure 1-8 Magnetically integrated full wave converter [B10]: (a) discrete full wave double transformer circuit, (b) one implementation of the magnetic devices, (c) IM structure when \( Np_1 = Np_2 = Np \), \(Ns_1 = Ns_2 = Ns\)

Most of these prior-art IM techniques focus only on core integration while neglecting the winding integration on the high current side. For low voltage, high current applications, a proper winding integration on the output side is becoming more important because the conduction loss is the dominant loss factor. The new magnetic integration procedure developed in this work will be able to achieve the winding integration.
1.1.3. Synchronous Rectification

Synchronous rectification is necessary when the output voltage is below 5V, because the voltage drop (0.3V) of the best Schottky diode takes an excessive percentage of the output voltage [C5, C11, C12, C15, C21, C23, C27]. The resulting conduction loss on the Schottky rectifiers has become unacceptable from the point of view of efficiency and thermal management of the individual device. The state-of-the-art low-voltage MOSFET can provide as low as 4 mohm on-resistance when it is properly driven. If the current stress on each device is below 30A, synchronous rectification using these low on-resistance MOSFETs always yields a performance superior to that of the Schottky diode.

![Figure 1-9 Comparisons of conduction power loss of Schottky diode and low-voltage MOSFET. Schottky: 85CN015, low-voltage MOSFET: SUP75N03-04](image)

An example is illustrated in Figure 1-9: 85CNQ015 is a 15V/80A Oring Schottky diode, and SUP75N03-04 is a 30V/75A, 4 mohm MOSFET. While the current rating is similar and the voltage rating is higher, SUP75N03-04 still dissipates less than half of the power of the best Schottky diode. For low-voltage, high-current applications, the high
Conduction loss in the Schottky rectifier diode makes it difficult to remove its heat. The poor efficiency caused by using the Schottky diodes also increases the thermal stress in the primary side semiconductor devices, the power components of the front-end converters (ac/dc, etc.), and the power distributing paths, because the input power of the low voltage power supply increases substantially. Therefore, using a Schottky diode may increase thermal stress on both the rectifier itself and the whole computing power system. Consequently, the synchronous rectification technique is a “must” technique for low voltage, high current output applications.

Usually, two synchronous rectifiers (SR) are arranged in the common-source configuration, as shown in Figure 1-11, to facilitate the gate driving design. Figure 1-11(a) shows the arrangement of SR in the two-inductor output circuit, while Figure 1-11(b) describes the case with the one-inductor circuit. The common part of these two cases is shadowed and redrawn in Figure 1-11(c). In the following discussion, the diagram shown in Figure 1-11(c) will be used to describe the different drive scheme of SR. There are two popular driving schemes for SR: external driving and direct self-driving, as shown in Figure 1-12 and Figure 1-13, respectively.

External driving is able to provide a proper driving voltage on the gate of SR. However, there are several self-defeating limitations in this circuit. Most SR are low voltage high current MOSFETs, which have excessively large gate capacitance. As shown in the recent survey of low voltage MOSFETs in Figure 1-10, lower $R_{ds,on}$ MOSFETs tend to have higher gate drive loss. Besides, most available MOSFET drivers are not able to provide the required driving current at high switching frequency. The external drive scheme also requires delicate control on the gate driving timing. To maximize the conduction time of the SR without losing ZVS and causing cross-conduction, the gate timing has to be very accurately controlled.

Therefore, the practical switching frequency when employing external driving is limited to about 30-40KHz. This relatively low switching frequency increases the size of the overall converter.
On Resistance vs. Gate Voltage
\( T = 25^\circ C, I_{ds} = 10A \)

![Graph showing on resistance vs. gate voltage](image)

Driving Loss vs. Gate Voltage (\( fs = 500KHz \))

![Graph showing driving loss vs. gate voltage](image)

Figure 1-10 Survey of Low Voltage MOSFETs (December 1997) (a) measured on-resistance, and (b) measured gate driving loss at different gate voltage
Figure 1-11 Common-source configuration of synchronous rectifiers (SR): (a) SR in a two-inductor output circuit, (b) SR in a one-inductor output circuit, (c) general diagram for common-source connected SR
The direct self-driving circuit [C5] shown in Figure 1-13 is simple. Because the body diode of the SR always conducts before the MOSFET portion, zero-voltage turn-on of SR is easily achieved. Most of the energy stored in the SR’s gate capacitor is recovered, the driving loss is minimized. Thus, the switching frequency for most of the silicon synchronous rectifiers using the direct self-driving technique can be pushed to around 500KHz. However, there are still some limitations of this technique.

i. It is only suitable for circuit topologies whose secondary voltage has only two states: positive and negative. For circuits whose transformer winding sees zero voltage during a certain interval of the switching period, e.g., two-switch forward, this technique is not suitable. Thus, in forward configuration, only an active-clamp reset scheme is suitable for applying this gate drive scheme; in HB circuits, only asymmetrical duty
cycle control is capable of implementing a direct self-driven synchronous rectification technique.

ii. It is unsuitable for very high and very low output voltage because the transformer secondary side voltage is out of range for driving the MOSFET gate. The output voltage range for applying this technique is usually limited to 2.5V~7.5V.

iii. There is no over-voltage protection on the SR’s gate. This may cause reliability problems.

iv. Modules with directly self-driven SRs cannot be paralleled. As shown in Figure 1-14, for example, if Module #2 is powered up before Module #1 during the start-up, the output bus voltage will be coupled into the gates of SR in Module #1, if Module #1 has not yet produced any driving waveform on the power transformer. When the output bus voltage is large enough, both SR in Module #1 will be biased on, resulting in a short circuit on the output side.

Parallel configuration is very important to high current applications, which may require thousands of amperes of current. Thus, the direct self-drive scheme is not the best scheme for many applications.

Figure 1-14 Module parallel operations
1.2. Outline of Work

The ultimate purpose of this work is to achieve a high density, high efficiency design for low voltage, high current output applications. The outline of this work is summarized as follows.

i. Develop an efficient and very high density IM circuit that is suitable for low voltage, high current applications (Ch. 2). The proposed IM technique should have an inherent ripple cancellation technique to achieve smaller capacitor size and must integrate windings and interconnections to reduce conduction loss. The proposed IM structure should also be simple and easy to manufacture. A new magnetic integration procedure, featuring both core integration and winding integration, is proposed to derive this new IM structure.

ii. Provide detailed analysis for the proposed IM circuits intended to optimize circuit performance (Ch. 3). The analysis will include dc characteristics, flux distribution and loss distribution within the IM structure, and the ripple cancellation technique.

iii. Give design guidelines for the low voltage IM circuits based on the analysis (Ch. 4). The core size selection and the optimization of the gate drive for SR will be discussed in detail. New synchronous rectification techniques are proposed to extend the self-driving SR technique to a wider range of output voltage and circuit topologies, including circuits whose transformer winding voltage has a zero state voltage in one portion of switching period. The proposed techniques must also provide over-voltage protection on the SR’s gates, and the capability to directly parallel modules.

iv. Present detailed design examples of applying the proposed low voltage IM circuits (Ch. 5), including a card-mounted hybrid power module for the aircraft distributed power system with a power density of 130W/in³, a profile of 0.21 inches, and an efficiency of 90% at 3.3V/30A output; a microprocessor power supply with an efficiency of 81-85% for 1.2-1.65V/70A output; and a node card with an efficiency of greater than 87% at 2.5V/35A for the space power distributed power system. The stability issue regarding module-parallel-operation is discussed.
v. Extend the IM technique to develop new circuit topologies for high output voltage or low output current application. (Ch. 6)

vi. Summarize the results of the work and propose new research areas to further improve power density and efficiency (Ch. 7).