Chapter 6

New Integrated Magnetic Circuits For Other Applications

So far, the discussion has focused on techniques to achieve high efficiency and high density for low voltage, high current output applications, for which HBI$^2$M and FI$^2$M circuits with single-turn secondary winding have proven to be among the best topologies. When the output voltage is higher than 5V or the output current is relatively low, the conduction loss in the secondary windings is not a dominant loss factor inside the magnetic structure. It might be desirable to use a multi-turn secondary winding. In these types of applications, the proposed HBI$^2$M and FI$^2$M circuits have some inherent limitations. A new integrated magnetic technique needs to be developed.

6.1. Limitations of previously proposed integrated magnetic circuits

The proposed integrated magnetic circuits (HBI$^2$M and FI$^2$M, shown in Figure 6-1) employ a three-leg, three-winding structure, with each leg hosting one winding. With single-turn secondary winding, these circuits are able to minimize the footprint and power loss of the magnetic devices. However, if multi-turn secondary windings are adopted, the implementation of PCB winding will give a large footprint, as shown in Figure 6-2(b) and (c). Besides, the leakage inductance of each winding increases approximately with the square of the number of turns of the secondary windings, as shown in Table 6-1. The large leakage inductance may cause large ringing on the secondary side rectifiers, decreasing the effective duty cycle and power conversion efficiency and aggravating the EMI problems.
Table 6-1 Leakage inductance (obtained by 2-D FEA simulation) associated with the turns number of the secondary winding (N=N_p/N_s=1:1), E22 core

<table>
<thead>
<tr>
<th>Np=N1=N2=Ns</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage Inductance (nH)</td>
<td>55</td>
<td>190</td>
<td>419</td>
<td>732</td>
</tr>
</tbody>
</table>

Figure 6-1 Low voltage integrated magnetic circuits (a) HBI^2M, (b) FI^2M
Figure 6-2 Planar winding structure in HBi\textsuperscript{2}M and FI\textsuperscript{2}M with different secondary configuration: (a) single turn secondary winding, $N_1=N_2=1$, (b) multi-turn secondary windings, $N_1>1$ and $N_2>1$

6.2. Development of New Integrated Magnetic Circuit For High Voltage Application

New integrated magnetic circuit must be able to provide the following features:

- small footprint for multi-turn secondary winding,
- continuous output current with inherent ripple current cancellation technique.

At first, a new rectifier circuit is proposed as shown in Figure 6-3. The output current is the sum of two inductor currents. Therefore, it is continuous. Without secondary winding $N_0$ and inductor $L_2$, this rectifier circuit is a half-wave rectifier circuit as often seen in the regular forward converter.
Figure 6-3 New rectifier circuit with current ripple cancellation technique

The purpose of the additional components is to inject a ripple current to the output, whose polarity is opposite to that of the ripple current in L1. The ripple cancellation technique can be obtained.

The operation stage in which \( V_{ab} = -V_2 < 0 \) will be used to discuss the realization of the ripple cancellation effect. During this stage, D1 is off and D2 conducts the load current. The current in L1 decreases because of the voltage applied on L1. If

\[
\frac{N_o}{N_p} V_2 > V_o,
\]

the current in L2 will increase. Consequently, the overall ripple output ripple current, which is the sum of two inductor ripple currents, is reduced.

The proposed rectifier circuit does not have much practical value because it contains too many magnetic components. So magnetic integration is necessary. The integration procedure proposed in Ch. 2 is again applied. There are four steps.

Step 1: Inject a current source to port ab, as shown in Figure 6-4(a). The inductance looking into port ab is

\[
L_{ab} = L_m \frac{N_p}{N_o} \left[ \left( \frac{N_p}{N_o} \right)^2 L_1 + \left( \frac{N_p}{N_o} \right)^2 L_2 \right]
\]

Eq. 6-1
If $L_1$, $L_2$ and $L_m$ can be realized by

\begin{align*}
L_1 &= \frac{N_o^2}{R_1} \\
L_2 &= \frac{N_o^2}{R_2} \\
L_m &= \frac{N_p^2}{R_c}
\end{align*}

Eq. 6-2

$L_{ab}$ can be expressed as

\[ L_{ab} = \frac{N_p^2}{R_c + R_1 \parallel R_2} \]

Eq. 6-3

For an integrated magnetic structure, $L_{ab}$ should be implemented on a single core with a flux of $\varphi_c$ enclosed by winding $N_p$,

\[ L_{ab} = \frac{N_p i_p}{\varphi_c} \]

Eq. 6-4

By combining Eq. 6-4 and Eq. 6-3, the following equation is obtained,

\[ \varphi_c = \frac{N_p i_p}{R_c + R_1 \parallel R_2} \]

Eq. 6-5

The magnetic reluctance circuit and the physical structure are derived as shown in the middle and right side of Figure 6-4(a), respectively.

Step 2: inject current $i_s$ into port ce, as shown in Figure 6-4(b), and derive an E-core structure with $N_s$ on center post.

Step 3: inject current $i_o$ into port ed, as shown in Figure 6-4(c) and derive an E-core structure with $N_o$ on the other outer leg.

Step 4: inject currents to all three ports, as shown in Figure 6-4(d), and the final IM structure can be obtained. It is an E-core structure with center post hosting winding $N_p$ and $N_s$, and one outer leg hosting winding $N_o$. 

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Figure 6-4 Magnetic integration of new rectifier circuit: (a) Step 1: inject a current $i_p$ to port ab and derive an E-core structure with $N_p$ winding on center post, (b) Step 2: inject current $i_s$ into port ce to and derive an E-core structure with $N_s$ on center post, (c) Step 3: inject current $i_o$ into port ed to and derive an E-core structure with $N_o$ on the other outer leg, (d) Step 4: inject currents to all three ports and derive an E-core structure with center post hosting windings $N_p$ and $N_s$, one outer leg hosting winding $N_o$ by applying superposition theory.
Figure 6-5 Integrated magnetic implementation of the proposed new rectifier circuit

Figure 6-5 shows the integrated magnetic implementation for the proposed rectifier circuit. Compared to the discrete magnetic circuit shown in Figure 6-3, this IM circuit reduces secondary winding numbers from four to two and combines three magnetic cores into one. The proposed magnetic integration procedure is again proved to be able to integrate the cores and windings simultaneously.

6.3. DC Characteristics

The investigation of DC characteristics employs the HB configuration. The circuit diagram is shown in Figure 6-6. There are two operation stages in the steady state operation of one switching cycle (as shown in Figure 6-7):

[0, DT], Q1 and D1 on, Q2 and D2 off
[DT, T], Q2 and D2 on, Q1 and D1 off
Figure 6-6 New integrated magnetic circuit in half-bridge configuration

Figure 6-7 Two operation stages of the new HB integrated magnetic circuit: (a) [0, DT], $i_s=0$, (b) [DT, T], $i_s=i_o$.
Following the analysis of two operation stages, the following equations are obtained:

\[
V_1 = (1 - D)V_{in} \\
V_2 = DV_{in} \\
V_o = \frac{N_s}{N_p} V_1 D
\]

Eq. 6-6

By combining the equations shown above, the dc transfer function for the HB configuration can be derived:

\[
V_o = \frac{N_s}{N_p} V_{in} D(1 - D)
\]

Eq. 6-7

6.3.1. Output Ripple Current

From the reluctance circuit shown in Figure 6-7, the output current can be written as

\[
i_o = \frac{\varphi_1 R_1 + \varphi_2 R_2}{N_o}
\]

Eq. 6-8

If only the ac components of the fluxes and current are considered, the output ripple current can be estimated to be

\[
|\Delta i_o| = \frac{|\Delta \varphi_1 R_1 + \Delta \varphi_2 R_2|}{N_o} = \frac{V_o}{f_s} \left| \frac{R_2}{N_s} - \frac{D(R_1 + R_2)}{N_o} \right|
\]

Eq. 6-9

Similar to the current doubler circuit, there exists a critical duty cycle, at which the output ripple current is zero. Therefore, the ripple current cancellation technique is also inherent in this circuit.
The critical duty cycle for the minimum output ripple current is estimated to be

\[ D_{crit} = \frac{N_o}{N_s} \cdot \frac{1}{\frac{R_1}{R_2} + 1} \]

Eq. 6-10

The ratio between two secondary side windings and the ratio between two reluctances can be adjusted in the design to achieve the minimum output ripple current for the given duty cycle range.

6.3.2. Flux distribution

The flux densities on each core leg can be solved from the magnetic reluctance circuits and the external circuit constraints on the winding voltage and currents. Following the procedure described in Ch. 3, the flux distribution inside the magnetic core can be identified. The ac flux density is estimated to be

\[ B_{1m} = \frac{V_o D}{f_s N_o A_1} \]
\[ B_{cm} = \frac{V_o}{f_s N_s A_c} \]
\[ B_{2m} = \frac{V_o}{f_s N_o A_2} \left| D - \frac{N_o}{N_s} \right| \]

Eq. 6-11

A_1, A_2, and A_c are the core cross-sectional areas of outer leg 1, outer leg 2, and center post respectively. As shown in the third equation, there is a duty cycle where the ac flux density in outer leg 2 will be zero. This duty cycle point is expressed as

\[ D_0 = \frac{N_o}{N_s} \]

Eq. 6-12
6.4. Design of New Integrated Magnetic Device with Minimum Footprint

In the new integrated magnetic circuit, the secondary winding on the outer leg needs to carry load current all the time. It is desirable to employ \( N_o=1 \) to minimize conduction loss. On the other hand, \( N_o=1 \) also allows the minimum footprint of the overall planar winding. As shown in Figure 6-8, the overall winding structure is like the conventional transformer winding with an additional tap termination D. \( N_p \) and \( N_s \) windings can be wound on the center post. The footprint of the complete planar winding is minimized.

![Figure 6-8 Planar winding configuration for proposed high voltage integrated magnetic circuit with No=1](image)

To minimize the footprint of the core structure, it is necessary to minimize the core cross-sectional areas. Because of the ripple cancellation technique inherent in the proposed circuit, the core cross-sectional areas are designed to meet the ac flux density requirement and minimum ripple requirement.

6.5. Experimental Verifications

Figure 6-9 shows the experimental waveforms with the new HB IM circuit. In this case, only outer leg 1 is gapped: \( N_i=2, N_o=1 \). Therefore, \( R_1<<R_2 \). According to Eq. 6-8, the critical duty cycle for the minimum output ripple is slightly lower than 50%:

\[
D_{crit} = \frac{N_o}{N_s} \frac{R_2}{R_1 + R_2} \approx \frac{1}{2} \frac{R_2}{R_2} = 0.5
\]

Eq. 6-13
The output ripple current is continuous. At close to 50% duty cycle, the peak-to-peak ripple current is less than 0.5 A. The ringing on the transformer secondary was caused by leakage inductance and junction capacitance of Schottky rectifiers.

### 6.6. Other circuits

By applying the proposed IM circuit to different primary topologies, a family of circuits can be derived based on the proposed integrated magnetic structure, as shown in Figure 6-10. Although only four primary topologies are presented in this figure, the proposed magnetic circuit are not limited to these four configurations. The proposed circuits can be applied to any applications that prefer a multi-turn secondary winding configuration, including low voltage applications.
Figure 6-10 A family of new IM circuits derived from the proposed rectifier topology

6.7. Summary

New rectifier circuits are proposed for the applications that require the use of multi-turn secondary. The output ripple cancellation techniques are inherent in this circuit. By applying the magnetic integration approach proposed in Ch. 2, a family of new integrated magnetic circuits are developed. The proposed IM structure is implemented on an E-core with the center post hosting primary winding and one secondary winding and one outer leg hosting the other secondary winding. By properly designing the ratio of two outer leg reluctances and the turns ratio of two secondary side windings, the output ripple current can be minimized. The proposed magnetic integration technique proves to be able to integrate the cores and windings simultaneously.