Chapter 3

Analysis of Proposed Integrated Magnetic Circuits

Forward circuit with improved integrated magnetics (FI^2M) and HB circuit with improved integrated magnetics (HBFI^2M), as shown Figure 3-1, are used as examples to analyze proposed IM circuits. The discussion will cover steady-state operation, dc characteristics, flux distributions, loss distribution, and the ripple cancellation technique. Steady state operations, dc gains, flux distribution and the loss distribution of the two circuits will discussed separately. The ripple current cancellation technique, which is unrelated to the primary side circuit configuration, will be investigated together. The analytical results will be evaluated with the intention of optimizing the design of the integrated magnetic structure.

3.1. Analysis of FI^2M

The analysis of the operation principles of the FI^2M includes steady state operation, dc transfer function, flux distribution, and loss estimation. Since the duty cycle range of the FI^2M is usually very wide, the loss within each portion of the core has become more uneven. It becomes more important to identify the loss in each portion of the integrated magnetic structure in order to prevent a hot spot inside the structure.

3.1.1. Steady State Operation

The steady state operation of the FI^2M consists of two operation stages, as shown in Figure 3-2 and Figure 3-3. The theoretical waveforms are shown in Figure 3-4 and Figure 3-5. The leakage inductances are neglected and the semiconductor devices are regarded as ideal switching devices to simplify the discussion.
Figure 3-1 Improved IM circuit: (a) HBF$^2$M, (b) FI$^2$M
Stage 1 [0, DT]: main switch Q1 on and clamp switch Q2 off, see Figure 3-2

During this stage, the power is transferred from the input source to the output directly. Since Q1 is on, the input voltage is applied on the primary winding, \( V_p = V_{in} > 0 \). The flux in the center post, \( \varphi_c \), increases, forcing the flux in Outer Leg 1, \( \varphi_1 \), to decrease and the flux in Outer Leg 2, \( \varphi_2 \), to increase. The energy stored in Outer Leg 2 and Center Post increases, and the energy stored in Outer Leg 1 is released to the output. The resulting secondary-winding voltages force Q3 to conduct load current and Q4 to block. Therefore, the load current will flow completely through Winding \( N_1 \), and there is no current in Winding \( N_2 \). The winding currents are estimated to be:

\[
\begin{align*}
  i_p &= \frac{R_c \varphi_c + R_2 \varphi_2}{N_p} \\
  i_1 &= i_o = \frac{R_1 \varphi_1 + R_2 \varphi_2}{N_1} \\
  i_2 &= 0
\end{align*}
\]

Eq. 3-1

During this stage, the flux changes in each core leg are:

\[
\begin{align*}
  \Delta \varphi_1 &= -\frac{V_o DT}{N_1} \\
  \Delta \varphi_c &= \frac{V_{in} DT}{N_p} \\
  \Delta \varphi_2 &= \frac{V_{in} DT}{N_p} - \frac{V_o DT}{N_1}
\end{align*}
\]

Eq. 3-2

Stage 2 [DT, T]: clamp switch Q2 (or its body diode) ON, Q1 OFF, see Figure 3-3

In this stage, the energy stored in the magnetic device during [0, DT] is transferred to the output. Q2 is on and Q1 is off, and the voltage applied on the primary winding (\( V_p = V_{in} - V_c < 0 \)), changes sign. The flux in the center post, \( \varphi_c \), decreases, forcing the flux in Outer Leg 1, \( \varphi_1 \), to increase, and the flux in Outer Leg 2, \( \varphi_2 \), to decrease. The resulting secondary-winding voltages force Q4 to conduct load current and Q3 to block. Therefore, Winding \( N_2 \) conducts the full load current, there is no current in Winding \( N_1 \).
\[
i_p = \frac{R_p \phi_c - R_t \phi_1}{N_p}
\]
\[
i_1 = 0
\]
\[
i_2 = i_o = \frac{R_t \phi_1 + R_s \phi_2}{N_s}
\]

Eq. 3-3

The flux changes in each core leg are:

\[
\Delta \phi_2 = -\frac{V_o (1-D)T}{N_2}
\]
\[
\Delta \phi_c = -\frac{(V_c - V_{in})(1-D)T}{N_p}
\]
\[
\Delta \phi_1 = -\frac{V_o (1-D)T}{N_2} + \frac{(V_c - V_{in})(1-D)T}{N_p}
\]

Eq. 3-4

Figure 3-2 Sub-topology for [0, DT]. Top: integrated magnetic circuit, Bottom: reluctance circuit
Figure 3-3 Sub-topology for [DT, T]: Top: integrated magnetic circuit, Bottom: Reluctance circuit
Figure 3-4 Voltage Waveform in FI²M Circuit
Figure 3-5 Current Waveform in FI²M circuit and Its Equivalent Circuit
3.1.2. DC Gain

To maintain the flux continuity in each core leg, the flux changes during two operation stages have to be equal in magnitude and opposite in polarity. Therefore, given Eq. 3-2 and Eq. 3-4, and the flux continuity requirement in the center post, the relationship between $V_c$ and $V_{in}$ can be obtained:

$$\frac{V_c}{V_{in}} = \frac{1}{1-D}$$

Eq. 3-5

Similarly, the flux continuity requirement in Outer Leg 2 will give the dc transfer function of the FI$^2$M:

$$M = \frac{V_o}{V_{in}} = \frac{N_2}{N_p} \left( \frac{D}{1 + \left( \frac{N_2}{N_1} - 1 \right) D} \right)$$

Eq. 3-6

When $N_1=N_2=N_s$, the dc transfer function can be simplified to

$$M = \frac{V_o}{V_{in}} = D \frac{N_s}{N_p}$$

Eq. 3-7

For the low voltage, high current output application, it is desirable to use single-turn secondary windings to minimize the conduction loss. In the following discussion, therefore, it is assumed that $N_1=N_2=N_s$.

3.1.3. Flux Distributions

The flux distribution within the core structure is shown as Figure 3-6.
3.1.3.1. DC Flux Density

If only the dc components of the fluxes and currents are considered, Eq. 3-1 and Eq. 3-3 can be rewritten as follows.

For [0, DT],

\[ \phi_{1dc} R_1 + \phi_{2dc} R_2 = N_s I_o, \]

Eq. 3-8

\[ \phi_{c_{dc}} R_c + \phi_{2dc} R_2 = N_p I_{p1}, \]

Eq. 3-9

where \( I_{p1} \) is the average dc value of \( i_p \) during [0, DT] interval.

Figure 3-6 Flux distribution within each core Leg
During \([DT, T]\), we have

\[
\varphi_{1dc} R_1 + \varphi_{2dc} R_2 = N_s I_o
\]

Eq. 3-10

\[
\varphi_{cde} R_c - \varphi_{1dc} R_1 = N_p I_{p2}
\]

Eq. 3-11

where \(I_{p2}\) is the average dc value of \(i_p\) during \([DT, T]\) interval.

As shown in Figure 3-2 and Figure 3-3, the converter input current always equals \(i_p\). During \([DT, T]\), the dc input current is zero because the current flows only through \(Cc\). Therefore,

\[
I_{p2} = 0
\]

Eq. 3-12

\[
I_{in} = DI_{p1} + (1 - D)I_{p2} = DI_{p1}
\]

Eq. 3-13

where \(D\) is the duty cycle, \(I_{in}\) is the dc input current, which is also the average value of \(i_p\). So Eq. 3-9 and Eq. 3-11 can be rewritten as

\[
\varphi_{cde} R_c + \varphi_{2dc} R_2 = N_p I_{in} / D
\]

Eq. 3-14

\[
\varphi_{cde} R_c - \varphi_{1dc} R_1 = 0
\]

Eq. 3-15

These two equations are valid for the entire switching period.

From the magnetic structure, we have

\[
\varphi_{1dc} + \varphi_{cde} = \varphi_{2dc}
\]

Eq. 3-16
By combining the previous three equations, we solve for the dc fluxes in each core leg,

\[
\Phi_{1dc} = \frac{R_c}{\Delta} N_p \frac{I_{in}}{D} = \frac{R_c}{\Delta} N_s I_o,
\]

\[
\Phi_{2dc} = \frac{R_c + R_1}{\Delta} N_p \frac{I_{in}}{D} = \frac{R_c + R_1}{\Delta} N_s I_o,
\]

\[
\Phi_{cdc} = \frac{R_1}{\Delta} N_p \frac{I_{in}}{D} = \frac{R_1}{\Delta} N_s I_o,
\]

where

\[
\Delta = R_1 R_2 + R_1 R_c + R_c R_2
\]

The dc flux densities in each core leg are estimated to be

\[
B_{1dc} = \frac{R_c}{\Delta} N_p \frac{I_{indc}}{D} \frac{1}{A_1} = \frac{R_c}{\Delta \cdot A_1} N_s I_o
\]

\[
B_{2dc} = \frac{R_c + R_1}{\Delta} N_p \frac{I_{indc}}{D} \frac{1}{A_2} = \frac{R_c + R_1}{\Delta \cdot A_2} N_s I_o
\]

\[
B_{cdc} = \frac{R_1}{\Delta} N_p \frac{I_{indc}}{D} \frac{1}{A_c} = \frac{R_1}{\Delta \cdot A_c} N_s I_o
\]

Eq. 3-17

Eq. 3-18

Eq. 3-19
3.1.3.2. AC Flux Density

The ac flux swing of each core leg can be simply calculated by the volt-second per turn applying on itself. The ac flux density is then estimated to be

\[ B_{1m} = \frac{(V_o + V_D)D}{2N_s f_s A_1} \]
\[ B_{2m} = \frac{(V_o + V_D)(1 - D)}{2N_s f_s A_2} \]
\[ B_{cm} = \frac{(V_o + V_D)}{2N_s f_s A_c} \]

Eq. 3-20

where \( V_D \) is the rectifier voltage drop. The rectifier drop is considered because it will give a more accurate estimation for a low output voltage, high output current application.

The remanent flux density in each core leg is negligible with the outer leg gappings (refer to the analysis presented in Appendix 1). The maximum flux density in each core leg can then be estimated by the sum of the dc flux density and the ac flux density. The following example will be used to discuss the flux distribution in the FI\(^2\)M.

Example 3-1

\( V_{in} = 70V, \ V_o = 2.5V, \ I_o = 35A, \ \text{Eff}=87\%, \ N_p = 12, \ N_s = 1. \) The planar EI core assembly, E32/6.4/20-3F3 with PLT32/20/3.2-3F3, is used. The winding is an eight-layer PCB with four oz Cu in each layer. Four primary layers are in series with three turns per layer; four secondary layers are in parallel with one turn per layer.

Figure 3-7 plots the maximum flux densities versus duty cycle for Example 3-1. The maximum flux density in Outer Leg 2 is always higher than those in the other two core legs. The lowest duty cycle (or highest input voltage) at full load presents a worst-case scenario for the maximum flux density. Therefore, preventing flux saturation in Outer Leg 2 is the first design priority. Figure 3-8 shows the influence of the leg gappings on the dc flux density distributions. Clearly, increasing the outer leg gap is more effective in reducing the dc flux densities than increasing the center post gap.
Figure 3-7 Maximum flux density vs. duty cycle (outer leg gap is 0.2mm)
Figure 3-8 Influence of gapping on DC flux densities (D=0.49): (a) influence of outer leg gapping on the dc flux densities, with no gap in center post, two outer legs are evenly gapped; (b) influence of center post gapping on the dc flux densities, with both outer legs pregapped at 0.2mm. Plots are generated on E32 planar core.
3.1.4. **Loss within Integrated Magnetic Structure**

The copper loss can be estimated from the rms current on each winding, and the core loss is computed from the ac flux density in each portion of the core. Figure 3-9 shows the estimated copper and core loss for Example 3-1. As the duty cycle increases, the core loss in Outer Leg 1 increases, as do the copper losses in Outer Leg 1 winding and Center Post winding. On the contrary, the core loss of Outer Leg 2 and the copper loss in the Outer Leg 2 winding decrease as the duty cycle increases. But the core loss in Center Post remains unchanged. The overall core loss reaches its minimum at 50% duty cycle. More importantly, there is no hot spot in the core at 50% duty cycle because the core losses in the two outer legs are balanced. The total winding loss is at a minimum at the lowest duty cycle or the highest input. The total power loss in the integrated magnetic device peaks at the maximum duty cycle when the input voltage is lowest. In order to avoid the local hot spot inside the magnetic structure, therefore, it is important to design the turns ratio to obtain a duty cycle near 50%. If the duty cycle range is wide, a proper thermal design must consider the worst-case condition for each winding and each core portion. It is desirable to fill in the air gaps of each core leg and the empty space inside the core windows with good thermal conduction materials.
Figure 3-9 Loss within Integrated Magnetic Structure in FI$^2$M Circuit: (a) copper loss, (b) core loss

### 3.1.5. Soft-Switching Technique in FI$^2$M circuit

In high power applications, large MOSFETs will be adopted for both Q1 and the SR (Q3,4). The turn-on loss in Q1 at high switching frequency may be excessively large
because the effective capacitance across the drain to the source of Q1 is quite large. As analyzed in Appendix 3, the ZVS condition can be expressed as

\[
\frac{\Delta I_m}{2} > \frac{I_o}{N} \frac{\Delta I_{L2}}{2} \quad \text{or} \quad \frac{N}{L_m} > \frac{2f_s I_o}{V_o} - \frac{1-D}{L_2}
\]

Eq. 3-21

Obviously, light load and high line (small D) conditions make it easier to achieve ZVS. Decreasing \( L_m \) can help extend the ZVS load range. Thus, in the proposed IM circuit, increasing the gap in the center post will help achieve ZVS. Like the active clamp forward circuit, the price is a higher primary-side conduction loss \([C14]\).

To lower the cost of fabricating the magnetic core, a spacer gap is usually adopted. This increases the primary side current stress, and therefore, the conduction loss. However, at high switching frequency, the gap in the center post helps reduce the switching loss of the primary side switch. So the overall increase of power loss by using the spacer gap may not be very large.

### 3.2. Analysis of HBI\textsuperscript{2}M circuit

If the asymmetrical duty cycle control is adopted, the steady state operation of the proposed circuit consists of two basic stages. During the first stage \([0, DT]\), the input power is processed. Part of the processed input energy is transferred to the output side directly. The rest is stored in the capacitor and integrated magnetic core. During the second stage \([DT, T]\), the energy stored in the previous stage is released to the output. Therefore, the output side will see a continuous power flow. The detailed operations are described below.

#### 3.2.1. Steady State Operation

Stage 1 \([0, DT]\) as shown in Figure 3-10(a), Q1 on:

Q1 is on and Q2 is off. The voltage applied on the primary winding, \( V_{ab} \), is positive. The induced voltage on the secondary side, \( V_{cd} \), is negative, forcing Q3 to conduct and Q4 to block. Correspondingly, winding \( cd \) conducts the full load current. During this period, the flux in outer leg 1 increases and the flux in outer leg 2 decreases. The magnetic reluctance circuit gives
Stage 2 [DT, T] as shown in Figure 3-10(b), Q2 on:
Q1 is off and Q2 is on. The voltage applied on the primary winding, \( V_{ab} \), is negative. The induced voltage on the secondary side, \( V_{dc} \), is positive, forcing Q4 to conduct and Q3 to block. Correspondingly, winding \( de \) conducts the full load current. During this period, the flux in outer leg 1 decreases and the flux in outer leg 2 increases. Similar to Stage 1, the following equations can be obtained,

\[
R_1\phi_1 + R_2\phi_2 = N_1i_1 = N_1i_o
\]

Eq. 3-22

\[
R_2\phi_2 + R_c\phi_c = N_p i_p
\]

Eq. 3-23

\[
R_1\phi_1 + R_2\phi_2 = N_2i_2 = N_2i_o
\]

Eq. 3-24

\[
-R_1\phi_1 + R_c\phi_c = N_p i_p
\]

Eq. 3-25
3.2.2. DC characteristics

The volt-seconds balance on each core leg gives the steady state voltage on the blocking cap and output terminal:

\[ V_c = DV_{\text{in}} \]

Eq. 3-26

\[ V_o = V_{\text{in}} \frac{N_2}{N_p} \frac{D(1-D)}{1+D(N_2/N_1-1)} \]

Eq. 3-27

If \( N_1 = N_2 = N_s \), the dc transfer function can be simplified to be

\[ V_o = V_{\text{in}} \frac{N_s}{N_p} D(1-D) \]

Eq. 3-28
Figure 3-11 shows the voltage conversion gain of the new half bridge circuit. When \( N_1 \) and \( N_2 \) are not equal, the available duty cycle range for the output voltage regulation can be larger than 50%. So the circuit can operate over a relatively wide input range.

\[
M = \frac{V_0}{V_{in}}
\]

**Figure 3-11 Conversion gain of HBI^2M under different N2/N1**

### 3.2.3. Flux Distributions

Unlike that in a discrete magnetic component, the flux distribution inside the integrated magnetic structure is not uniform. The ac flux in each core leg is determined by the corresponding winding voltage, while the dc flux is determined by the geometry of the core and the load condition. For low-voltage, high-current applications, the adoption of the single-turn secondary winding configuration is highly desirable. In the following discussion, it is assumed that \( N_1 = N_2 = N_s \).

#### 3.2.3.1. AC flux density

The ac flux density in each core leg can be calculated by estimating the volt-seconds per turn seen by each core leg:

\[
B_{cm} = \frac{V_o T}{2 N_s A_c}
\]

\[
B_{1m} = \frac{V_o DT}{2 N_s A_1}
\]

\[
B_{2m} = \frac{V_o (1 - D) T}{2 N_s A_2}
\]

Eq. 3-29
3.2.3.2. **DC flux density**

If only dc fluxes are considered, Eq. 3-22, Eq. 3-23, Eq. 3-24, and Eq. 3-25 can be rewritten as

\[
R_1 \phi_{1dc} + R_2 \phi_{2dc} = N_1 i_{1dc} = N_s I_o
\]

Eq. 3-30

and

\[
R_2 \phi_{2dc} + R_c \phi_{cdc} = N_p \frac{I_{indc}}{D}
\]

Eq. 3-31

respectively.
Again, the relationship between the three fluxes in each core leg gives

$$\phi_{dc} + \phi_{c} = \phi_{dc}$$

Eq. 3-32

By solving Eq. 3-30, Eq. 3-31, and Eq. 3-32, and dividing the fluxes by the cross-sectional areas, the flux densities in each core leg can be obtained as:

$$B_{dc} = \frac{N_p I_{in,dc}}{D(1-D)A_c} \left[ \frac{R_1(1-D) - R_2D}{\Delta} \right]$$

$$B_{1dc} = \frac{N_p I_{in,dc}}{D(1-D)A_1} \left[ \frac{R_c + R_2D}{\Delta} \right]$$

$$B_{2dc} = \frac{N_p I_{in,dc}}{D(1-D)A_2} \left[ \frac{R_c + R_1(1-D)}{\Delta} \right]$$

Eq. 3-33

where $\Delta$ is defined as Eq. 3-18.

If there is no center post gap, $R_c \ll R_1, R_2$:

$$B_{dc} \equiv \frac{N_s I_o}{A_c} \left[ \frac{R_1(1-D) - R_2D}{R_1 R_2} \right]$$

$$B_{1dc} \equiv \frac{N_s I_o}{A_1} \left[ \frac{D}{R_1} \right]$$

$$B_{2dc} \equiv \frac{N_s I_o}{A_2} \left[ \frac{1-D}{R_2} \right]$$

Eq. 3-34

Thus, the dc flux in the center post is at its minimum at the critical duty cycle, $D_{crit}$, the dc flux in Outer Leg 2 is proportional to the duty cycle, and the dc flux in Outer Leg 1 is proportional to $(1-D)$. The critical duty cycle is defined as

$$D_{crit} = \frac{R_2}{R_1 + R_2}$$

Eq. 3-35

Since the HB$^2$M is preferably employed in the application with fixed input and fixed output, the duty-cycle can be designed to be very close to 50%. The ac flux density imbalance in each core leg at extreme duty cycles is not as severe as that in the FI$^2$M.
3.3. Ripple Current Cancellation Technique

The proposed IM structure has an inherent ripple cancellation technique. The following analysis uses the Fi²M as an example. The derived results can be applied to all of the proposed low-voltage IM circuits.

Based on Eq. 3-1 and \( N_1 = N_s \), the output current of the proposed integrated magnetic circuit can be written as

\[
i_o = \frac{R_i \varphi_1 + R_2 \varphi_2}{N_s}.
\]

Eq. 3-36

If only the ac component is considered, the output ripple current can be estimated to be

\[
\Delta i_o = \frac{R_1 \Delta \varphi_1 + R_2 \Delta \varphi_2}{N_s} = \frac{2B_{1m} A_1 R_1 + 2B_{2m} A_2 R_2}{N_s}
\]

Eq. 3-37

By substituting Eq. 3-2 into Eq. 3-37, the output ripple current can be estimated to be:

\[
\Delta i_o = \frac{V_o}{N_s f_s} \left| (1 - D) R_2 - D R_1 \right| \quad \text{or}
\]

\[
\Delta i_o = \frac{V_o}{f_s} \left| \frac{(1 - D)}{L_2} - \frac{D}{L_1} \right|
\]

Eq. 3-38

To account for the secondary side rectifier voltage drop, the output ripple current is estimated as

\[
\Delta i_o = \frac{V_o + V_D}{N_s f_s} \left| (1 - D) R_2 - D R_1 \right| \quad \text{or}
\]

\[
\Delta i_o = \frac{V_o + V_D}{f_s} \left| \frac{(1 - D)}{L_2} - \frac{D}{L_1} \right|
\]

Eq. 3-39

where \( V_D \) is the rectifier voltage drop. It can be seen from the previous two equations that there is a critical duty cycle point, at which the “zero” output ripple current is achieved. The critical duty cycle is estimated to be
\[
D_{\text{crit}} = \frac{1}{\frac{R_1}{R_2} + 1} \approx \frac{1}{\frac{l_{1g}}{l_{2g}} \frac{A_2}{A_1} + 1},
\]

Eq. 3-40

where \(l_{1g}\) and \(l_{2g}\) are the air gaps in outer leg 1, and outer leg 2, respectively, and \(A_1\) and \(A_2\) are the cross-sectional areas of outer leg 1, and outer leg 2, respectively.

To evaluate the factors that affect the output ripple current, the following example will be used. The circuit topology is the Fl3M.

**Example 3-2:**

The electrical specifications and the core design are the same as for Example 3-1. The switching frequency is 100 KHz. The nominal duty cycle for the given electrical specifications is 49.3%. The two outer legs of the E32/6/20 core are gapped by 0.2 mm and the center post is gapped by 0.02 mm. The nominal output ripple current for full-load operation is about 1.035 A. For an efficiency of 87%, \(V_D\) is about 0.375 V at full load.

3.3.1. **Influence of Duty Cycle on Output Ripple Current**

The variation of the ripple current due to the change of the duty cycle can be evaluated from Figure 3-12. It can be seen that the full duty cycle range should be centered around \(D_{\text{crit}}\) in order to minimize the output ripple current for the complete line/load range. This requires a proper design of turns ratio.

![Figure 3-12 Influence of Duty Cycle on Output Ripple Current](image)
3.3.2. **Influence of Frequency on Output Ripple Current**

If the duty cycle is far away from the critical point defined in Eq. 3-40, the output ripple decreases as $f_s$ increases. However, when the frequency changes, the duty cycle also changes because of the increased duty cycle loss resulting from the switching transients. This may have more influence on the overall ripple if the duty cycle is close to the critical point. In some occasions, higher switching frequency may give a higher switching ripple if the duty cycle turns out unfavorably at higher switching frequency.

3.3.3. **Influence of Outer-Leg Reluctances on Output Ripple Current**

Figure 3-13 shows the output ripple current variations due to the change of the magnetic reluctances of two outer legs. In this plot, we assume that the input and output voltage are constant. The nominal reluctances are $2.44E6$ for both $R_1$ and $R_2$, corresponding to a ripple current of about 1.0 A. The first curve is generated by varying $R_1$ without changing $R_2$. If $R_1$ alone is increased by 10% to $2.684E6$, the output ripple current increases to 4.6 A, a 360% increase. Similarly, the second curve shows that a decrease of 10% on $R_2$ alone also produces about 350% increase in the output ripple current. The third curve is generated by varying $R_1$ and $R_2$ with the same ratio. Although the absolute values of both reluctances change by 10%, the output ripple current hardly changes at all. Therefore, the accurate control on $R_1/R_2$ is instrumental in minimizing the output ripple current. In a practical design, this reluctance ratio can be controlled by changing either $A_1/A_2$ or $l_{1g}/l_{2g}$. 
3.3.4. **Leakage inductance effect near critical duty cycle**

For a given magnetic design, the duty cycle plays a major role in determining the output ripple current. However, near the critical duty cycle, the output ripple current may be affected by the leakage inductance if the leakage inductance of the secondary side windings is comparable to $L_1$ and $L_2$, the equivalent inductance represented by two outer legs. Figure 3-14 shows the leakage inductance’s influence on the output ripple current.
Figure 3-14 Simulation waveform of output ripple current with and without leakage inductance

The phenomenon shown in Figure 3-14 originates from the current commutation between two secondary side rectifiers. If there is no leakage inductance, the commutation can be completed instantly. But in practice, the existence of the leakage inductance extends the interval for the current commutation. Consequently, the shape of the output ripple current waveform changes.

To address this issue, the equivalent circuit including the winding leakage inductance, as shown in Figure 3-15(c) is employed. F12M circuit is used as an example to analyze the circuit operation. The derivation of this circuit model can follow the text in [B5]. \( \phi_{1L} \), \( \phi_{2L} \), and \( \phi_{cl} \) are the leakage fluxes of windings \( N_p \), \( N_1 \), and \( N_2 \), respectively.
Q1 turn-off transient, as shown in Figure 3-16(a)

Before Q1 turn-off, D3 conducts the full load current. After Q1 turns off, Vs drops to zero quickly and then reverses its polarity. The current in $L_{1LK}$ starts to decrease and the current in $L_{2LK}$ increases. The load current gradually commutes from D3 to D4. During this period, the voltages seen by $L_1$ and $L_2$ are

$$V_{L1} \equiv \frac{-V_o + \frac{V_c - V_{in}}{N}}{L_{pLK}/N^2 + L_{1LK} + L_{2LK}}$$

$$V_{L2} \equiv \frac{V_{in} - V_c}{N} \frac{L_{2LK}}{L_{pLK}/N^2 + L_{1LK} + L_{2LK}} - V_o$$

Eq. 3-41
During this current commutation, the voltages on both inductors are different from those before and after the current commutation. Consequently, the current slopes in these two inductors during this commutation are different from those before and after the commutation. As a result, the load current, sum of the currents in $L_1$ and $L_2$, has a different current slope.

This commutation interval will last

$$t_{c1} = \frac{L_{plk} + N^2(L_{1lk} + L_{2lk})}{NV_{in}} \cdot I_o$$

Eq. 3-42

Q2 turn-off transient, as shown in Figure 3-16(b)

Before Q2 turn-off, D4 conducts the full load current and D3 is off. After Q2 turns off, $V_s$ drops to zero and reverses its polarity. The current in $L_{2LK}$ starts to decrease and the current in $L_{1LK}$ increases. The load current gradually commutes from D4 to D3. During this period, the voltages seen by $L_1$ and $L_2$ are

$$V_{L1} \equiv -V_o \frac{V_{in}}{N} \frac{L_{1LK}}{L_{plk}/N^2 + L_{1LK} + L_{2LK}}$$

$$V_{L2} \equiv \frac{V_{in}}{N} \frac{L_{2LK}}{L_{plk}/N^2 + L_{1LK} + L_{2LK}} - V_o$$

Eq. 3-43

Since the voltages on both inductors during the current commutation are different from those before and after this commutation, the current slopes in these two inductors during this commutation are different from those before and after this commutation. Consequently, the load current, has a fourth current slope. The length of this commutation is estimated to be

$$t_{c2} \approx \frac{L_{plk} + N^2(L_{1lk} + L_{2lk})}{NV_{in}} \cdot (1 - D) \frac{I_o}{D}$$

Eq. 3-44

Due to the leakage inductance, it is practically impossible to achieve zero output ripple current. To alleviate the influence of the leakage inductance on the output ripple current
Figure 3-16 Illustration of Secondary Side Current Commutation in FT²M Circuit

Figure 3-17 Waveforms to illustrate the leakage inductance’s effect on the output ripple current
and design of the output capacitor, the leakage inductance of each winding must be minimized. The load condition affects the output ripple current in two ways.

First, the load condition changes $V_d$ and the duty cycle. According to Eq. 3-39, the output ripple current will be affected.

Second, the load condition also changes the secondary side commutation times. At heavy load, the effect of the leakage inductance is amplified. The output ripple current changes greatly compared to the light load.

In conclusion, the size of the output capacitor must be chosen with several factors in mind: the complete duty cycle range (with any line and load condition), the reluctance variation range, and the possible leakage inductances influence.